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InfoTracks

Semitracks Monthly Newsletter

Die Attach—Part II

By Christopher Henderson

Die Attach Film

A die attach film, or DAF, can be an alternative to using epoxy tubes. This is a high volume manufacturing process, and die attach films can be used where one does or does not need an electrically conductive path between the die substrate and the leadframe. Die attach film can also provide a more uniform bond line, create a uniform fillet, and avoid die tilt problems. Die attach film typically comes in rolls like we picture here, where the DAF is the same size as the wafer. Accordingly, these rolls can be for 150, 200, or 300 millimeter wafers.

In this Issue:

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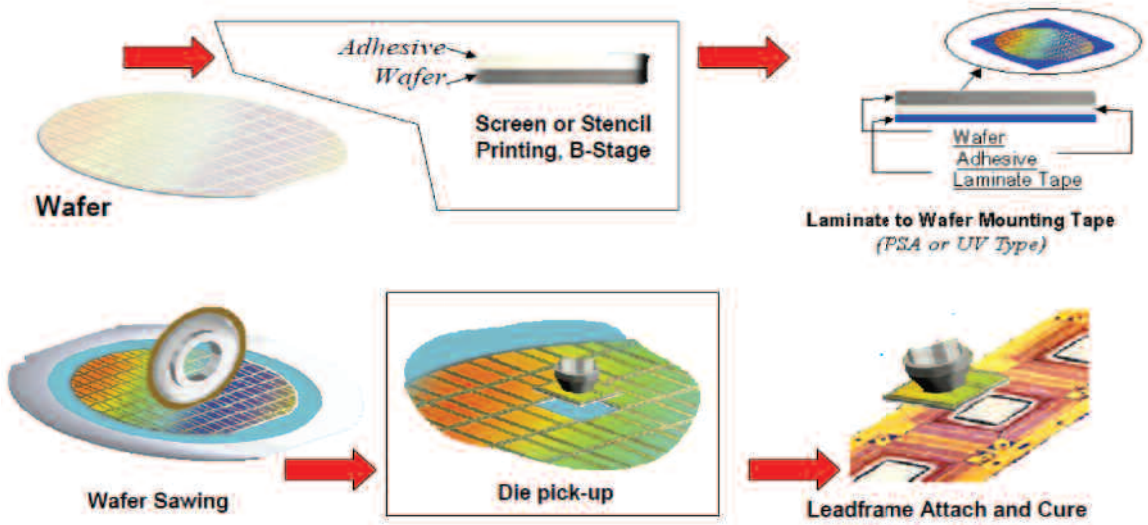
Semiconductor, Microelectronics, Microsystems, and Nanotechnology Training



Alternative process for low thermal conductive or non-conductive requirements; Chip on Lead process flow

Another approach to die attach is a liquid coating applied to the backside of the wafer. This is sometimes referred to as B-stage. A B-stage epoxy resin is a term used to define a one-component epoxy system, using a low reactivity curing agent. This product can be partially cured or "pre-dried" as an initial stage after being applied onto one substrate/surface. It can, at a later time, be completely cured under heat and pressure. This is significantly different from a typical A-stage epoxy system that is provided in a one or two component format and, is cured in one step at ambient or elevated temperatures. B-Stage can be squeegeed on to the back of the wafer, and it can be both insulating and conductive. It is also cheaper than a die attach film. These materials are pre-cured so that the die saw doesn't spread any conductive material. This can be a good alternate process for devices with low thermal conductivity requirements, and works well with a chip of lead process flow.

Die attach can be critical for certain applications. Power dissipation is one consideration that is quite important. If the power dissipation is greater than about 2 or 3 watts, then engineers normally select die attach materials with high thermal conductivity, in the range of three to seven watts per milli-degree Kelvin. This is usually done in conjunction with a heat slug or power pad to aid in the removal of heat. One must watch for die attach delamination, as this can result in sharply higher temperatures. For lower

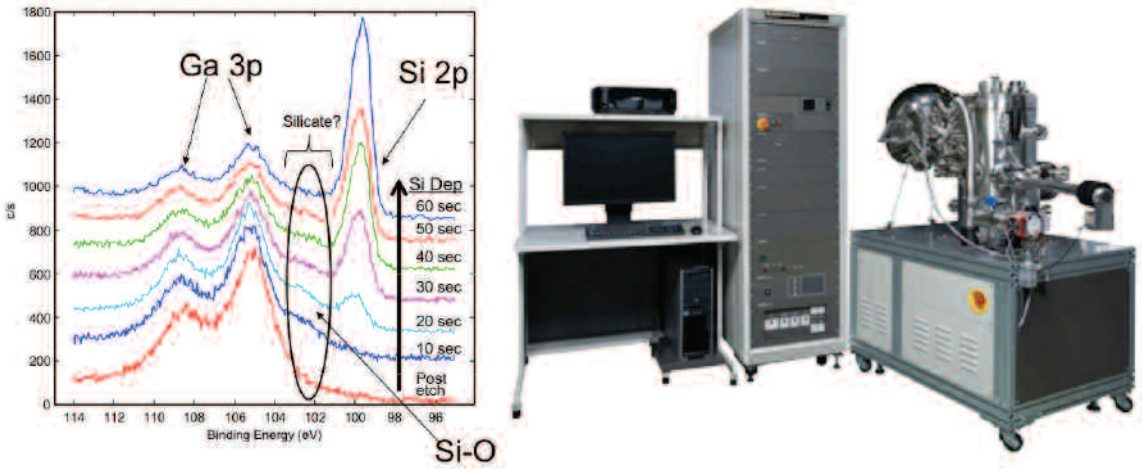
power devices, a die attach thermal conductivity in the range of 0.6 to 2.0 watts per milli-degree Kelvin is acceptable. The die attach can cost less, because less silver is needed to obtain these lower conductivity levels.

The above chart shows data comparing nominal temperatures to the change in temperature at different sensor positions within the chip. The left side shows three regions with good attach from several devices. We use Location 0 max as the reference point, so it shows 0 degree rise. The regions where the temperature rise exceeds 3 degrees would indicate die attach delamination.

Technical Tidbit

ESCA/XPS

In this month's technical tidbit, we'll briefly discuss Electron Spectroscopy for Chemical Analysis and X-Ray Photoelectron Spectroscopy.



Electron Spectroscopy for Chemical Analysis, or ESCA, and X-Ray Photoelectron Spectroscopy, or XPS, are two different analysis techniques obtained from one stimulation method. As such, they are usually performed and analyzed together. ESCA/XPS allows the quantitative analysis and identification of chemical compounds. An X-ray source ejects valence band electrons from the sample. The binding energy of valance electrons is specific to a chemical bond. Spectroanalysis of the binding energies is used to accurately identify chemical compounds. ESCA/XPS is useful for understanding instabilities in oxides, particularly the oxide-silicon interface. By instabilities we mean broken and unterminated bonds in the oxide layer. These bonds can trap and detrap charge, leading to changes, or instabilities, in the behavior of the MOS capacitor, and therefore instabilities in the behavior of CMOS transistors. Data from ESCA/XPS can indicate need for steps such as pre-oxidation cleaning that can improve the yield in a process. This technique does require that one look at a large area test structure, since the x-ray source has a resolution of approximately 7.5 microns.

Ask the Experts

Q: What is the definition of "dump rinse?"

A: In semiconductor processing, a dump rinse is technically called a Quick Dump Rinse (QDR). The quick dump rinse tank is used to remove residues from the wafer surface after chemical processing. After a step that involves chemical processing, the wafers are immediately placed in the QDR tank for rinsing. The term "quick dump" describes the rinse technique used. The system fills the tank with deionized water to the point of overflowing for a short period of time (typically 30 seconds to one minute), similar to the way the overflow rinse works. Next the system opens a door on the tank bottom, draining the tank very quickly. The system refills the tank and repeats the process, typically four to six times. The advantage of the QDR tank is that it helps to remove viscous chemical residues on the wafer surface by introducing shear stresses during the dump phase of the cycle.

Spotlight: Semiconductor Reliability and Qualification

OVERVIEW

Package reliability and qualification continues to evolve with the electronics industry. New electronics applications require new approaches to reliability and qualification. In the past, reliability meant discovering, characterizing and modeling failure mechanisms and determining their impact on the reliability of the circuit. Today, reliability can involve tradeoffs between performance and reliability, assessing the impact of new materials, dealing with limited margins, etc. in particular, the proliferation of new package types. This requires information on subjects like: statistics, testing, technology, processing, materials science, chemistry, and customer expectations. While customers expect high reliability levels, incorrect testing, calculations, and qualification procedures can severely impact reliability. Your company needs competent engineers and scientists to help solve these problems. ***Semiconductor Reliability and Qualification*** is a four-day course that offers detailed instruction on a variety of subjects pertaining to semiconductor reliability and qualification. This course is designed for every manager, engineer, and technician concerned with reliability in the semiconductor field, qualifying semiconductor components, or supplying tools to the industry.

What Will I Learn By Taking This Class?

Participants learn to develop the skills to determine what failure mechanisms might occur, and how to test for them, develop models for them, and eliminate them from the product.

1. **Overview of Reliability and Statistics.** Participants learn the fundamentals of statistics, sample sizes, distributions and their parameters.
2. **Failure Mechanisms.** Participants learn the nature and manifestation of a variety of failure mechanisms that can occur both at the die and at the package level. These include: time-dependent dielectric breakdown, hot carrier degradation, electromigration, stress-induced voiding, moisture, corrosion, contamination, thermomechanical effects, interfacial fatigue, etc.
3. **Qualification Principles.** Participants learn how test structures can be designed to help test for a particular failure mechanism.
4. **Test Strategies.** Participants learn about the JEDEC test standards, how to design screening tests, and how to perform burn-in testing effectively.

COURSE OBJECTIVES

1. The seminar will provide participants with an in-depth understanding of the failure mechanisms, test structures, equipment, and testing methods used to achieve today's high reliability components.
2. Participants will be able to gather data, determine how best to plot the data and make inferences from that data.
3. The seminar will identify the major failure mechanisms, explain how they are observed, how they are modeled, and how they are eliminated.

4. The seminar offers a variety of video demonstrations of analysis techniques, so the participants can get an understanding of the types of results they might expect to see with their equipment.
5. Participants will be able to identify the steps and create a basic qualification process for semiconductor devices.
6. Participants will be able to knowledgeably implement screens that are appropriate to assure the reliability of a component.
7. Participants will be able to identify appropriate tools to purchase when starting or expanding a laboratory.

COURSE OUTLINE

Day 1 (Lecture Time 8 Hours)

1. Introduction to Reliability
    1. Basic Concepts
    2. Definitions
    3. Historical Information
2. Statistics and Distributions
    1. Basic Statistics
    2. Distributions (Normal, Lognormal, Exponent, Weibull)
    3. Which Distribution Should I Use?
    4. Acceleration
    5. Number of Failures

Day 2 (Lecture Time 8 Hours)

1. Overview of Die-Level Failure Mechanisms
    1. Time Dependent Dielectric Breakdown
    2. Hot Carrier Damage
    3. Negative Bias Temperature Instability
    4. Electromigration
    5. Stress Induced Voiding
2. Package Level Mechanisms
    1. Ionic Contamination
    2. Moisture/Corrosion
        1. Failure Mechanisms
        2. Models for Humidity
        3. Tja Considerations
        4. Static and Periodic stresses
        5. Exercises

3. Thermo-Mechanical Stress
    1. Models
    2. Failure Mechanisms
4. Interfacial Fatigue
    1. Low-K fracture
5. Thermal Degradation/Oxidation

Day 3 (Lecture Time 8 Hours)

1. Package Attach (Solder) Reliability
    1. Creep/Sheer/Strain
    2. Lead-Free Issues
    3. Electromigration/Thermomigration
    4. MSL Testing
    5. Exercises
2. TSV Reliability Overview
3. Board Level Reliability Mechanisms
    1. Interposer
    2. Substrate
4. Electrical Overstress/ESD
5. Test Structures and Test Equipment
6. Developing Screens, Stress Tests, and Life Tests
    1. Burn-In
    2. Life Testing
    3. HAST
    4. JEDEC-based Tests
    5. Exercises

Day 4 (Lecture Time 8 Hours)

1. Calculating Chip and System Level Reliability
2. Developing a Qualification Program
    1. Process
    2. Standards-Based Qualification
    3. Knowledge-Based Qualification
    4. MIL-STD Qualification
    5. JEDEC Documents (JESD47H, JESD94, JEP148)
    6. AEC-Q100 Qualification
    7. When do I deviate? How do I handle additional requirements?
    8. Exercises and Discussion

INSTRUCTIONAL STRATEGY

By using a combination of instruction by lecture, video, problem solving and question/answer sessions, participants will learn practical approaches to the failure analysis process. From the very first moments of the seminar until the last sentence of the training, the driving instructional factor is **application**. We use instructors who are internationally recognized experts in their fields that have years of experience (both current and relevant) in this field. The handbook offers hundreds of pages of additional reference material the participants can use back at their daily activities.

The Semitracks Analysis Instructional Videos™

One unique feature of this workshop is the video segments used to help train the students. Reliability Analysis is a visual discipline. The ability to identify nuances and subtleties in graphical data is critical to locating and understanding the defect. Some tools output video images that must be interpreted by engineers and scientists. No other course of this type uses this medium to help train the participants. These videos allow the analysts to directly compare material they learn in this course with real analysis work they do in their daily activities.

International Symposium for Testing and Failure Analysis

November 6-10, 2016
Fort Worth Convention Center
Fort Worth, TX, USA

Registration is available at
http://www.asminternational.org/web/istfa-2016

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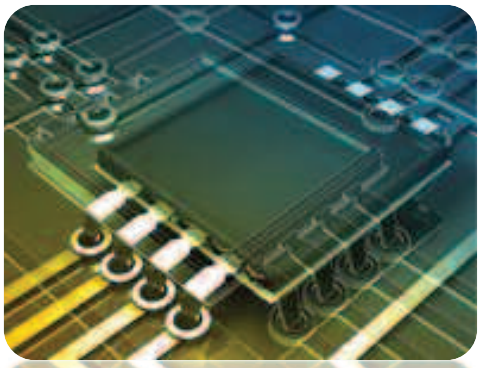
Semitracks will be attending and will be available for meetings. Please contact us at info@semitracks.com to schedule a meeting.



Feedback

If you have a suggestion or a comment regarding our courses, online training, discussion forums, or reference materials, or if you wish to suggest a new course or location, please call us at 1-505-858-0454 or Email us (info@semitracks.com).

To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered in the next newsletter, please contact Jeremy Henderson by Email (jeremy.henderson@semitracks.com).

We are always looking for ways to enhance our courses and educational materials.

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For more information on Semitracks online training or public courses, visit our web site!

http://www.semitracks.com

To post, read, or answer a question, visit our forums.
We look forward to hearing from you!

Upcoming Courses

(Click on each item for details)

Failure and Yield Analysis
May 17 – 20, 2016 (Tue – Fri)
Munich, Germany

EOS, ESD and How to Differentiate
May 23 – 24, 2016 (Mon – Tue)
Munich, Germany

Semiconductor Reliability / Product Qualification
May 30 – June 2, 2016 (Mon – Thur)
Munich, Germany

Advanced Thermal Management and Packaging Materials
June 7 – 8, 2016 (Tue – Wed)
Albuquerque, New Mexico, USA

Wafer Fab Processing
June 27 – 30, 2016 (Mon – Thur)
San Jose, California, USA

Semiconductor Reliability
July 11 – 13, 2016 (Mon – Wed)
Singapore

EOS, ESD and How to Differentiate
July 25 – 26, 2016 (Mon – Tue)
Manila, Phillippines

Semiconductor Reliability / Product Qualification
September 12 – 15, 2016 (Mon – Thur)
Sam Jose, California