Issue 71 May 2015

InfoTracks

Semitracks Monthly Newsletter

Hot Carrier Degradation—Physics

By Christopher Henderson

In this section we will discuss another heavily researched failure mechanism: hot carrier degradation. This mechanism historically was not an issue in larger feature size technologies. However, as technology has decreased from submicron to nanometer feature sizes, hot carrier effects have become more of a concern. First, we'll introduce hot carrier degradation and describe the physics of the mechanism, which will include a discussion on the relationship of hot carriers to other energetic carrier mechanisms, like tunneling currents. We'll discuss when it occurs during transistor behavior, and also discuss the relationship of hot carriers to an observed phenomenon called light emission. We'll then discuss how scientists model the behavior of hot carriers and show several classical models as well as some newer models.

Basically, hot carrier degradation is the result of physical damage to the gate oxide of transistors from high energy electrons. As the electrons decelerate in the drain region, they can scatter into the gate oxide. There they impart damage to the silicon dioxide as they collide with the lattice. This mechanism is more pronounced in smaller technologies because smaller technologies tend to operate with higher electric fields. Most manufacturers scale voltage as they scale the channel length of the transistors, but not at the same rate. This means that the electric fields are creeping ever higher in advanced technologies. This mechanism is also more pronounced in high speed circuits. High speed circuits spend more time in the

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saturation condition as a percentage of the total clock cycle. This means that there is more opportunity for damage to occur. Finally, this mechanism can be more pronounced in some types of analog circuits. If the circuit uses transistors that are biased into saturation, they are susceptible to this mechanism as well.

Figure 1 shows a cross sectional view of a MOS transistor. The source is on the left and the drain is on the right. Let's assume the transistor is biased into saturation. As the electrons leave the source, they drift across the channel until they reach the pinch-off region. Once they enter it, they rapidly accelerate under the influence of the high electric field. As the electrons accelerate, they may collide into the silicon lattice atoms with enough energy to knock off other electrons and holes. Some electrons can scatter into the gate oxide, where hot carrier damage can then occur.

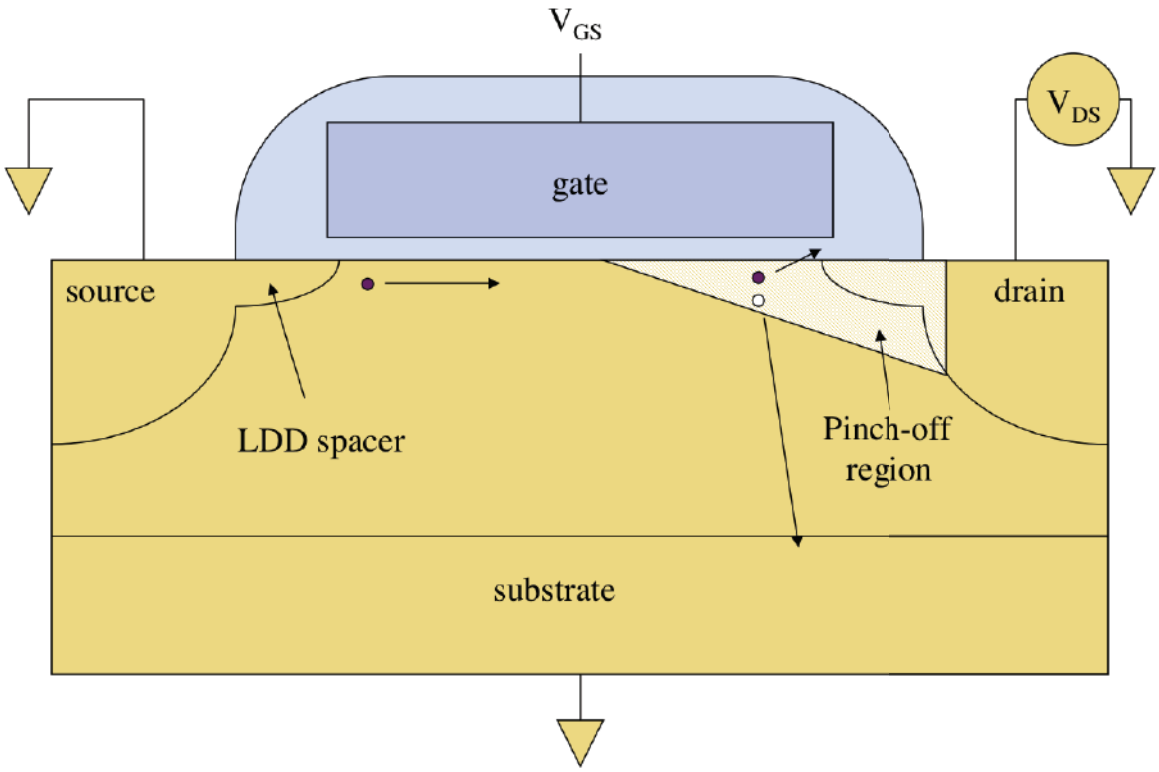


Figure 1. Cross Section of a MOS Transistor.

There are four major types of hot electron injection mechanisms. The first is Fowler-Nordheim tunneling. We also discuss this mechanism in detail in the time dependent dielectric breakdown section. Fowler-Nordheim tunneling can occur from the substrate into the gate, or from the gate into the substrate. The second is Direct Tunneling. This occurs in thin oxides where electrons can traverse the oxide ballistically; that is, without losing any energy. The third injection mechanism is channel hot electron injection. This is the mechanism that most engineers think of when they think of hot carrier degradation. The fourth mechanism is substrate hot electron injection. This lesser-known phenomenon can also cause degradation. We will discuss these mechanisms.

Probably the most widely understood oxide injection mechanism is Fowler-Nordheim tunneling. Fowler-Nordheim tunneling occurs when the electric field is high enough that the electrons have a statistically significant chance of tunneling through the energy barrier presented by the oxide. The left hand side of Figure 2 shows the energy band diagram for an oxide with a high voltage on the gate. As electrons in the conduction band approach the oxide, there is a large difference between the energy of the conduction band of the polysilicon and the conduction band of the oxide. With a sufficiently large electric field applied across the oxide, the conduction and valence bands of the oxide bend, presenting a triangular barrier to the electrons. The thinner this triangular barrier, the greater the probability that the electrons can tunnel through the barrier and into the conduction band of the oxide. Once the electrons have tunneled through the barrier, they gain energy as they move toward the channel. These energetic electrons will then release energy as they reach the conduction band of the channel. In the same manner, holes can tunnel through the barrier from the valence band of the channel into the valence band of the oxide. Fowler-Nordheim tunneling is a symmetric process. If the channel voltage is high with respect to the gate, then electrons can tunnel from the channel to the conduction band of the oxide, and holes can tunnel from the gate to valence band of the oxide. The thinner the oxide, the more Fowler-Nordheim tunneling can occur. The higher the applied voltage, the more Fowler-Nordheim tunneling as well.

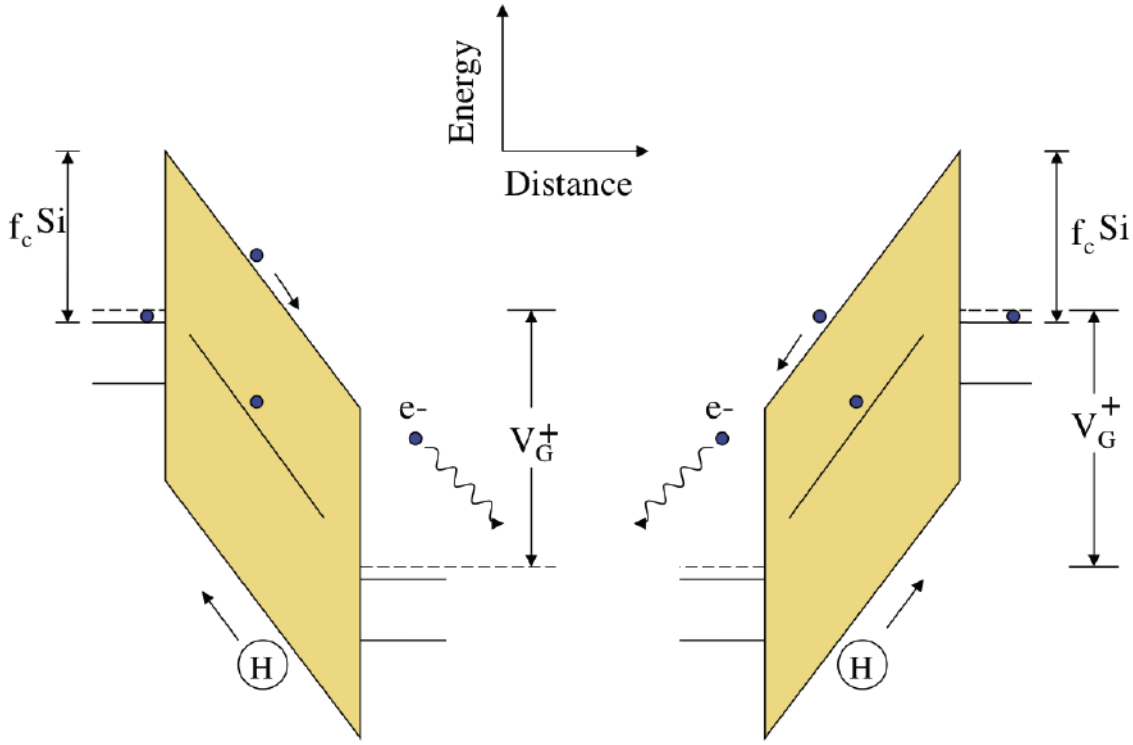


Figure 2. Fowler-Nordheim Tunneling.

As manufacturers have decreased the thickness of the gate oxides, another injection mechanism has become important: direct tunneling. Unlike Fowler-Nordheim tunneling, direct tunneling occurs when the electron passes through the thickest portion of the oxide. In this scenario, the applied voltage across the barrier does not affect the ability of the electron to pass through the oxide. Rather, the probability of tunneling through the oxide is dependent on the energy of the electron, and more importantly, the thickness of the oxide itself. The same factors apply to direct tunneling of holes through the oxide as well. Direct tunneling does not normally damage the oxide, since the electrons do not deposit their energy in the oxide.

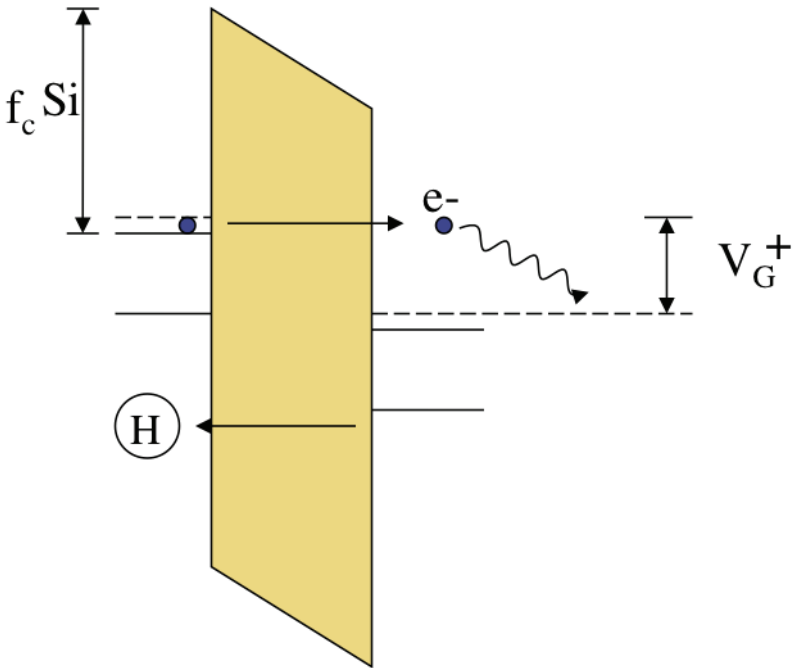


Figure 3. Direct Tunneling.

Figure 4 is a band diagram depicting channel hot electron injection. In this scenario, energetic electrons are scattered toward the gate oxide. These electrons can deposit their energy in the oxide, causing interface states as shown on the left. If the electrons have sufficient energy, they can also create deep traps within the oxide and tunnel through or even pass over the barrier and emerge in the gate region, leading to gate leakage. In addition to electron movement, holes can impact the oxide, creating interface states and traps as well.

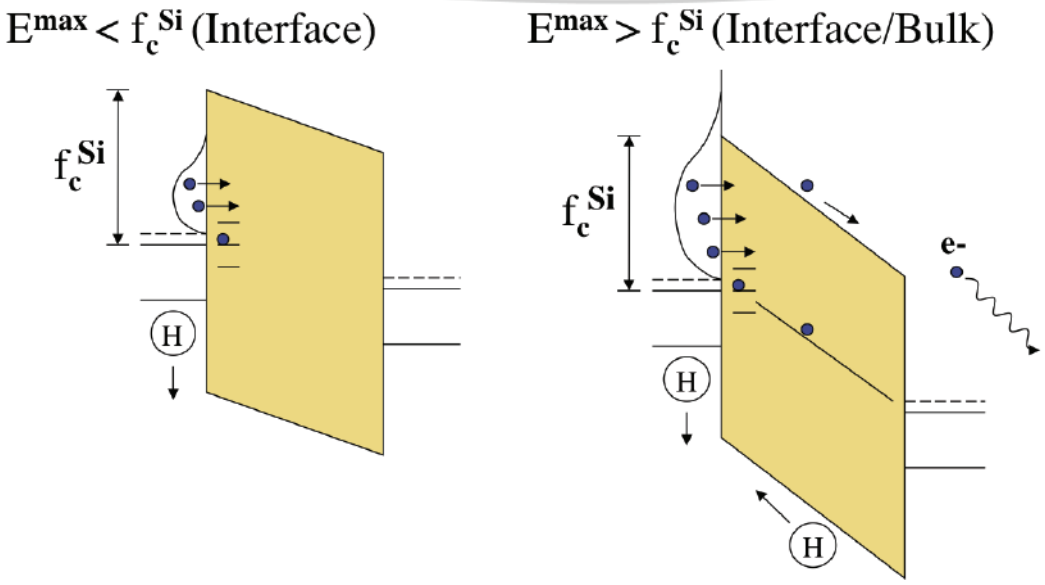


Figure 4. Channel Hot Electron Injection.

A related mechanism is substrate hot electron injection. With substrate hot electron injection, there are two conditions. The first condition occurs when the maximum electric field is less than the workfunction between the conduction band of the silicon and the conduction band of the silicon dioxide. In this scenario, the electrons have a distribution that does not reach the top of the barrier. These energetic electrons can create interface traps at the Si-SiO_2 interface. In the second condition—shown on the right—the electrons have an energy distribution whose tails exceed the height of the silicon dioxide barrier. Not only do these energetic electrons create interface traps, but they can also create bulk traps, or travel through the oxide and emerge in the gate region. Notice that in both situations, hydrogen is released. In the situation on the left, hydrogen is released at the interface; while on the right, hydrogen is released from the interface and the bulk silicon dioxide.

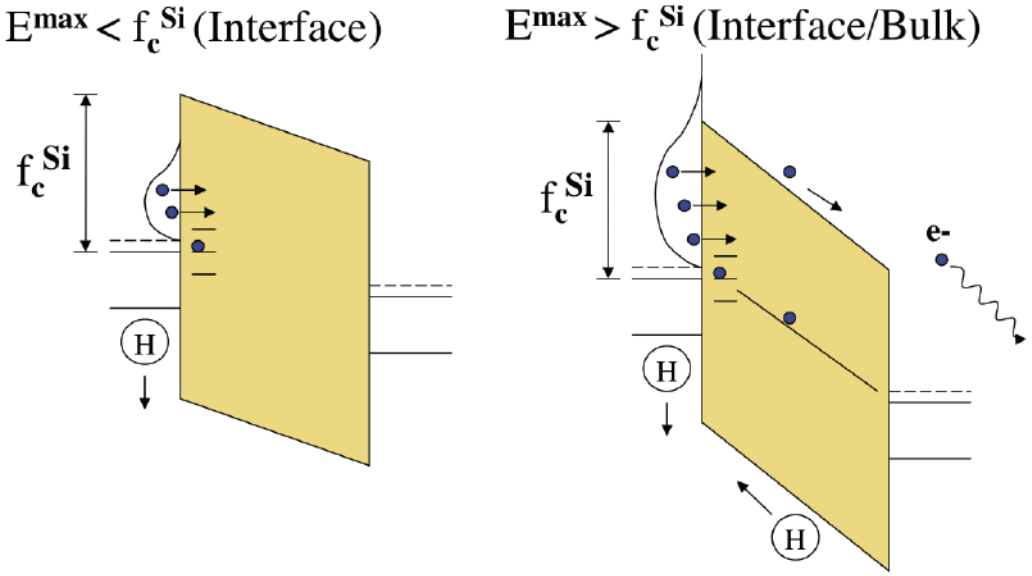


Figure 5. Substrate Hot Electron Injection.

Initially, researchers thought that Fowler-Nordheim tunneling, channel hot electron injection, and substrate hot electron injection resulted in different effects on a transistor. Channel hot electron injection is a low electric field mechanism, substrate hot electron injection is a medium field mechanism, and Fowler-Nordheim tunneling is a high field mechanism. In 2000, Donnelli DiMaria showed that the three mechanisms cause the same degradation. This graph shows that each of the injection mechanisms lie on a single curve. Only electron energy delivered to the appropriate silicon-silicon dioxide interface is important for defect generation and degradation.

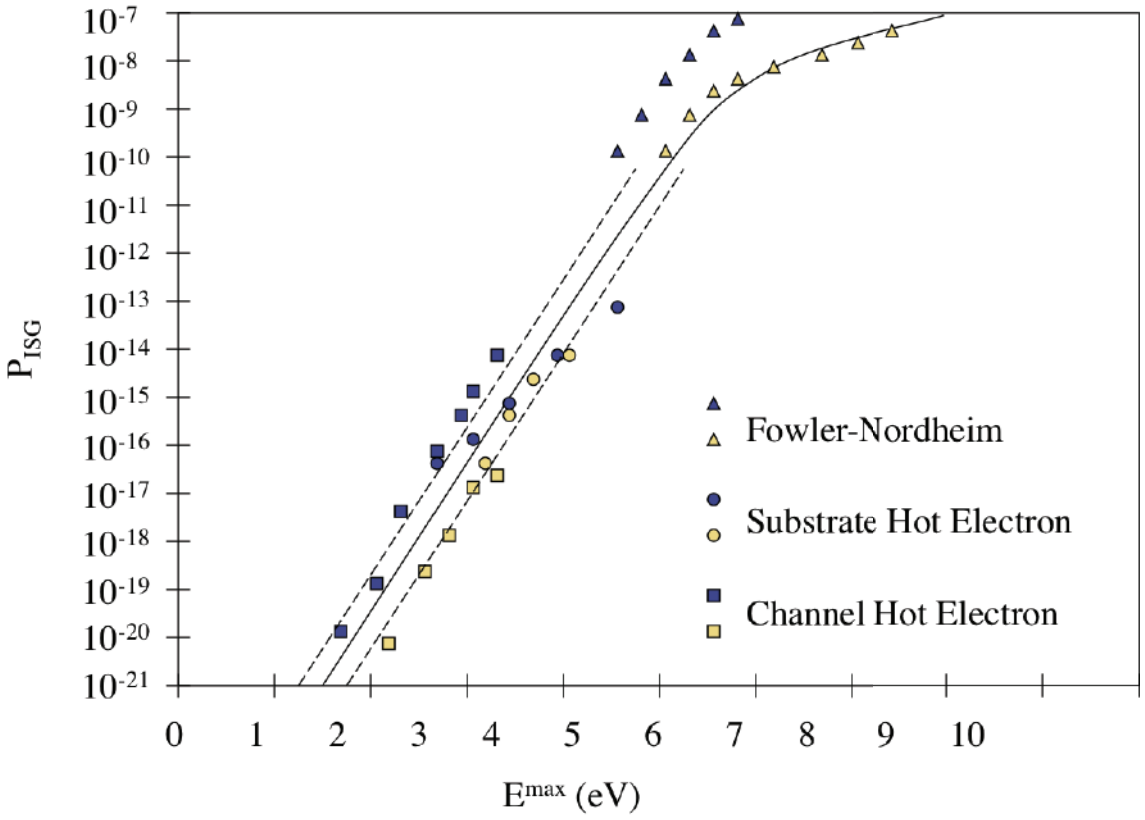


Figure 6. One Degradation Mechanism.

One useful technique to indirectly observe the damage created by hot carriers is to measure the p-well current. The p-well current closely tracks the current into the gate oxide in a hot carrier stress situation. In this graph, one can see that the p-well current peaks at approximately 50% of the drain-to-source voltage. The p-well current is almost non-existent at low gate-to-source voltages, increases rapidly to its peak, and then tails off to a lower value at higher gate-to-source voltages. At low gate-to-source voltages, there is no current through the channel. At high gate-to-source values the pinch-off region decreases, precluding the possibility of electrons scattering into the p-well. The p-well current at these higher values comes solely from diffusion currents.

Technical Tidbit

Dielectric Breakdown Induced Epitaxy

Dielectric Breakdown Induced Epitaxy is a concept developed by reliability researchers to help explain the difference between stable and unstable breakdown filaments in thin gate oxides.

Several researchers have done work showing that after a breakdown occurs, a thin epitaxial region forms. It is referred to as dielectric breakdown induced epitaxy or DBIE (pronounced "D-B-I-E"). DBIE forms because the region gets very hot, causing the silicon to melt. This causes the silicon to epitaxially grow into the gate dielectric. Furthermore, DBIE grows toward the cathode, so there is a polarity dependence to the feature. DBIE stabilizes the preculation path. It helps reduce thermal runaway by consuming system's free energy by reconfiguring the conductive path formed around percolation path. The DBIE dome is approximately two times larger in n-channel transistors than in p-channel transistors.

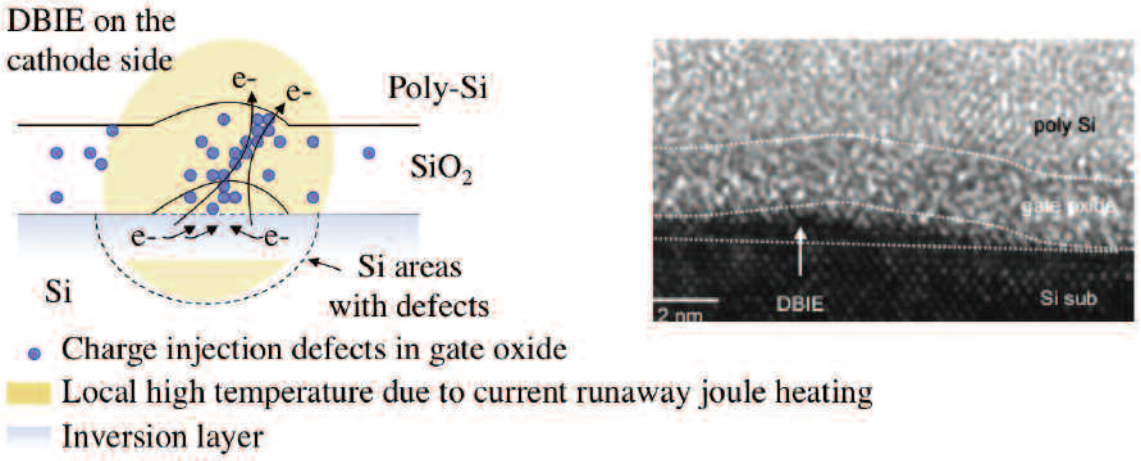
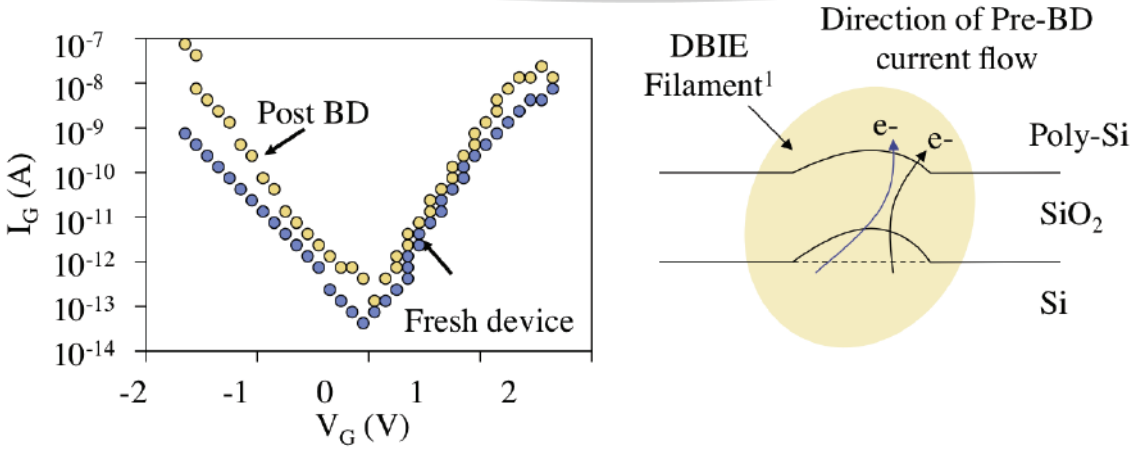


Figure 1. TEM Analysis of DBIE.

Dielectric breakdown induced epitaxy helps to stabilize the filament. When the current is reversed, the filament's physical structure is polarized and becomes stable.



Filament's physical structure is polarized and may become stable when electron current is reversed.

Figure 2. Stable filament formation observed when stress polarity is reversed.

The reason why mixed modes occur appears to be directly related to the amount of power available at breakdown. At lower power levels, there is not enough heating to form the dielectric breakdown induced epitaxy structure. Instead, it produces a silicon-rich area in the gate dielectric. This may simply be the process of oxygen diffusing out under the elevated temperature conditions. The electron current induced local defect generation path continues to degrade, leading to progressive breakdown. For higher power levels, the silicon melts, forming the DBIE dome. The DBIE structure limits the current forming a stable breakdown path. This type of breakdown path allows one to use statistics like prevalence ratio theory and successive breakdown theory. However, in today's circuits, most breakdown events involve low levels of power dissipation, and therefore unstable filaments will dominate.

Ask the Experts

Q: Are there chromium-free chemical etch recipes for decorating silicon?

A: Decorating silicon used to be a straightforward process using the Secco etch, Sirtl etch, or Wright-Jenkins etch. However, in recent years, a number of governments and municipalities have banned chromium due to its toxicity. A few etches like the Dash etch, FS Chromium-free etch and the Jeita/MEMC etch are chromium-free and will etch silicon, but their etch rates are too high to reveal defects in small areas and in SOI materials. Copper decoration in combination with preferential etching is a procedure that can used for the delineation of small crystal defects in bulk silicon and SOI. The crystal defects can be decorated using either $Cu(NO_3)_2$ - or $LiNO_3$ solutions of varying metal concentrations. Experimental parameters such as concentration and volume of the solution used and annealing temperature for the decoration procedure would need to be developed and optimized for each fabrication process.

Spotlight: EOS, ESD and How to Differentiate

OVERVIEW

Electrical Overstress (EOS) and Electrostatic Discharge (ESD) account for most of the field failures observed in the electronics industry. Although EOS and ESD damage can at times look quite similar to each other, the source each and the solution can be quite different. Therefore, it is important to be able to distinguish between the two mechanisms. The semiconductor industry needs knowledgeable engineers and scientists to understand these issues. ***EOS, ESD, and How to Differentiate*** is a two-day course that offers detailed instruction on EOS, ESD and how to distinguish between them. This course is designed for every manager, engineer, and technician concerned with EOS, ESD, analyzing field returns, determining impact, and developing mitigation techniques.

Participants learn to develop the skills to determine what constitutes a good ESD design, how to recognize devices that can reduce ESD susceptibility, and how to design new ESD structures for a variety of technologies.

1. **Overview of the EOS Failure Mechanism.** Participants learn the fundamentals of EOS, the physics behind overstress conditions, test equipment, sources of EOS, and the results of failure.
2. **Overview of the ESD Failure Mechanism.** Participants learn the fundamentals of ESD, the physics behind overstress conditions, test equipment, test protocols, and the results of failure.
3. **ESD Circuit Design Issues.** Participants learn how designers develop circuits to protect against ESD damage. This includes MOSFETs, diodes, off-chip driver circuits, receiver circuits, and power clamps.
4. **How to Differentiate.** Participants learn how to tell the difference between EOS and ESD. They learn how to simulate damage and interpret pulse widths, amplitudes and polarity.
5. **Resolving EOS/ESD on the Manufacturing Floor.** Participants see a number of common problems and their origins.

COURSE OBJECTIVES

1. The seminar will provide participants with an in-depth understanding of electrical overstress, the models used for EOS, and the manifestation of the mechanism.
2. Participants will understand the ESD failure mechanism, test structures, equipment, and testing methods used to achieve robust ESD resistance in today's components.
3. The seminar will identify the major issues associated with ESD, and explain how they occur, how they are modeled, and how they are mitigated.
4. Participants will be able to identify basic ESD structures and how they are used to help reduce ESD susceptibility on semiconductor devices.
5. Participants will be able to distinguish between EOS and ESD when performing a failure analysis.
6. Participants will be able to estimate a pulse width, pulse amplitude, and determine the polarity of an EOS or ESD event.
7. Participants will see examples of common problems that result in EOS and ESD in the manufacturing environment.

INSTRUCTIONAL STRATEGY

By using a combination of instruction by lecture, written text material, problem solving and question/answer sessions, participants will learn practical approaches to the failure analysis process. From the very first moments of the seminar until the last sentence of the training, the driving instructional factor is **application**. We use instructors who are internationally recognized experts in their fields that have years of experience (both current and relevant) in this field. The course notes offer dozens of pages of additional reference material the participants can use back at their daily activities.

COURSE OUTLINE

Day 1

1. Introduction
   a. Terms and Definitions
   b. ESD Fundamentals
   c. EOS Fundamentals
2. Electrical Overstress Device Physics
   a. Sources of EOS
   b. EOS Models
   c. Electrothermal Physics
3. Electrostatic Discharge Device Physics
   a. ESD Models
   b. ESD Testing and Qualification
   c. ESD Failure Criteria
   d. Electrothermal Physics
   e. Electrostatic Discharge Failure Models
   f. Semiconductor Devices and ESD Models
   g. Latchup
4. EOS Issues in Manufacturing
   a. Charging Associated with Equipment
      i. Testers
      ii. Automated Handling Equipment
      iii. Soldering Irons
   b. Charge Board Events
   c. Cable Discharge Events
   d. Ground Loops/Faulty Wiring
   e. Voltage Differentials due to High Current
   f. Event Detection

Day 2

5. ESD Protection Methods
   a. Semiconductor Process Methods
   b. MOSFET Design
   c. Diode Design
   d. Off-Chip Drivers
   e. Receiver Networks
   f. Power Clamps
6. Differentiating Between EOS and ESD
   a. EOS Manifestation
   b. ESD Manifestation
   c. Circuit considerations
      i. Chip level
      ii. System level
   d. Simulating ESD
   e. Simulating EOS
7. EOS/ESD Design and Modeling Tools
   a. Electrothermal Circuit Design
   b. Electrothermal Device Design
   c. ESD CAD Design

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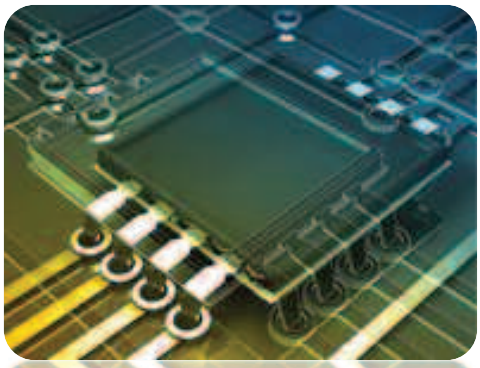
Hsinchu Science Park, Taiwan

Registration is available at
http://ieee-ipfa.org/

Chris Henderson will be attending and will be available for meetings. Please contact us at info@semitracks.com to schedule a meeting.



Upcoming Courses

(Click on each item for details)

Failure and Yield Analysis
August 10 – 13, 2015 (Mon – Thur)
San Jose, California, USA

Semiconductor Reliability
September 2 – 4, 2015 (Wed – Fri)
Munich, Germany

EOS, ESD and How to Differentiate
September 7 – 8, 2015 (Mon – Tue)
Munich, Germany

Product Qualification
September 9 – 10, 2015 (Wed – Thur)
Munich, Germany

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We are always looking for ways to enhance our courses and educational materials.

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