Issue 35 May 2012

InfoTracks

Semitracks Monthly Newsletter

Ion Implantation—Part III

By Christopher Henderson

In part III, the final part of our Ion Implantation series, we will discuss some process monitoring and characterization issues. The major issues include doping process control issues, in-line monitoring and mapping tools to diagnose problems, and offline characterization techniques to look at the results of an implant, or a series of implants and thermal steps.

There are a number of process control issues that affect ion implantation. We list some of the more common issues here. Total implanted dose must be closely controlled for many applications. The dopant profile is also important. One must pay careful attention to the surface concentration, the peak concentration, the implant depth, and lateral distribution effects that are caused by shadowing of overlying structures and thermal diffusion. Another key issue in nanometer-scale ICs is uniformity across the wafer. One needs to examine this problem at both the macro and micro scale. Closely related is wafer-to-wafer and day-to-day repeatability of the dose. The equipment must be precise for each wafer and for each run.

Contaminants are another important issue. Particles can locally shadow or interact with ion implantation, causing problems. The ion beam can sputter material, causing dopant cross-contamination, or introducing metals into the silicon, which can impact device performance. Beam purity is important. We want a consistent energy beam without lower or higher energy tails. Residual crystal damage can lead to leakage and other device performance issues. And finally,

In this Issue:

SEMITRACKS, INC.
Semiconductor, Microelectronics, Microsystems, and Nanotechnology Training

dopant activation is important. We want dopant atoms on lattice sites to create proper semiconductor action. If they remain as interstitials or as clusters, they do not produce the desired electrical behavior.

Characterization is an important aspect of monitoring the ion implant process. This can be done with electrical or physical tools. Four-point probe to measure sheet resistance of implanted layers is an important technique because it is fast and can be done inline with the process. This is the method of choice for monitoring medium and high dose implants. A material's bulk resistivity ρ is defined by this equation:

$$\rho = (ne\mu)^{-1}$$

where n is the number of charge carriers, e is the elementary charge of the electron, and μ is the mobility of the charge carriers. The sheet resistance of a uniformly-doped layer of thickness t is ρ over t. The units of R_S are ohms per square.

For a non-uniformly-doped layer, like a diffused layer, or an implanted layer that has undergone an anneal or high temperature event, the sheet resistance is the integral of the local sheet resistance at each point in the depth z, where z is the layer thickness:

$$R_S = \left(\int n(z) e\mu(z) dz\right)^{-1}$$

To make a four-point probe measurement, first contact the implant or structure of interest with an array of four co-linear probes, apply current across the two outer probes, and measure the voltage drop across the two inner probes. If the probe spacing is equal, and if z is much larger than a, then the sheet resistance can be reduced to the value:

$$R_S = 4.532(V/I)$$

Another in-line measurement tool is the Modulated Optical Reflectance Probe, like the KLA-Tencor Therma-Probe. A modulated argon pump laser generates thermal waves in the silicon wafer, propagating temperature oscillations in thermally conductive material like silicon. The wave propagation is perturbed by lattice disorder, which could be implant damage. This causes local changes to the optical properties of the silicon surface. A helium-neon probe laser measures the net modulated optical reflectance signal, which is correlated to amount of damage. The correlation curves relate implant damage to implant dose. This is the method of choice for monitoring low doses. However, there are several important limitations. First, it is a very indirect measure of dose. The implant damage is a function of not only dose, but of other variables like energy, dose rate, beam spot size, and self-annealing. Another type of tool that can be used for in-line monitoring is the Wafer Surface Scanner. It is primarily used for particle or defect monitoring, but can resolve some implant damage effects.

Let's move on to offline characterization techniques. Since they are primarily destructive and time-consuming, they are done less frequently. They are primarily for characterization but also used for periodic monitoring. The first one is Secondary Ion Mass Spectroscopy or SIMS. It is used to measure dopant profiles in semiconductor devices. The primary ion beam sputters through the implanted layer at a known rate, and the amount of ejected dopant is measured. The technique measures chemical concentration, not carrier concentration. It is also useful for confirming the presence of known or suspected contaminants, if they're present in large-enough amounts. The second technique is Time-of-Flight SIMS or TOF-SIMS. This technique is used to for shallow implants and surface analysis. The primary ion beam is pulsed in the nanosecond range; the secondary ion time-of-flight to detector will be a function of the ion's mass. A separate sputter beam is required to advance to the next depth.

Figure 1. Secondary Ion Mass Spectroscopy Equipment
(left: Quadrupole SIMS; right: Time of Flight SIMS). Images courtesy Cameca and Ion-TOF

Another offline technique is the Transmission Electron Microscope or TEM. It is used to check for residual crystal damage. A focused electron beam passes through a very thin sample, and produces an image based on the electron interaction with the sample due to differences in elements or crystal orientation. It is capable of atomic resolution. Another technique is spreading resistance probing, or SRP. It is used to measure dopant profiles. In order to accomplish this, one must bevel a large-area structure and measure the resistance stepwise across the bevel. The carrier concentration can be computed from measurements of the resistance.

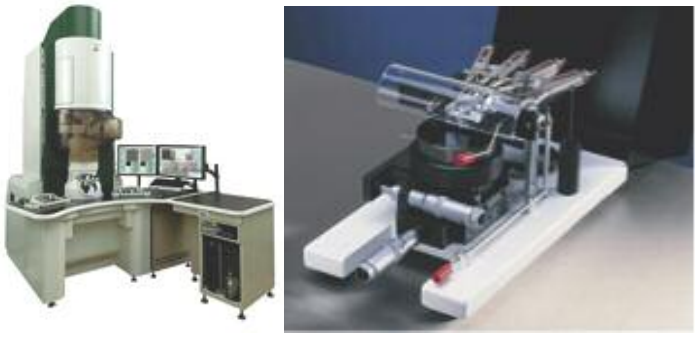
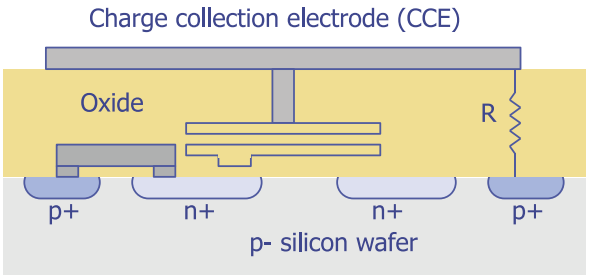


Figure 2. Transmission Electron Microscope (left) and Spreading Resistance Profilometer (right). Images courtesy JEOL and Bridge Technology.

A final offline characterization technique is the charge monitor. It is used to measure charge build-up on a wafer during the ion implantation process. One can use a range of capacitor, EEPROM and MOS test structures. The most popular structure is a EEPROM structure known as CHARM2 . The structure uses large metal charge collection electrodes or antennae tied to the control gate of a EEPROM transistor. Electrodes tied to the silicon through polysilicon resistors measure the net flux. On can then infer voltages and currents on the wafer surface from the threshold voltage shift.

Figure 3. Charge Monitor (after Current)



Finally, let's discuss some new techniques. A popular technique for ultra-shallow junctions is to use cluster boron beams. The basic idea is to implant a boron-based molecule that is much heavier than elemental boron, like octadecaborane. This yields much higher beam current for heavier doping and a factor of twenty better control over the projected range of the boron. It also helps to overcome problems like beam blow-up during acceleration and transport, beam neutralization during deceleration and low beam current instabilities. It also gives sharper implant profiles because of its self-amorphization. It can be implemented with a relatively simple modified source design, and the technology is adaptable to other species like arsenic and phosphorus.

Technical Tidbit

Solid Immersion Lenses

This section provides a brief overview of solid immersion lenses.

We will discuss the rationale for their use. Next, we'll discuss the historical development of these lenses. We discuss their construction, followed by some of their applications in imaging and failure analysis.

The main reason for using a solid immersion lens is to increase spatial resolution. A simplistic way to think about a solid immersion lens is that it acts like a magnifying glass on the circuit. Solid immersion lenses are used to image from the backside of the silicon. This can be advantageous since silicon limits the wavelengths of light through the backside of the silicon to approximately 1.1 microns. With transistor gate lengths approaching 20nm, the size of the source/drain regions is now less than 100nm. In order to distinguish between transistors, we need a technique that not only allows light to pass through the silicon, but also to provide enough resolution to see these structures.

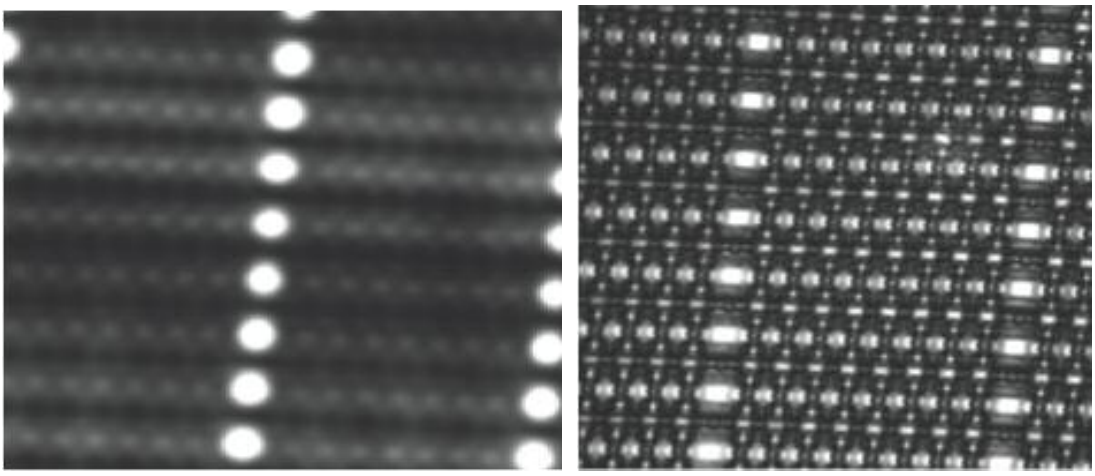


Figure 1. Standard optical imaging (left) and imaging using a solid immersion lens (right)

Much of the early work on Solid Immersion lenses was done at Boston University by Stephen Ippolito, Selim Unlu, and Bennett Goldberg. They first demonstrated the technique for imaging in 2000. In 2003 they showed the technique for failure analysis purposes, and shortly thereafter, a number of semiconductor manufacturers began using SILs for their analysis work. Some used separate SILs, while others machined SILs or SIL-like structures into the backside of the silicon. By 2005, companies like DCG Systems and Hamamatsu were offering SILs with their optical probing tools. Today, most companies analyzing leading edge ICs use SILs in their equipment. There are now more than 30 publications on this technology, and there are likely to be more in the near future as this is still an active area of research.

There are three basic types of SILs: standard hemispherical SILs, aplanatic SILs, and Super SILs. This figure shows an example of a standard hemispherical SIL. The hemispherical shape of the SIL improves the collection efficiency of the light. It also introduces a magnification factor of n, where n is the index of refraction of the SIL.

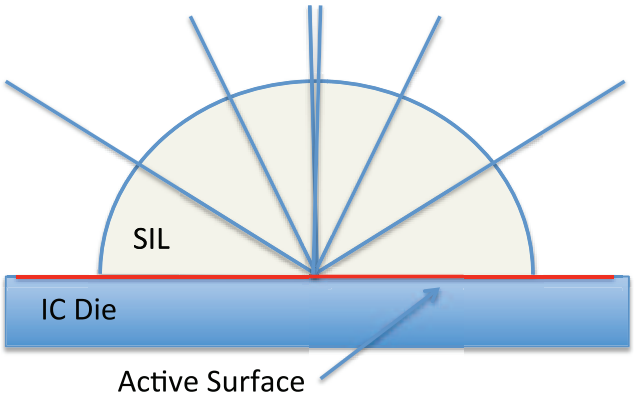


Figure 2. Standard hemispherical SIL

The figure below shows an aplanatic SIL. First, we need to define aplanatic. The aplanatic point or plane is the location at which the light can be focused without any aberration. In an aplanatic SIL, the focal point of the light rays is not at the interface between the SIL and the IC die, but rather at a point within the die. The change in index of refraction between the SIL and the die causes the light to be bent to a new focal point. If the die is thinned appropriately, or if a mount is used, one can tailor the focal point to the active surface of the die.

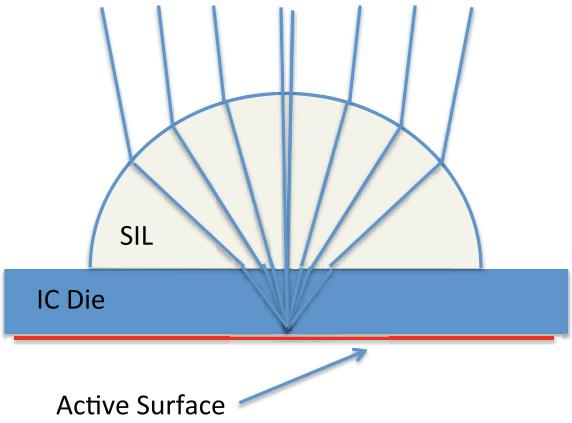


Figure 3. Aplanatic SIL

The Super-SIL is a third type of SIL where the lens is polished flat to a point that permits the light to focus on the feature plane of interest – in this case, the active surface of an IC prepared for backside analysis. Because the focal point is within the IC die, the light rays are significantly below 90 degrees, allowing more light to be captured. In a standard aplanatic SIL, light near the edge of the hemisphere is lost due to reflection, as it is close to 90 degrees.

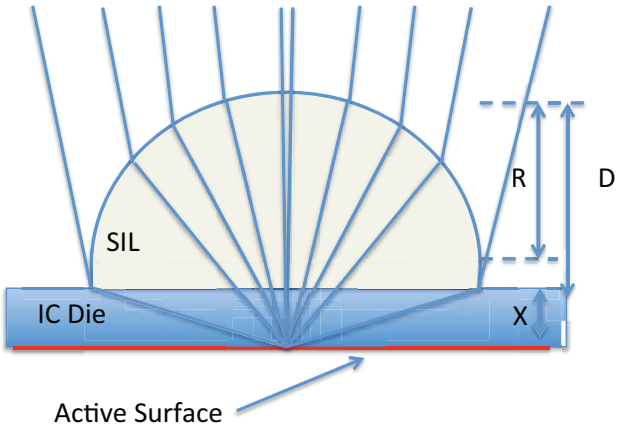


Figure 4. Super-SIL

Researchers are working on methods to improve solid immersion lens technology through the use of alternate lens materials, like gallium arsenide and sapphire, as well as combining SILs with other light technologies like polarization and apodization. For further reading on this topic, there is an excellent review article by Serrels et. al. in the 2008 Journal of Nanophotonics.

Ask the Experts

Q: Is there a way to do a selective wet etch so that only a portion of the chip is etched?

A: Yes there is. You can deposit photoresist, selectively expose it, develop it, and then etch in the area or outside of the area, depending on the type of photoresist used. The paper that discusses this technique is called "Micro-Control of Photoresist Deposition for Failure Analysis of Microelectronic Circuits," presented by K. Hussey, N. Dickson and J. Reyes at ISTFA in 1992.

Spotlight on our Courses: Copper Pillar Technology and Challenges

We are offering a new course on Copper Pillar Bumping in Penang, Malaysia later this year. Here is more information about the course. If there is sufficient demand, we'll also offer it in the US later this year. If you're interested in having this course as an in-house course for your staff, please feel free to contact us at (505) 858-0454, or at info@semitracks.com.

OVERVIEW

The drive to reduce costs in semiconductor and integrated circuits remains a key challenge for the industry. For example, many of today's ICs use expensive gold wiring. As a result, the industry is pushing to use copper wires and copper pillar bumping in an increasing array of applications. This has created a number of challenges related to the bonding and packaging of these components. Copper Pillar Technology and Challenges is a 2-day course that offers detailed instruction on the technology issues associated with today's semiconductor packages. We place special emphasis on current issues like bond formation, bumping, and package design and manufacturing processes. This course is a must for every manager, engineer, and technician working in semiconductor packaging, using semiconductor components in high performance applications or non-standard packaging configurations, or supplying packaging tools to the industry.

By focusing on current issues in packaging technology, participants will learn why advances in the industry are occurring along certain lines and not others. Our instructors work hard to explain semiconductor packaging without delving heavily into the complex physics and materials science that normally accompany this discipline.

Participants learn basic but powerful aspects about the semiconductor packaging. This skill-building series is divided into four segments:

1. **Basic Semiconductor Copper Pillar Bumping Metallurgy:** Participants will study the manufacturing techniques used to create these packages.
2. **Wafer Design Rules and Pillar Design:** The course presents design concepts needed at the wafer and package level to ensure a successful package design. The Back-End-of-Line (BEOL) materials interact with the copper pillar and the copper pillar interacts with the package substrate. These interfaces need to be properly designed to ensure a reliable, cost-effective solution.
3. **Common Package Types:** Participants will learn about the various package types on which on can use copper pillar bumping. This includes both molded packages like Ball Grid Arrays and Quad Flat No-Lead packages, as well as direct chip attach packages such as chip scale packages and package-on-package configurations.
4. **Reliability and Environmental Tests:** The last part of the class brings together the basic principles and selected alloy systems to analyze the results of reliability testing, interpret the observed failure modes to identify root causes, and predict behavior for materials or process changes implemented to lower costs and/or improve reliability. The course covers moisture tests, thermomechanical tests, electromigration, and failure analysis methodology.

COURSE OBJECTIVES

1. At the end of the course, participants will understand the various types of copper pillar bumping techniques and technologies.

2. They will also know about the manufacturing techniques involved in creating these packages.
3. Participants should be able to predict and identify potential reliability problems and the environmental testing that can identify and bring these problems to the surface. They should also know how to interpret failure analysis results.
4. Participants will gain methods to apply these principles to process and material changes to lower cost and produce increased reliability for IC packaging.
5. Participants will be able to make decisions about how to construct and evaluate new packaging designs and technologies.
6. The participant will see several case studies associated with Copper Pillar Bumping.

INSTRUCTIONAL STRATEGY

By using a combination of instruction by lecture, classroom exercises, and question/answer sessions, participants will learn practical information on semiconductor packaging and the operation of this industry. From the very first moments of the seminar until the last sentence of the training, the driving instructional factor is application. We use instructors who are internationally recognized experts in their fields that have years of experience (both current and relevant) in this field.

COURSE OUTLINE

1. Copper Pillar Metallurgy
   a. Types and advantages/disadvantages (This would include copper pillar solder bumping, thermal copper pillar bumping, and thin-film thermoelectric technologies)
   b. Reliability considerations (This would include a discussion on FIT rates, the Arrhenius equation, HAST testing for copper oxidation and degradation, voltage-bias tests, autoclave tests, temperature cycling, electromigration, and failure analysis techniques)
   c. Cost considerations (This would include a discussion on material costs, processing costs, impacts on package size, die size, interposer technologies, and other factors that affect the cost)
2. Wafer design rules and pillar design
   a. Coplanarity (This includes a discussion of wafer flatness, and the techniques necessary to maintain flatness with the assembly/bumping equipment)
   b. Shapes and sizes (This includes factors like copper pillar height, total height, row-to-row pitch, bond pad width, trace pitch, etc.)
3. Common package types and cost
   a. BGA, Leaded packages (QFN, etc.)
   b. Direct chip attach (This includes chip scale packages, and package-on-package configurations like bare die, molded, flip chip, and flip stack technologies)
4. Package reliability
   a. Underfill (This includes a discussion on both reworkable and non-reworkable underfills. It also includes a discussion on flex tests and drop tests)
   b. Overmold, glob top (This includes a discussion on selection of appropriate polymers/thermosets for chip protection)
5. Case Studies

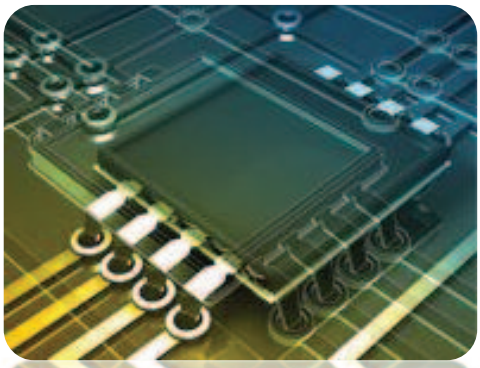
Semitracks will be offering two courses this year in conjunction with Semicon West: Copper Wire Bonding and Challenges, and Advanced Semiconductor Reliability and Characterization Challenges.
Click here for more information on the Copper Wire Bonding Course, and here for the Reliability Challenges Course.

SEMICON® West 2012

July 10 – 12
Moscone Center • San Francisco, California

Stop by and see us!

http://www.semiconwest.org



Feedback

If you have a suggestion or a comment regarding our courses, online training, discussion forums, or reference materials, or if you wish to suggest a new course or location, please call us at 1-505-858-0454 or Email us (info@semitracks.com).

To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered in the next newsletter, please contact Jeremy Henderson by Email (jeremy.henderson@semitracks.com).

We are always looking for ways to enhance our courses and educational materials.

~

For more information on Semitracks online training or public courses, visit our web site!

http://www.semitracks.com

To post, read, or answer a question, visit our forums.
We look forward to hearing from you!

Upcoming Courses

(Click on each item for details)

Semiconductor Reliability
May 14 – 16, 2012 (Mon – Wed)
Munich, Germany

Polymers and FTIR
May 21 – 22, 2012 (Mon – Tues)
Penang, Malaysia

Wafer Fab Processing
June 5, 2012 (Tues)
San Jose, CA, USA

MEMS Technology
June 12 – 13, 2012 (Tues – Wed)
Enschede, Netherlands

Reliability Challenges
July 11, 2012 (Wed)
San Francisco, CA, USA

Copper Wire Bonding
July 11 – 12, 2012 (Wed – Thur)
San Francisco, CA USA

ESD Design and Technology
July 15 – 17, 2012 (Sun – Tues)
Tel Aviv, Israel

Failure and Yield Analysis
July 15 – 18, 2012 (Sun – Wed)
Tel Aviv, Israel

Polymers and FTIR
August 16 – 17, 2012 (Thur – Fri)
San Jose, California