ISSUE #176
March 2024

SEMITRACKS, INC.

INFOTRACKS

YOUR MONTHLY LOOK INSIDE SEMICONDUCTOR TECHNOLOGY

Semiconductor Cleanroom Technology

By Christopher Henderson

In this month's Feature Article, we will continue our discussion of Cleanroom Technology. This Article covers Automated Material Handling Systems. An Automated Material Handling System, or AMHS, is the robotic system used to transport wafer lots from one process tool to the next within the semiconductor cleanroom environment.

The AMHS is an important component of a modern fab. There are different types of AMHS implementations. These implementations can include one or more of the following systems: Automated Guidance Vehicles (AGVs), Rail Guided Vehicles (RGVs), Overhead Hoist Vehicles (OHV) and Overhead Transport (OHT) systems. AGV and RGV systems are more common in older 200mm fabs, while OHV and OHT systems are more common in 300mm fabs. In Figure 1, we show an example of an AMHS that contains both OHV and OHT systems. In conjunction with these systems in 300mm fabs, wafers are processed and transported in an enclosed container called a Front Opening Unified Pod, or FOUP (FOUPs will be covered in more detail later in this presentation). A FOUP is transported from one fab processing tool to another using an Overhead Hoist Transfer vehicle (OHT) system. The OHT travel rail can extend up to 10 kilometers with up to several hundred cars in large fabs, according to Daifuku, a major integrator of AMHS. To get everything working in unison, fabs use various combinations

WHAT'S INSIDE?

Want to take control of your learning? See page 08

Upcoming Courses:

- Wafer Fab Processing
- Failure and Yield Analysis

See page 11 for more details

of these factory automation technologies. Vendors also use Wafers In Process flow techniques, such as real-time dispatching and scheduling, to coordinate the fab flow. Wafers In Process is sometimes referred to as WIP by Fab Process Engineers, but for clarity we will the term "Wafers In Process" in this article.

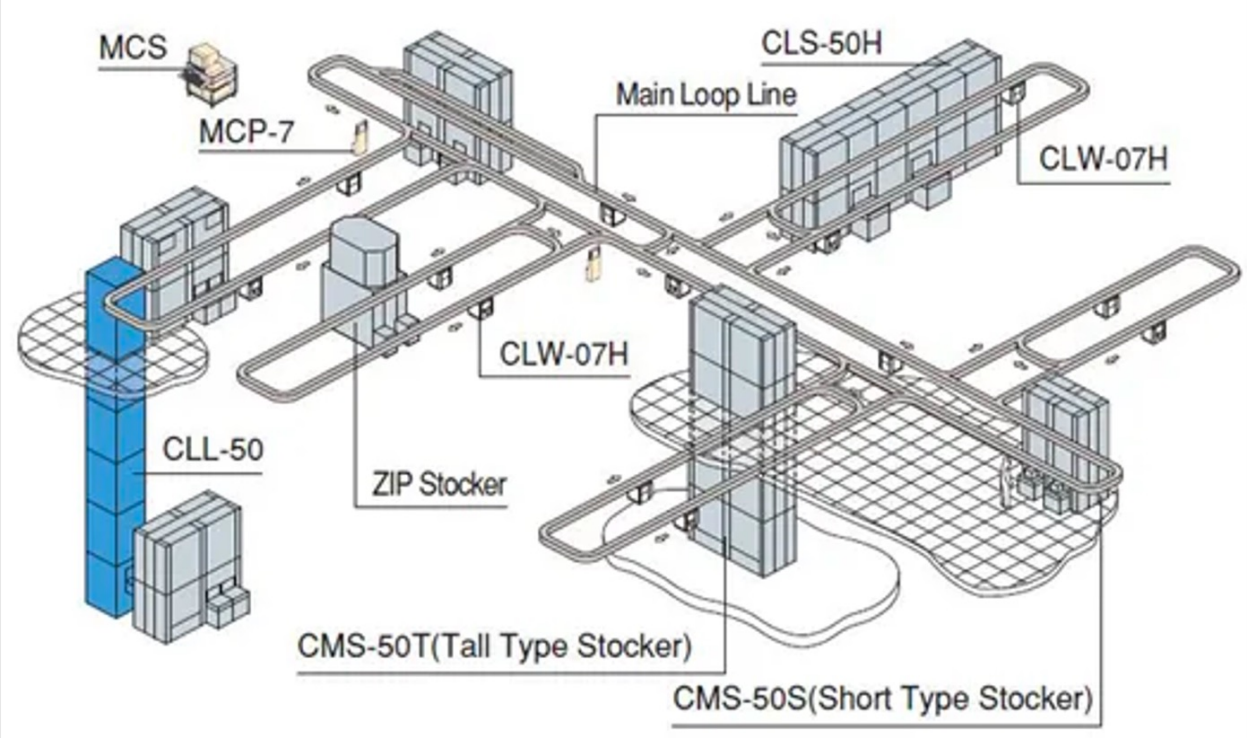

Figure 1- Diagram showing components in an AMHS.

Before we talk about the development of the AMHS, let's briefly review how things were done prior to the AMHS. Historically, fab operators used the SMIF, or Standard Mechanical Interface Pod to transport wafers. The SMIF pod is an isolation technology developed in the 1980s by engineers at Hewlett-Packard in Palo Alto. The SMIF pod was initially used in semiconductor wafer fabrication and cleanroom environments for 150mm wafers, and is currently used for 200mm wafers as well. There is also a SEMI standard for SMIF dimensions, construction, and use. As a point of interest, the leader of the SMIF development team went on to start Technologies, with a license for the SMIF technology from SEMI. Asyst Technologies was later purchased by Brooks Automation, and Brooks Automation still sells SMIF pods for the industry, as of the publication of this article. We show an example of a SMIF pod in Figure 2.

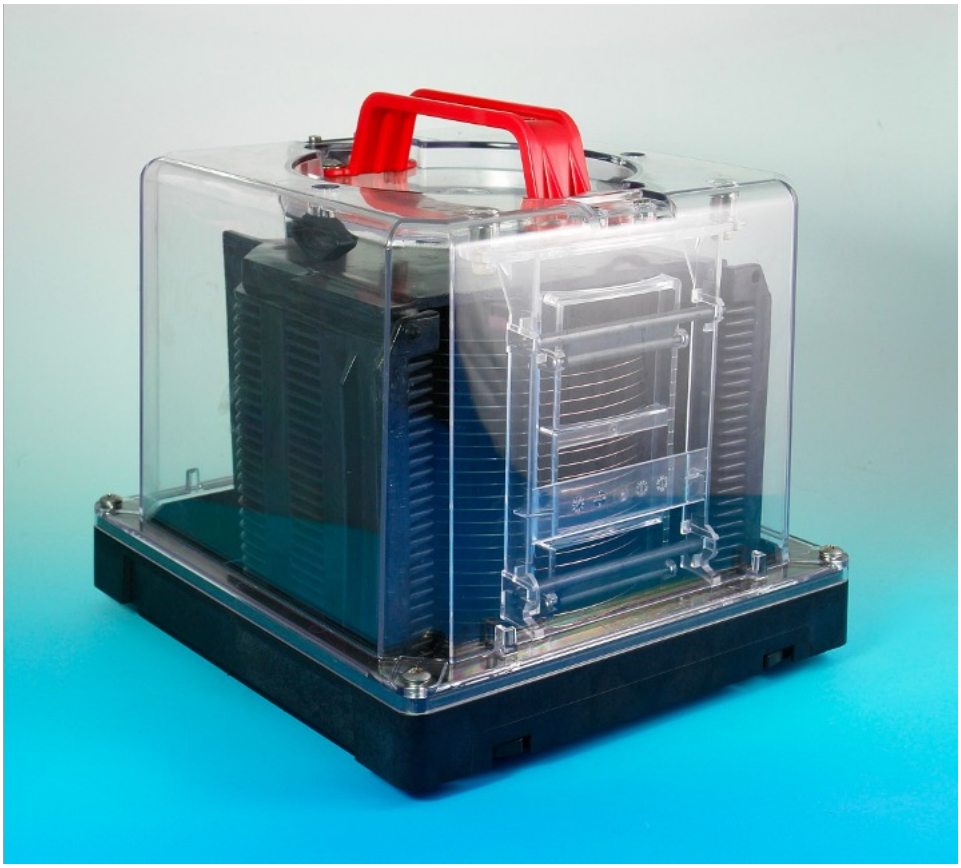

Figure 2- SMIF Pod

Let's briefly discuss the history of the AMHS. Before they existed, fab personnel moved wafer lots to and from various process tools. While much of the transport of SMIF pods could be done with carts, wafer lots still needed to be moved on and off the cart and mounted on the process tool port while keeping the wafers in the SMIF pods. However, the step up to 300mm required major changes. 300mm wafer factories are fully automated while 200mm wafer factories use almost no automation. A FOUP for 300mm wafers weighs about 7.5 kilograms, or about 16.5 pounds, when loaded with 25 300mm wafers, whereas a SMIF pod weighs about 4.8 kilograms, or about 11 pounds, when loaded with 25 200mm wafers. This requires twice the amount of physical strength from factory workers, and increases fatigue and strain injuries.

The AMHS is typically implemented in a new cleanroom facility using an overhead transport scheme, like we show in Figure 3. An overhead transport scheme helps to avoid interfering with personnel movement on the floor of the cleanroom. Furthermore, an overhead transport scheme works well as an interface to process tools, since the FOUPs can be lowered into place at the process tool interface, and then raised once the process tool completes the processing of the wafer lot.

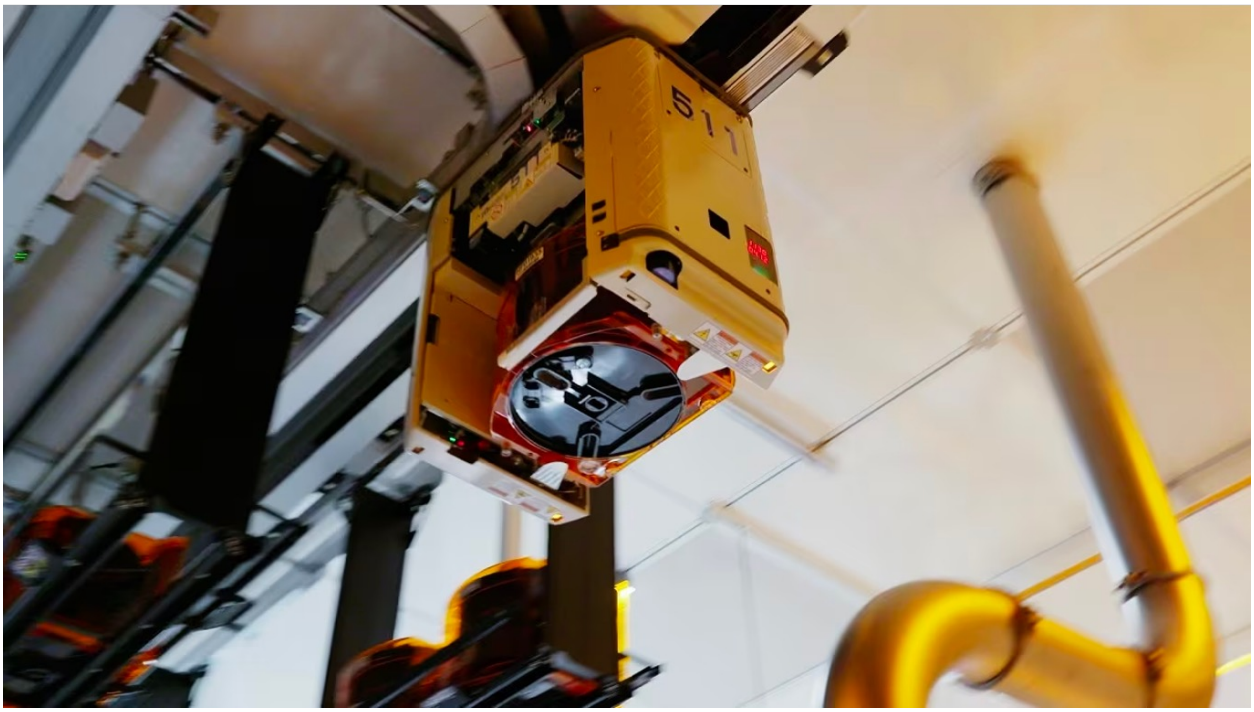

Figure 3- Overhead transport scheme for an AMHS (photo courtesy ST Microelectronics).

In next month's Feature Article, we will continue our discussion of Automated Material Handling Systems and discuss some of the individual components of the system.

Technical Tidbit: The Bosch DRIE Etch

In this month's Technical Tidbit, we will discuss the Bosch DRIE Etch. The most common method for creating the holes through the silicon for Through Silicon Vias (TSVs), or for creating deep trenches in certain Microelectromechanical System (MEMS) devices is to use the "Bosch" Deep Reactive Ion Etch Process, or DRIE etch process. This etch is known as the "Bosch" etch since engineers at Robert Bosch GmbH developed this particular etch process. The DRIE etch process is a type of plasma etching with a high vertical, or "Y", energy sulfur hexafluoride (SF_6) gas. The SF_6 gas contains large amounts of available fluorine, which provides chemical etching. Furthermore, the mass of the fluorine atom can be used to bombard the surface, breaking the surface bonds, to assist with the chemical etching process. To protect the top surface of the wafer in areas where there will be no vias or trenches, engineers use a masking layer that is resistant to fluorine etching, like photoresist (as noted in the top portion of Figure 1). Unfortunately, some lateral, or "X", etching of the sidewall of the via or trench occurs in this process, so engineers need to implement techniques to protect the sidewall of the via or the trench to minimize lateral etching. Engineers accomplish this by using C_4F_8(known as octafluorocyclobutane, or perfluorocyclobutane) to passivate, or cover the sidewalls of the structure. Even with the protective layer, the sidewalls do experience a slight amount of etch below the protective layer, which creates the "scalloped" structure that is common to the Bosch etch. We should also note that the C_4F_8 not only covers the sidewalls of the structure, but also the bottom of the structure. However, the next cycle of SF_6 etches away the C_4F_8 at the bottom of the trench and continues to etch the silicon, like we show at the bottom of Figure 2. Since the fluorine in the SF_6 primarily lands vertical to the surface of the wafer, and the bottom of the trench or via, the sidewalls experience minimal etching of the C_4F_8 layer. One can then repeat the process to etch deeper and deeper into the silicon.

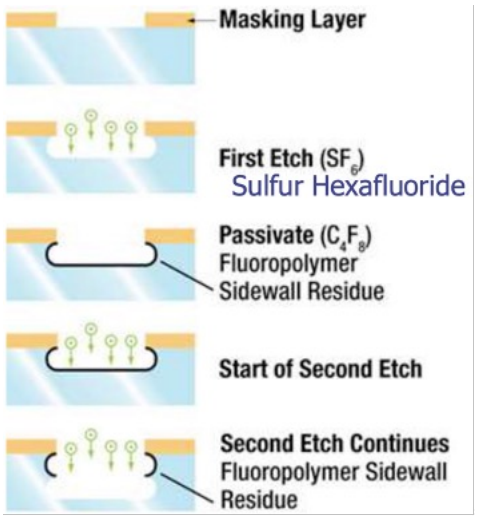

Figure 1- Diagram showing the basic steps in the Bosch etch process.

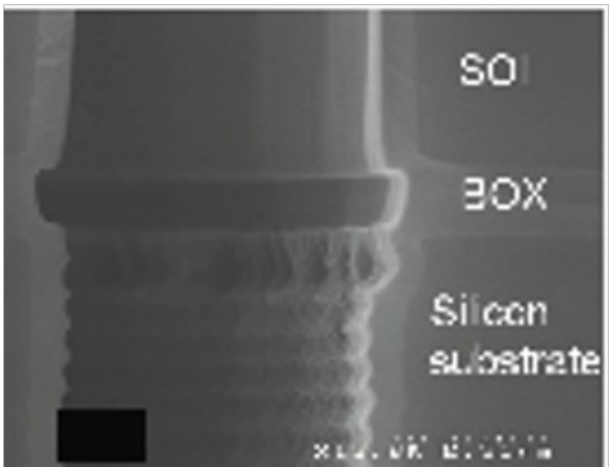

Figure 2- Scanning Electron Microscope (SEM) image showing the scalloped structure of the etch process in the silicon substrate, along with a recessed artifact in the Buried Oxide, or BOX, layer in this SOI wafer after the Bosch etch was performed.

Engineers typically use a High-Density Plasma, or HDP, system to perform the Bosch etch. These systems use a combination of magnetic and electrostatic energy to create the plasma. We show a diagram of the system in Figure 3. By alternating the polarity, one can improve the "Y" velocity of the etch. A typical HDP system can facilitate an etch rate of 50-100μm/min.

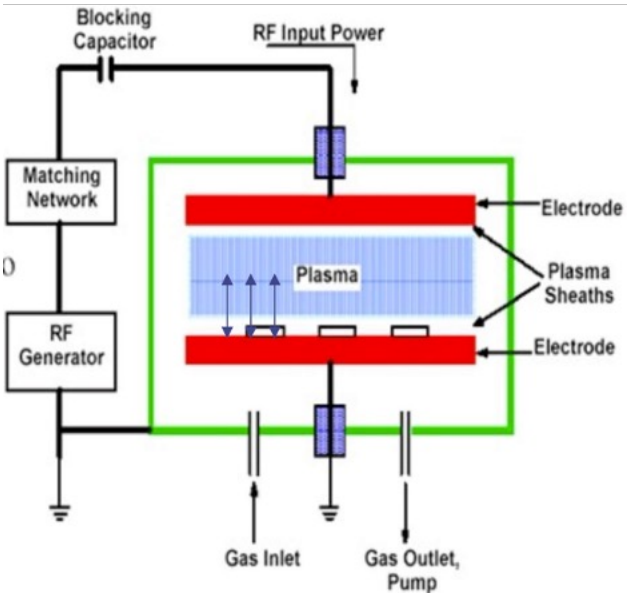

Figure 3- Diagram showing an HDP system configured for the Bosch etch.

Ask The Experts

Q: Why do engineers sometimes perform a "Soft-Landing Step" in conjunction with an etch process?

A: A soft-landing etch step provides a uniform oxide layer thickness, and prevents the underlying substrate from being damaged during etching. A soft-landing etch process is usually performed to etch various layers covering the gate oxide layer. It often involves using Helium Oxide (HeO_2). The HeO_2 forms an oxide layer with a relatively uniform thickness on an open area (e.g., between flash memory transistors). Furthermore, since the helium atom is light and non-reactive, it doesn't etch or damage the surface while the oxide layer is forming. Since the resulting oxide layer covering the substrate has a uniform thickness, no regions of the substrate are exposed to etching. As a result, the substrate is prevented from being damaged during the soft-landing etch process.

Course Spotlight: FAILURE AND YIELD ANALYSIS

OVERVIEW

Failure and Yield Analysis is an increasingly difficult and complex process. Today, engineers are required to locate defects on complex integrated circuits. In many ways, this is akin to locating a needle in a haystack, where the needles get smaller and the haystack gets bigger every year. Engineers are required to understand a variety of disciplines in order to effectively perform failure analysis. This requires knowledge of subjects like: design, testing, technology, processing, materials science, chemistry, and even optics! Failed devices and low yields can lead to customer returns and idle manufacturing lines that can cost a company millions of dollars a day. Your industry needs competent analysts to help solve these problems. ***Failure and Yield Analysis*** is a 4-day course that offers detailed instruction on a variety of effective tools, as well as the overall process flow for locating and characterizing the defect responsible for the failure. This course is designed for every manager, engineer, and technician working in the semiconductor field, using semiconductor components or supplying tools to the industry.

By focusing on a ***Do It Right the First Time*** approach to the analysis, participants will learn the appropriate methodology to successfully locate defects, characterize them, and determine the root cause of failure.

Participants will learn to develop the skills to determine what tools and techniques should be applied, and when they should be applied. This skill-building series is divided into three segments:

1. **The Process of Failure and Yield Analysis.** Participants will learn to recognize correct philosophical principles that lead to a successful analysis. This includes concepts like destructive vs. non-destructive techniques, fast techniques vs. brute force techniques, and correct verification.

2. **The Tools and Techniques.** Participants will learn the strengths and weaknesses of a variety of tools used for analysis, including electrical testing techniques, package analysis tools, light emission, electron beam tools, optical beam tools, decapping and sample preparation, and surface science tools.

3. **Case Histories.** Participants will identify how to use their knowledge through the case histories. They will learn to identify key pieces of information that allow them to determine the possible cause of failure and how to proceed.

COURSE OBJECTIVES

1. The course will provide participants with an in-depth understanding of the tools, techniques and processes used in failure and yield analysis.

2. Participants will be able to determine how to proceed with a submitted request for analysis, ensuring that the analysis is done with the greatest probability of success.

3. The course will identify the advantages and disadvantages of a wide variety of tools and techniques that are used for failure and yield analysis.

4. The course will offer a wide variety of video demonstrations of analysis techniques, so the analyst can get an understanding of the types of results they might expect to see with their equipment.

5. Participants will be able to identify basic technology features on semiconductor devices.

6. Participants will be able to identify a variety of different failure mechanisms and how they manifest themselves.

7. Participants will be able to identify appropriate tools to purchase when starting or expanding a laboratory.

COURSE OUTLINE

DAY 1

1. Introduction

2. Failure Analysis Principles/Procedures
    a. Philosophy of Failure Analysis
    b. Flowcharts

3. Gathering Information

4. Package Level Testing
    a. Optical Microscopy
    b. Acoustic Microscopy
    c. X-Ray Radiography
    d. Hermetic Seal Testing
    e. Residual Gas Analysis

5. Electrical Testing
    a. Basics of Circuit Operation
    b. Curve Tracer/Parameter Analyzer Operation
    c. Quiescent Power Supply Current
    d. Parametric Tests (Input Leakage, Output voltage levels, Output current levels, etc.)
    e. Timing Tests (Propagation Delay, Rise/Fall Times, etc.)
    f. Automatic Test Equipment
    g. Basics of Digital Circuit Troubleshooting
    h. Basics of Analog Circuit Troubleshooting

DAY 2

6. Decapsulation/Backside Sample Preparation
    a. Mechanical Delidding Techniques
    b. Chemical Delidding Techniques
    c. Backside Sample Preparation Techniques

7. Die Inspection
    a. Optical Microscopy
    b. Scanning Electron Microscopy

8. Photon Emission Microscopy
    a. Mechanisms for Photon Emission
    b. Instrumentation
    c. Frontside
    d. Backside
    e. Interpretation

9. Electron Beam Tools
    a. Voltage Contrast
        i. Passive Voltage Contrast
        ii. Static Voltage Contrast
        iii. Capacitive Coupled Voltage Contrast
        iv. Introduction to Electron Beam Probing
    b. Electron Beam Induced Current
    c. Resistive Contrast Imaging
    d. Charge-Induced Voltage Alteration

DAY 3

10. Optical Beam Tools
    a. Optical Beam Induced Current
    b. Light-Induced Voltage Alteration
    c. Thermally-Induced Voltage Alteration
    d. Seebeck Effect Imaging
    e. Electro-optical Probing

11. Thermal Detection Techniques
    a. Infrared Thermal Imaging
    b. Liquid Crystal Hot Spot Detection
    c. Fluorescent Microthermal Imaging

12. Chemical Unlayering
    a. Wet Chemical Etching
    b. Reactive Ion Etching
    c. Parallel Polishing

DAY 4

13. Analytical Techniques
    a. TEM
    b. SIMS
    c. Auger
    d. ESCA/XPS

14. Focused Ion Beam Technology
    a. Physics of Operation
    b. Instrumentation
    c. Examples
    d. Gas-Assisted Etching
    e. Insulator Deposition
    f. Electrical Circuit Effects

15. Case Histories

Upcoming Courses:

Public Course Schedule:

Defect-Based Testing - March 20-21, 2024 (Wed.-Thurs.) | Munich, Germany - $1,195 until Wed. Feb. 28

Advanced CMOS/FinFET Fabrication - May 6-7, 2024 (Mon.-Tues.) | Phoenix, AZ - $995

Failure and Yield Analysis - May 13-16, 2024 (Mon.-Thurs.) | Phoenix, AZ - $2,095 until Mon. Apr. 22

Semiconductor Reliability and Product Qualification - May 20-23, 2024 (Mon.-Thurs.) | Phoenix, AZ - $2,095 until Mon. Apr. 29

Fundamentals of High-Volume Production Test - May 20-21, 2024 (Mon.-Tues.) | Phoenix, AZ - $1,195 until Mon. Apr. 29

Defect-Based Testing - November 18-19, 2024 (Mon.-Tues.) | Munich, Germany - $1,195 until Mon. Oct. 28

Wafer Fab Processing - November 25-28, 2024 (Mon.-Thurs.) | Munich, Germany -$2,095 until Mon. Nov. 4

Failure and Yield Analysis - December 2-5, 2024 (Mon.-Thurs.) | Munich, Germany - $2,095 until Mon. Nov. 11

Semiconductor Reliability and Product Qualification - December 9-12, 2024 (Mon.-Thurs.) | Munich, Germany - $2,095 until Mon. Nov. 18

Have an idea for a course? If you have a suggestion or a comment regarding our courses, online training, discussion forums, or reference materials, or if you wish to suggest a new course or location, please email us at info@semitracks.com

To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered, please contact Jeremy Henderson at jeremy.henderson@semitracks.com

We are always looking for ways to enhance our courses and educational materials and look forward to hearing from you!