Issue 153 March 2022

InfoTracks

Semitracks Monthly Newsletter

MEMS Die Attach Issues

By Christopher Henderson

This month, we will conclude our two-part series of Feature Articles on issues related to the die attach process for MEMS devices by discussing die attach materials. We don't want the die attach material or outgas byproducts to contaminate the MEMS structures causing them to malfunction.

If it is too expensive to use Wafer Level Processing (WLP), or custom pick and place fixturing, there are some options with traditional materials and processes. First, a substrate with the same coefficient of thermal expansion as the MEMS device can be used. Second, appropriate material to control stress can be chosen. You could use an adhesive with a low Young's modulus, or an adhesive with a coefficient of thermal expansion that is between that of the substrate and the die. Third, the bond line can be controlled to minimize stress by minimizing voiding. Also, by incorporating filler beads we can lower the stress and make it more uniform. Fourth, die attach fillet control is critical to controlling stress as well. Figure 1 shows examples of methods to control voiding and stress. Figure 1 (left) shows an example of a die attach dispense pattern that can reduce voiding. Figure 1 (right) shows a fillet structure on the edge of a die that can help reduce the stress.

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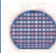

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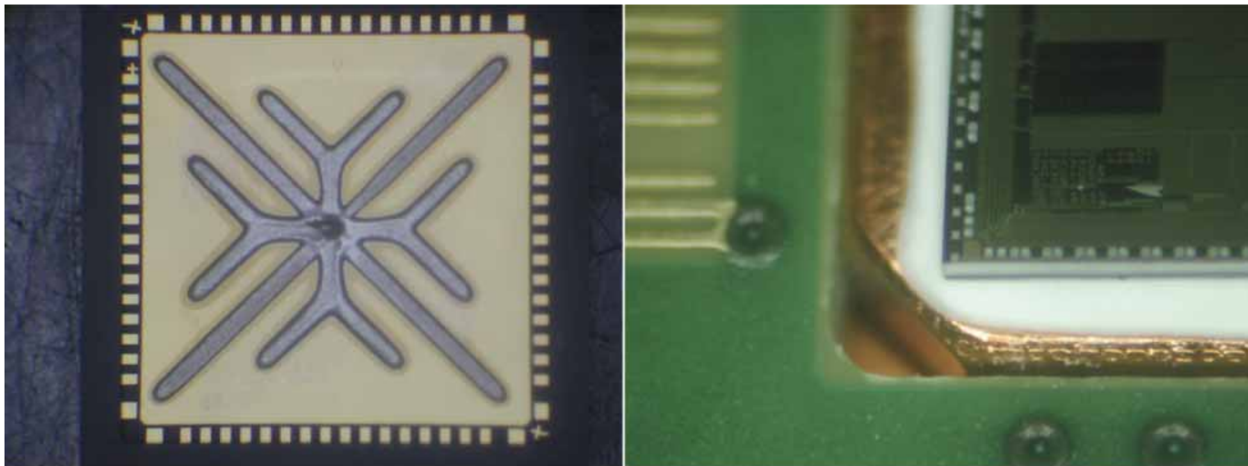

Figure 1. Die attach dispense pattern to reduce voiding (left) and fillet to reduce stress (right).

Now let's look at the effects of substrate and die adhesive materials on die stress. Figure 2 shows examples of warpage with three different combinations of substrates and die adhesive. The image on the left of Figure 2 shows an aluminum oxide (ceramic) substrate, and die adhesive A. Notice the severe warpage in the substrate. The image in the center of Figure 2 shows an aluminum nitride substrate, and die adhesive A. Since aluminum nitride has a CTE that is more closely matched to the die, the warpage is minimal. The image on the right of Figure 2 shows an aluminum oxide (ceramic) substrate, and die adhesive B. Notice that with die adhesive B, which uses a low Young's Modulus material, the die shows very low warpage levels. This is evidenced by the small changes in warpage, compared to the die bonded with adhesive A. Another option is to try and match the CTE of the substrate material more closely with the die CTE.

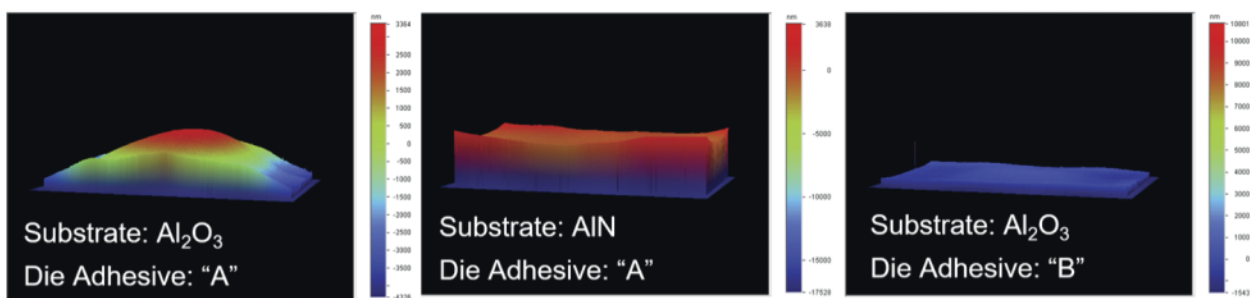

Figure 2. Example of warpage with three different combinations of substrates and die adhesive.

Let's discuss polymer adhesives. We show an example of a polymer adhesive in Figure 3. Polymer adhesives and epoxies are comprised of a bonding material filled with metal flakes. Typically, silver flakes are used as the metal filler since it has good electrical conductivity and has been shown not to migrate through the die attach material. These die attach materials have the advantage of lower process temperatures. These materials generally require between 100 and 200°C to cure the material. They also have a lower built-in stress from the assembly process as compared to a solder attachment process. Furthermore, since the die attach does not create a rigid assembly, the shear stresses caused by thermal cycling and mechanical forces are relieved to some extent. There are a couple of disadvantages to

polymers though. One particular disadvantage of the polymer die attach adhesives is that they have a significantly higher electrical resistivity which is 10 to 50 times greater than solder, and a thermal resistivity which is 5 to 10 times greater than solder. Another disadvantage is that humidity has been shown to increase the aging process of the die-attach material.

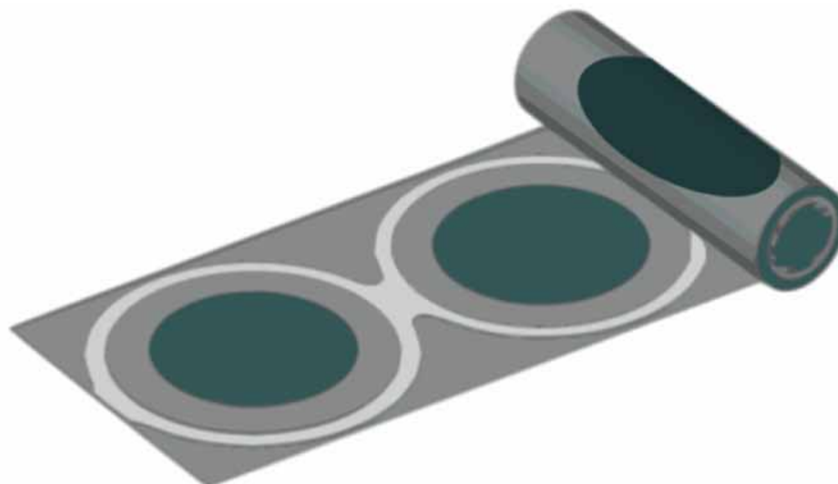

Figure 3. Polymer adhesive die attach sheets.

Engineers can use two additional methods for die attach: solders and glass frit materials. Two important advantages these methods share is no outgassing, and excellent thermal conductivity. This works well for vacuum-sealed packages, and MEMS structures that are coupled with high-power dissipation chips. Generally, when a solder is used, the silicon die would have a gold backing. The most common solder is an 80% 20% gold-tin solder. This solder forms a gold-tin metal alloy, known as a eutectic when the assembly is heated to approximately 250°C in the presence of a forming gas. When this method is applied, we end up with a single rigid assembled part with low thermal and electrical resistances between the MEMS device and the package. We show the die and package forms for this process in Figure 4. One problem with this attachment method is that the solder attach is rigid (and brittle) which means it is critical that the MEMS device and the package CTEs match since the solder cannot absorb the stresses.

Figure 4. Photographs showing images of the MEMS packaging process.

Glass frit bonding, also referred to as glass soldering or seal glass bonding, is a die bonding technique with an intermediate glass layer. This technique requires wafer or die backside preparation. We need to

deposit a layer that can readily adhere to the solder material. There are three common materials: gold-tin eutectics, gold-silicon eutectics, and standard glass frits. A gold-tin preform requires a backside metal layer and an attach temperature of 320°C. We show examples of gold-tin preforms in Figure 5. A gold-silicon material will react with the gold plating in the package and the silicon on the die, but requires a higher attach temperature of 390°C. Glass frit does not require a metal layer, but does require an even higher attach temperature of 450°C. These techniques require the die to be scrubbed into the substrate during the reflow operation, and process control is very critical, since the techniques use high temperatures and require clean surfaces for bonding.

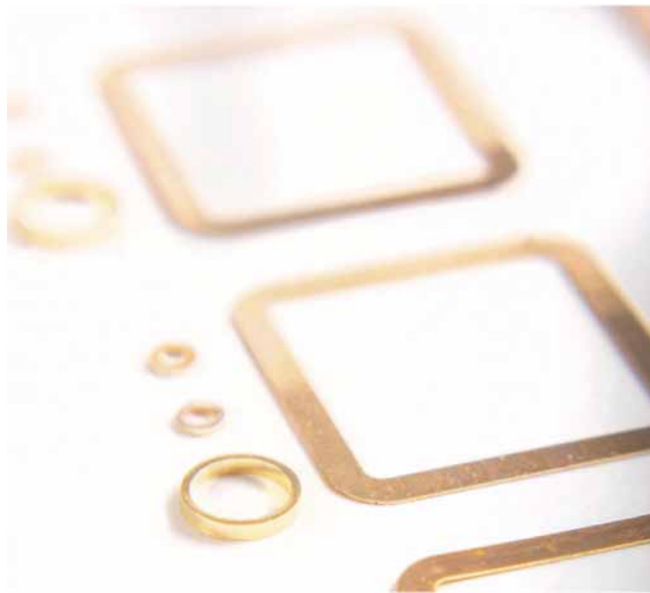

Figure 5. Gold-tin preforms.

Process control during die attach is critical for MEMS devices. The dispense volume and pattern are critical, so computer control is mandatory. A step-cure can help reduce internal stress. For example, engineers might perform the initial cure step for 30 hours at 80°C, and then perform the final cure step for 60 minutes at 150°C. We show the equipment for the curing process in Figure 6. The die alignment is often more critical, so six axes may need to be monitored: X, Y, and Z, along with rotational axes, θ_X, θ_Y, and θ_Z. The oven venting is often optimized to help reduce the redeposition of outgassed volatiles from the die attach material.

Figure 6. Equipment for die attach curing process.

Table 1 summarizes the major properties and issues with die attach materials. Shown are coefficients of thermal expansion, elastic modulus, glass transition temperature, thermal conductivity, cure temperature, reworkability and other issues for epoxy, thermoplastic materials, silicon, and solder. As you can see, certain materials have advantages in some areas. Other materials have advantages in other areas. This means that you, as the engineer, will need to determine which factors are critical, and optimize for those factors.

Parameter	Epoxy	Thermoplastic	Silicone	Solder
CTE	Medium	Medium	Very High	High
Elastic Modulus	Low to Medium	Low to Medium	Very Low	Very High
Glass Transition Temp	Medium	Low to Medium	Very Low	High
Electrical Conductivity	None to Medium	None to Medium	Insulating	Very High
Thermal Conductivity	Low to High	Low to High	Insulating	Very High
Cure Temperature	Low to Medium	Low to Medium	Low	Medium to High
Reworkability	Poor	Excellent	Moderate	Poor
Other Issues	Can Outgas Very Low Cost	Reworkable Suited for Hermetic Pkgs	Can Be Difficult for Wirebonding	Self-centering Low Outgassing

Table 1. Summary of major properties and issues with die attach materials.

In summary, there are several issues which engineers need to consider. First, the sensitive nature of MEMS structures typically does not allow for topside contact of the wafer during die attach pick and place. Second, stress is critical, and affects sensitive MEMS structures, so caution must be taken to choose a material that controls die stress. Third, process control is also critical. Dispense, die placement, die alignment, and die attach cure, all must be done in a highly-controlled manner. Fourth, as a general rule, epoxies are not well suited for hermetic packages as outgassing can affect MEMS structures. The adhesive curing step, along with other high temperature steps, can lead to volatile compounds coating a MEMS structure, rendering it inoperable. Finally, the operations need to be done in a cleaner environment than standard IC die attach to avoid particle contamination.

Technical Tidbit

FPGAs

This month's Technical Tidbit provides a basic overview of Field Programmable Gate Array, or FPGA, devices. We will use a Xilinx Virtex II Pro as an example. Even though this is an older FPGA, the concepts implemented in this device are similar to those implemented in today's state-of-the-art FPGAs. However, it is somewhat easier to understand, due to its basic structure.

This FPGA is available in a variety of different sizes and packaging configurations. We show a photograph of the front and back side of the FPGA in Figure 1 on the left, and a diagram of the pin configuration on the right. The version shown here is packaged in a flip-chip fine-pitched 672 ball Ball Grid Array, or BGA, package. This pin configuration provides for numerous input/output connections to the outside world, should the design engineer require numerous connections into the system.

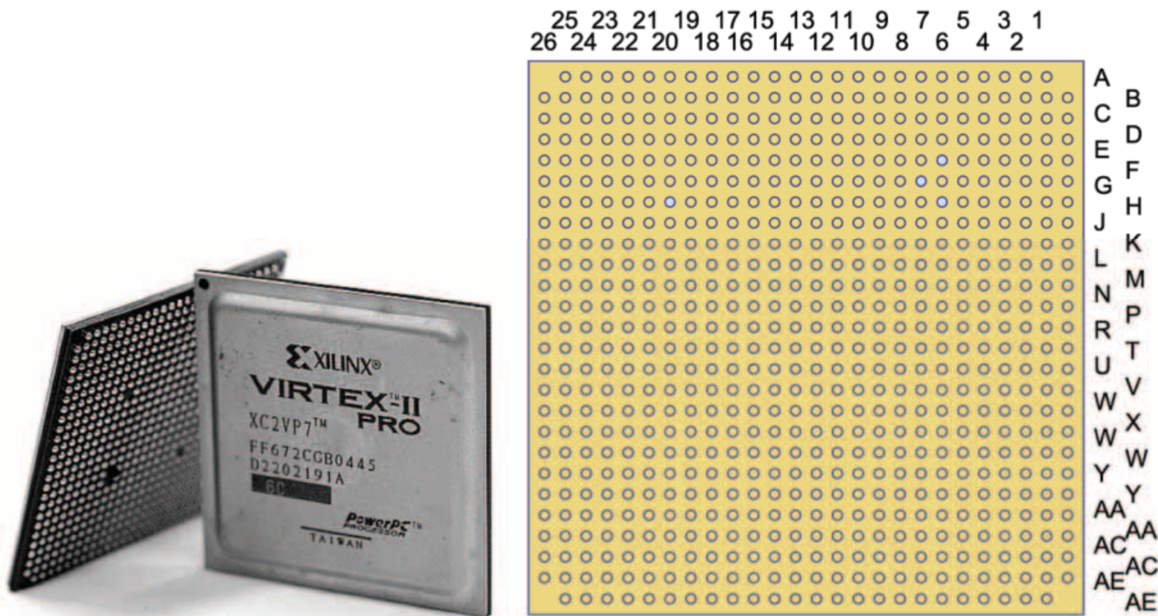

Figure 1. Photograph showing the front and back of Xilinx Virtex II Pro FPGAs (left) and the pin configuration diagram (right).

Figure 2 shows the basic block layout for the Xilinx Virtex II Pro FPGA. We show an optical image of the die on the left, and a block diagram view of the circuitry on the right. The majority of the die is populated with configurable logic blocks for implementing functionality. Some blocks can be reserved for drop-in processing elements, like the IBM Power PC 405 series core. The channels between the logic blocks are configured as block select RAM multipliers. These blocks can perform 18-bit by 18-bit multiplication operations. The blocks on the periphery can be configured with digital clock managers, multi-gigabit serial transceivers, and highly versatile input-output blocks. The digital clock managers can reduce clock skew problems across the chip, generate a wide range of clock frequencies, perform clock multiplication or division, and provide phase shifting. The multi-gigabit serial transceivers provide high frequency serial communications on and off the FPGA. Finally, the input/output logic blocks provide for a

multitude of voltage and drive levels, as well as other useful concepts like low voltage differential signaling.

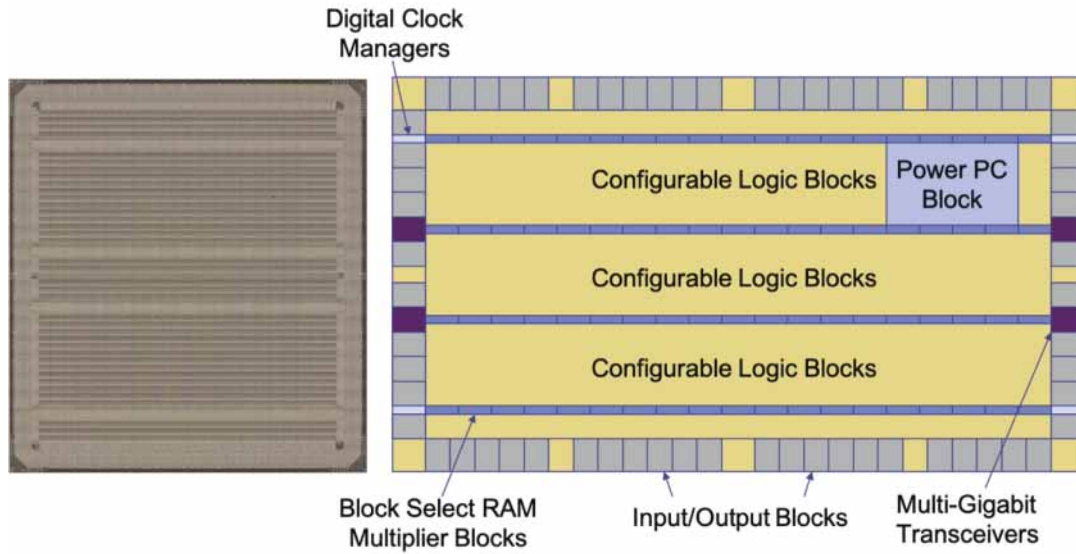

Figure 2. Optical image of the Virtex II Pro die (left)
and the block diagram view of the Virtex II Pro circuitry (right).

A Virtex II configurable logic block contains four similar slices like we show in Figure 3. The four slices are split into two columns of two slices each that contain two independent carry logic chains and one common shift chain. Each slice is tied to a switch matrix, shown on the left, that allows access from the general routing matrix.

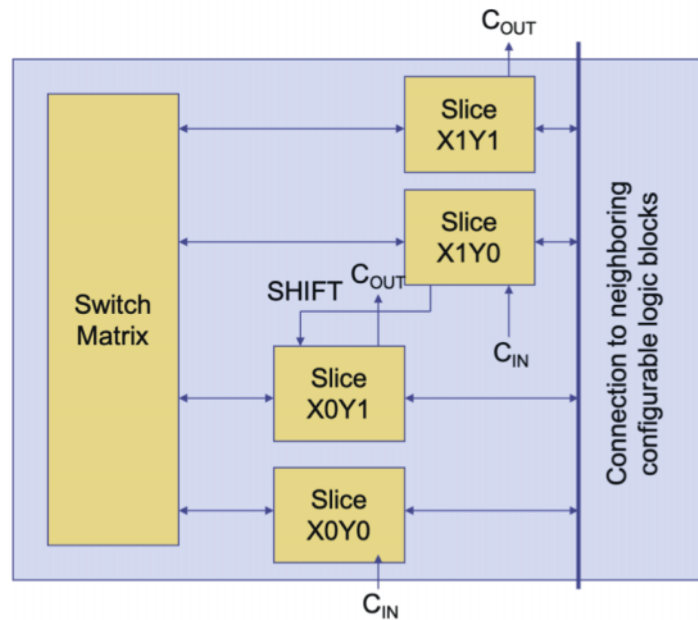

Figure 3. Virtex II Pro Configurable Logic Block.

A Virtex II configurable logic block contains four similar slices. Each slice has an upper half and a lower half. Each half contains a dual port shift register that can be configured as a Look Up Table, 16 bits of Static Random-Access Memory (SRAM), or a 16-bit variable tap shift register element. Each half also contains a register/latch function to implement sequential logic, and the logic to permit integration of the two halves. We show the block diagram of the slices in Figure 4.

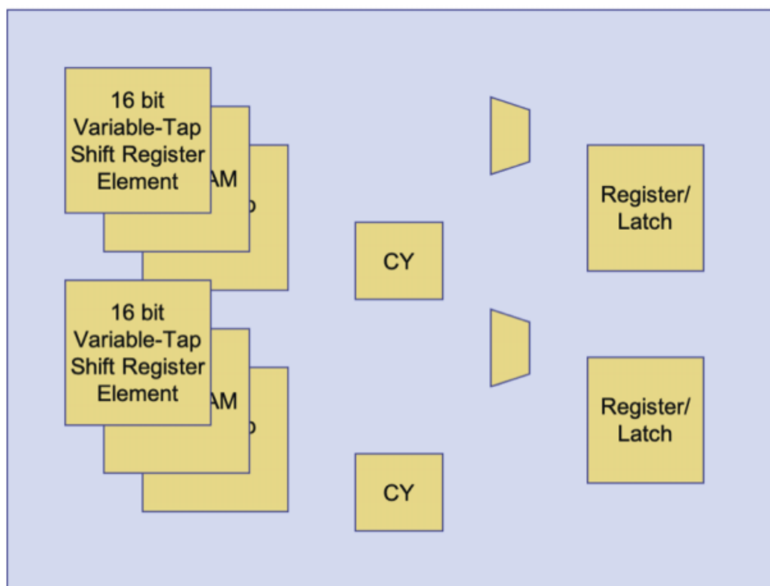

Figure 4. Block diagram of a Virtex II Pro Configurable Logic Block slice.

The Xilinx Virtex II cell architecture, shown in more detail in Figure 5, represents a typical FPGA cell design. In the case of the Virtex II, there is a complementary slice that is not shown. The basic function generator is implemented as a four-input Look Up Table, labeled here as block G. This results in a propagation delay that is independent of the function that one implements. The function can exit the cell block through the GYMUX, go to the dedicated exclusive or gate, input the carry logic multiplexer, feed the d input on the register, or feed the logic from the bottom slice to implement more complex logical functions. The register can be configured either as an edge-triggered d flip flop or as a level sensitive latch. Each slice has clock, clock enable, set and reset signals to provide additional control. The set function can be configured to be either synchronous or asynchronous. The dual port shift register can also be configured as memory. One can implement a sixteen by one-bit synchronous random access memory resource. Since two slices can work in tandem, one can create a variety of memory blocks ranging from single port sixteen by eight blocks to a dual port sixty-four by one block.

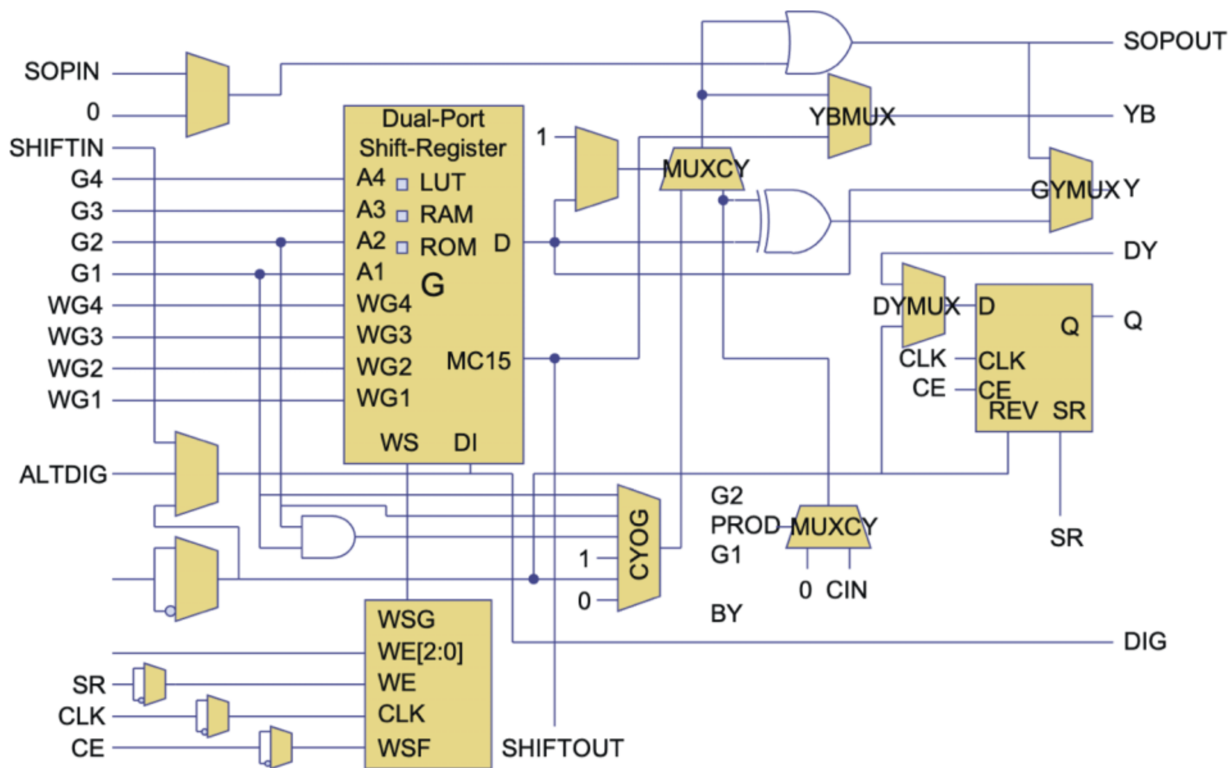

Figure 5. Block diagram of the Virtex II Pro cell architecture.

In summary, the FPGA is highly configurable, as we showed in this Technical Tidbit. FPGAs can provide designers with a wide range of programmable functionality for many different applications, such as telecommunications, consumer electronics, automotive, and military applications.

Ask the Experts

Q: What is the typical viscosity of a photoresist material?

A: The viscosities of photoresist materials range from about 10 to 120 cSt (centistokes). These materials are formulated for different layers on the wafers and for different applications, so the viscosities will vary.

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Spotlight: Design for Reliability

OVERVIEW

Semiconductor reliability is at a crossroads. In the past, reliability meant discovering, characterizing and modeling failure mechanisms and determining their impact on the reliability of the circuit. Today, reliability can involve tradeoffs between performance and reliability, assessing the impact of new materials, dealing with limited margins, etc. The product lifecycle for many components has become so short that there are limited opportunities to impact the overall reliability of the device, whether that be testing at the package level or even the wafer level. While reliability levels are at an all-time high level in the industry, rapid changes may quickly cause reliability to deteriorate. This requires that one put thought and effort into the reliability of a component upfront, during the design phase. The question is how to do this properly. Your company needs competent engineers and scientists to help solve these problems. ***Design for Reliability*** is a 1-day course that offers detailed instruction on a variety of subjects pertaining to designing in reliability. This course is designed for every manager, engineer, and technician concerned with reliability in the semiconductor field, designing semiconductor components, or supplying tools to the industry.

Participants learn to develop the skills to determine what failure mechanisms might occur, and how to develop models for them, understand their impact at the circuit, block, and IC level, and minimize their impact in the product.

1. **Fundamentals of Reliability Physics and Accelerated Testing.** Participants learn the fundamentals of various failure mechanisms and the testing used to accelerate those mechanisms.
2. **Design-In Reliability Issues.** Participants learn how the major failure mechanisms manifest themselves at the circuit and chip level. These include: time-dependent dielectric breakdown, hot carrier degradation, electromigration, stress-induced voiding, moisture, corrosion, contamination, thermomechanical effects, etc. They learn the process for converting test structure results into circuit level behaviors.
3. **Mission Profiles.** Participants learn the conversion of transient use-conditions into static equivalents for Design Rule generation and verification.

COURSE OBJECTIVES

1. The seminar will provide participants with an in-depth understanding of the failure mechanisms, test structures, equipment, and testing methods used to achieve today's high reliability components.
2. Participants will be able to identify basic test structures and how they are used to help quantify reliability on semiconductor devices.
3. Participants will be able to interpret test structure data and make inferences from that data.
4. The seminar will identify the major failure mechanisms, explain how they are observed, and how they are modeled at the circuit level.
5. Participants will learn to convert dynamic condition test data into a static model that can be used in the design environment for design rule checking and layout.
6. Participants will be able to knowledgeably implement screens that are appropriate to assure the reliability of a component.
7. Participants will be able to identify appropriate software tools to purchase when starting or expanding their design operations.

INSTRUCTIONAL STRATEGY

By using a combination of instruction by lecture, problem solving and question/answer sessions, participants will learn practical approaches to the failure analysis process. From the very first moments of the seminar until the last sentence of the training, the driving instructional factor is **application**. We use instructors who are internationally recognized experts in their fields that have years of experience (both current and relevant) in this field. The handbook offers hundreds of pages of additional reference material the participants can use back at their daily activities.

COURSE OUTLINE

(Lecture Time 8 Hours)

1. Device-Parameter Degradation
2. Degradation Modeling
3. Time-to-Failure Modeling
4. Time-to-Failure Statistics
    a. Normal
    b. LogNormal
    c. Exponential
    d. Weibull
5. Accelerated Degradation
6. Acceleration Factor
    a. Arrhenius
    b. Eyring (Black's Model, Peck's Model, others)
    c. Power Law (Coffin-Manson)
7. Six-Sigma Approach to Designs
8. Design-In Reliability Issues
    a. Electromigration
    b. Stress Migration
    c. Time-Dependent Dielectric Breakdown
    d. Hot Carrier Injection
    e. Negative Bias Temperature Instability
    f. Plasma Damage Issues
    g. Thermal Cycling Issues
    h. Energy Density Issues

9. Mission Profiles
   a. Understanding Product Mission Profiles
   b. Conversion of Dynamic Voltage Conditions into Static Equivalents for Design Rule Generation/Verification
   c. Conversion of Dynamic Power/Temperature Conditions into Static Equivalents for Design Rule Generation/Verification

You may want to stress some aspects more than others or conduct a simple one-day overview course. Many of our clients seek ongoing just-in-time training that builds in-depth, advanced levels of reliability expertise. We'll work with you to determine the best course of action and create a statement of work that emulates the very best practices of semiconductor reliability analysis.

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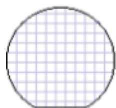

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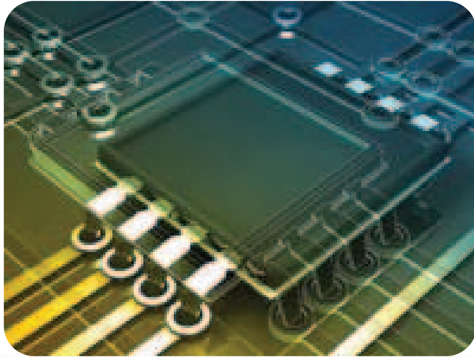

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Upcoming Webinars

(Click on each item for details)

Failure and Yield Analysis WEBINAR
4 sessions of 4 hours each
US: April 4 – 7, 2022 (Mon – Thur),
7:00 A.M. – 11:00 A.M. PST,
1:00 P.M. – 5:00 P.M. CET