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InfoTracks

Semitracks Monthly Newsletter

Low-K Materials Properties Part 1

By Christopher Henderson, continued from last month

Let's move on to the second set of materials properties: the mechanical properties. The materials properties become very important during packaging. Dicing, wirebonding, and flip chip mounting all mechanically stress the chip (see Figure 7, next page).

To measure the modulus or the strength of the material, researchers calculate stress-strain curves (see Figure 7, next page). They pull a sample of the material as shown here *(a),* measure the change in length, and measure the stress as a function of strain. Below some value, a material can be pulled and it will return to its original shape or length without any permanent deformation. If one continues to pull the material beyond its yield strength, it will permanently deform; it will not go back to its original shape. If one continues to pull the material, it will eventually fail and fracture. The slope of the stress-strain curve is the Young's modulus, which is basically the strength of the material. If we look at the stress-strain curve for different materials, we see that there are brittle materials, which include ceramics, and oxide-based low-k materials. A brittle material has a very high slope or stress to strain ratio, or a high Young's modulus or mechanical strength *(b).* The plastic deformation region is very small. Basically, the sample breaks before significant plastic deformation occurs. For a material like copper, we see a stress-strain curve that looks like this *(c).* There is a large region of plastic behavior where the material is permanently deformed but does not break. Instead it stretches as the strain is increased. Eventually, under some

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Figure 7. Stress-strain curves.

level of strain, the material will fracture. A third type of behavior would be mostly elastic, like one would observe with a polymer *(d).* There is no permanent change in shape over a large range of strain, but at some level it will deform and eventually fracture.

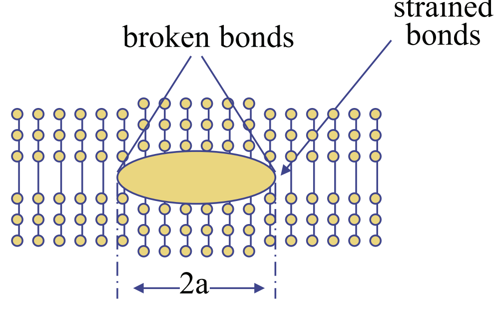


Figure 8. Diagram explaining fracture at the atomic level.

The fracture properties are very important for the brittle low-k materials, such as the carbon-doped glasses. A crack will grow if the elastic strain energy exceeds the surface energy. There are lower critical stress values for materials with low Young's modulus and low strain energy release rates. For non-brittle materials, there is also plastic deformation energy associated with crack propagation.

tensile stress; Young's modulus; Surface energy / area

$$\text{Crack energy} = W = -\sigma^2 \pi a^2 / E + 4a\gamma_s$$

elastic strain energy; surface energy

Crack growth condition: $dW/dA = 0$

Critical stress required for crack propagation in a brittle material

$$\sigma_c(\pi a)^{1/2} = (2E\gamma_s)^{1/2}$$

Critical stress intensity factor (fracture toughness)

$$\sigma_c(\pi a)^{1/2} = [E\, 2(\gamma_s + \gamma_p)]^{1/2}$$

Critical strain energy release rate

Figure 9. Basic strain energy equations.

The fracture is determined by the strain energy. The strain energy tries to propagate the crack to relieve the strain in the bonds. The increase in strain is balanced by the increase in surface energy. This determines whether or not the crack will grow. The strain energy is a function of the tensile stress and the Young's modulus of the material. The critical stress required for crack propagation in a brittle material like a carbon-doped oxide is sigma sub c times pi a to the one-half power. This is also equal to the critical strain energy release rate. For a brittle material, there is only one component: gamma sub s. For a plastic material, there is also a plastic energy release rate: gamma sub p.

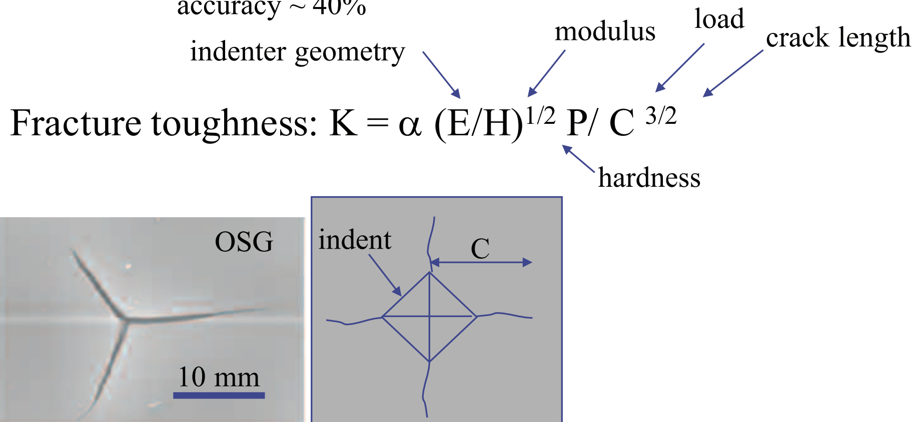
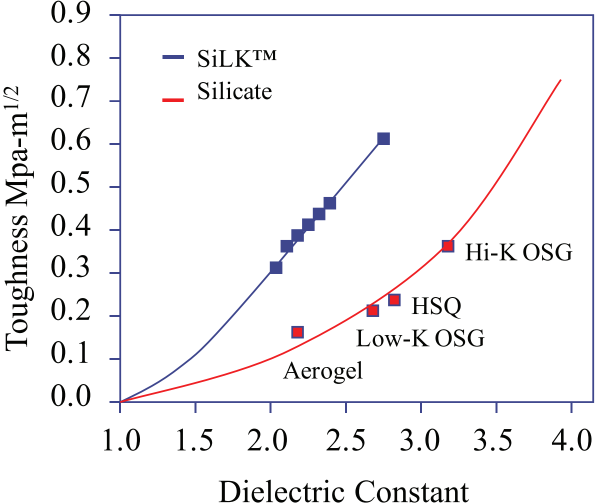


Figure 10. Indentation test for fracture toughness.

The important parameter is the fracture toughness. The fracture toughness is typically measured using a technique called indentation. The fracture toughness K is a function of the indenter geometry, the Young's modulus of the material, its hardness, the load, and the crack length. One can indent the surface with a particular load and measure the crack length and use the data to determine the fracture toughness. This technique is also referred to as nano-indentation.



Material	Toughness (Mpa $m^{1/2}$)	Reference
Si	**0.7**	**Harding et. al.**
SiO_2	**0.75**	**Harding et. al.**
SiC	**4.1**	**Harding et. al.**
Si_3N_4	**4.7**	**Harding et. al.**
SiLK	**0.62**	**Shaffer et. al.**
OSG	**0.05**	**Vella et. al.**

Figure 11. Fracture toughness results for dielectrics.

This graph and table in Figure 11 show how the fracture toughness varies with dielectric constant. In general, just as the modulus goes down with the dielectric constant, the fracture toughness also decreases. Therefore, the materials are more likely to crack as we lower the dielectric constant. The table also compares fracture toughness for oxide-based materials and the Dow Chemical SiLK material, which is a polymer. It shows that the polymer materials for a given dielectric constant have a much higher fracture toughness than the oxide-based materials. This is the one advantage of the polymer-based materials compared to the oxide-based materials: they have a higher fracture toughness.

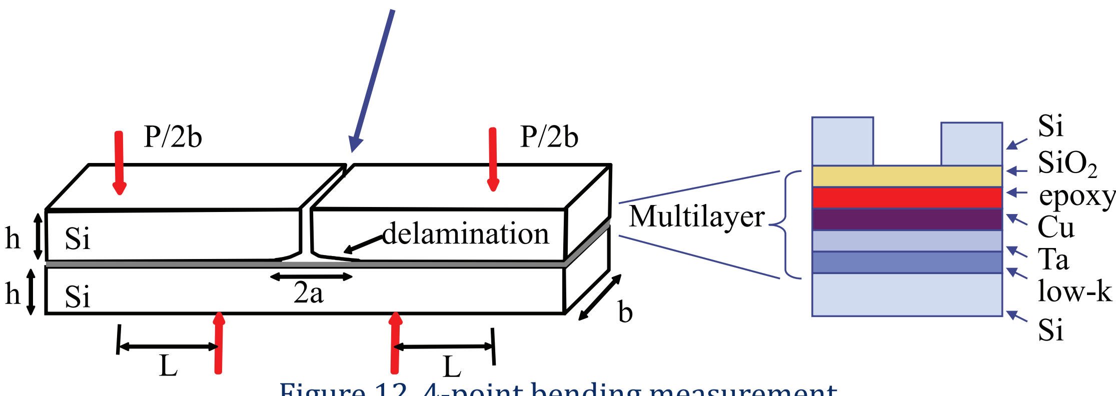


Figure 12. 4-point bending measurement.

Not only can fractures occur due to pressure on a local point, but they can also occur due to bending or warping. The most common method for calculating fracture due to bending or warping is the 4-point

bending measurement. In this technique a pre-crack is initiated in silicon, followed by 4-point bending. The crack will propagate to the weakest interface, and then along that same interface.

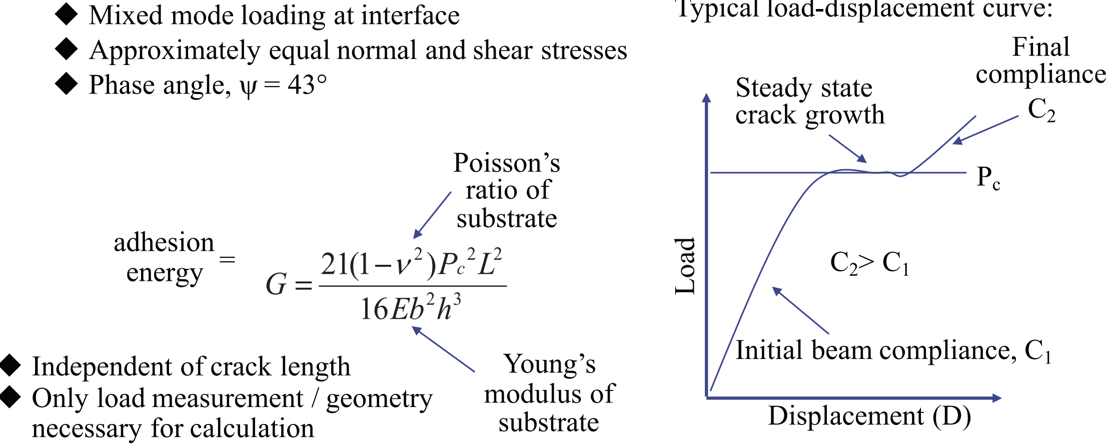
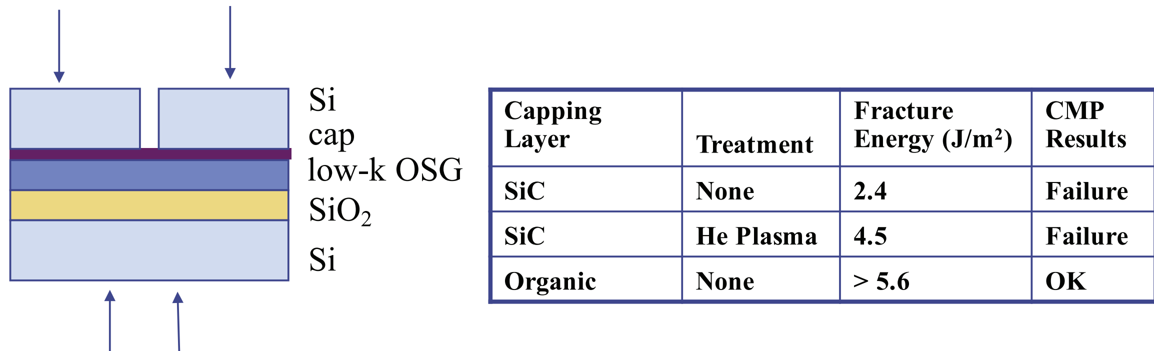


Figure 13. Typical load as function of displacement.

The graph on the right in Figure 13 shows a typical load as a function of displacement. Initially, there is a beam compliance where the load increases proportionally to the displacement. At a critical load, the crack begins to grow. The material then goes through a final compliance at higher displacement values. Crack growth will be a function of adhesion energy. The adhesion energy G is given by the equation shown here, where nu is Poisson's ratio of the substrate and E is the Young's modulus of the substrate. The test is independent of crack length; one only needs the load measurement and geometry to calculate the fracture toughness in a 4-point bending measurement.



Capping Layer	Treatment	Fracture Energy (J/m²)	CMP Results
SiC	None	2.4	Failure
SiC	He Plasma	4.5	Failure
Organic	None	> 5.6	OK

Figure 14. Adhesion: effect of surface treatment.

One also must understand the adhesion of the low-k materials to other layers. In particular, one must understand the adhesion of the capping layer to the low-k material. The adhesion is affected by the type of plasma treatment that is performed. Typically, an adhesion failure will occur between the cap and the low-k material. One method for improving adhesion is a helium plasma treatment before the capping layer is deposited. The OSG layer is formed first. It is plasma treated, and then the capping layer is deposited. The helium plasma apparently reacts with the silicon carbide to form more favorable bonding

between the materials. This only works for certain materials though. For example, performing an oxygen treatment on an OSG layer before deposition of an organic layer degrades the adhesion qualities.

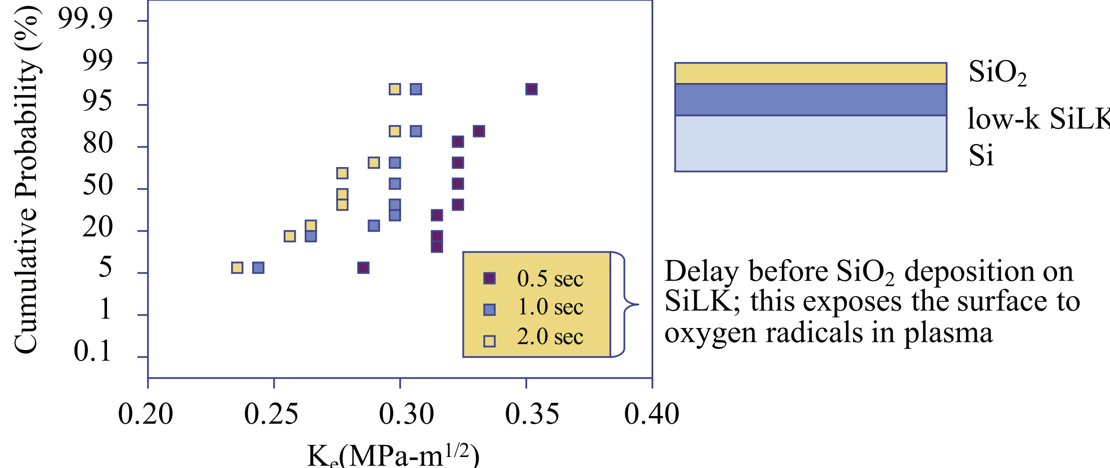


Figure 15. Effect of surface treatment on adhesion properties.

This graph in Figure 15 shows that an increase in delay before depositing the silicon dioxide on the SiLK polymer will lower the adhesion properties. The delay allows the surface of the SiLK material to be exposed to oxygen radicals in the plasma.

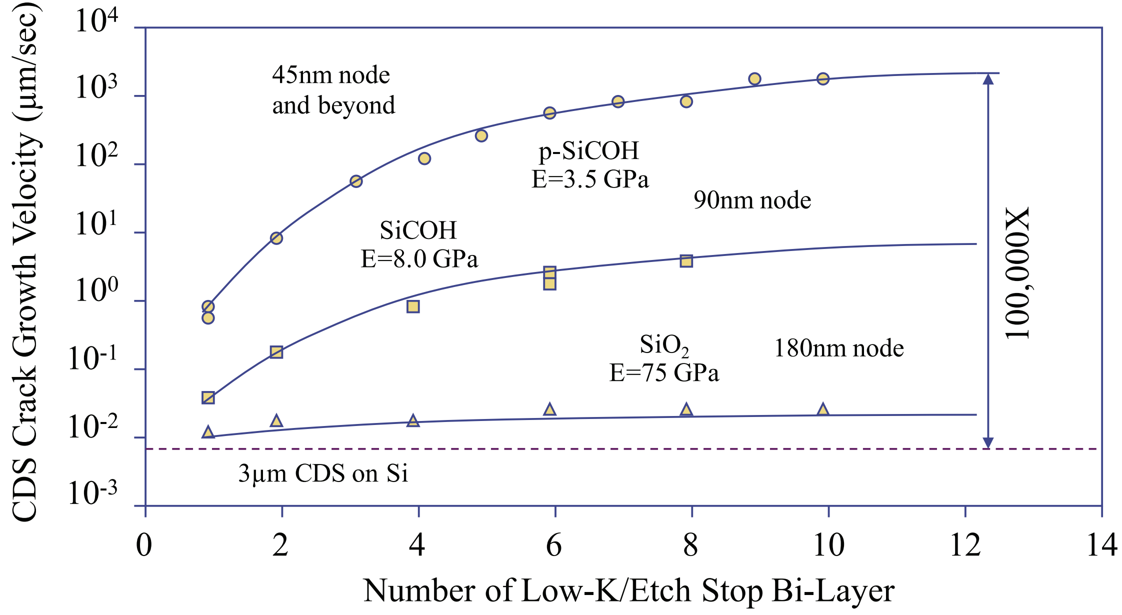


Figure 16. Crack growth: effect of multilayers.

The graph in Figure 16 shows the problems the industry is encountering when trying to build multilayer dielectric stacks. The graph shows the crack grow velocity—or the ease in growing cracks—as a function of the number of metal layers in the structure. There are data for three types of materials: SiO_2,

SiCOH, and porous SiCOH. As the industry moves toward more and more brittle materials, it is easier to form cracks as measured by the crack growth velocity. Also, as the industry adds more metal layers it is easier to form cracks. Unfortunately the trend is toward more metal layers and lower dielectric constant films, which introduces numerous problems during packaging.

The main message is that all of the mechanical properties get worse as one reduces the dielectric constant. The hardness of the materials decreases with decreasing dielectric constant. The fracture toughness decreases with decreasing dielectric constant. Adhesion depends on bonding at the interface, and can be influenced by plasma treatments and humidity. One can use a technique called nano-indentation to measure the hardness, modulus, toughness and adhesion. It is a popular technique because it is fast; however, one needs thick films to minimize substrate effects.

In conclusion, we have discussed the materials properties of several low-k dielectrics in use as well as several potential low-k dielectrics. As the dielectric constants get lower, there is an increasing number of issues with their thermal properties, mechanical strength, and chemical stability. These materials each have strengths and weaknesses. Therefore, one may be better suited to a particular application than another. There is definitely not a “one size fits all” solution for current and future technology nodes.

Resources

Figure 1: S.M. Sze, Physics of Semiconductor Devices, 1981, chap. 7; S. Scarpula et al., Int. Rel. Phys. Symp., 1999, p. 128

Figures 2,3: S.M. Sze, Physics of Semiconductor Devices, 1981, chap. 7; S. Habermehl, C. Carmignani, Appl. Phys. Lett., 80, 261 (2002)

Figure 4: S.M. Sze, Physics of Semiconductor Devices, 1981, chap. 5; K.Y. Yiang et al., IRPS Proc., 2004

Figure 6: S.M. Sze, Physics of Semiconductor Devices, 1981, chap. 7; S. Kim et al., Int. Rel. Phys. Symp., 1999, p.277

Figure 7: W.D. Callister, Materials Science and Engineering, 5th ed., 2000, chap. 6

Figures 8,9: C.R. Barrett et al., The Principles of Engineering Materials, 1973, chap. 8; W.D. Callister, Materials Science and Engineering, 5th ed., 2000, chap. 6

Figures 10,11: D.S Harding et al., MRS Proc., vol. 356, 1995, p. 663; J.B. Vella et al., MRS Proc., vol. 716, 2002, p. B12.13; E. Shaffer et al., MRS Proc., vol. 612, 2000

Figures 12,13: R.H. Dauskardt et al., Eng. Frac. Mech., vol. 61, 141 (1998)

Figure 14: F. Iacopi et al., MRS Proc., vol. 795, 2004, p. U4.3

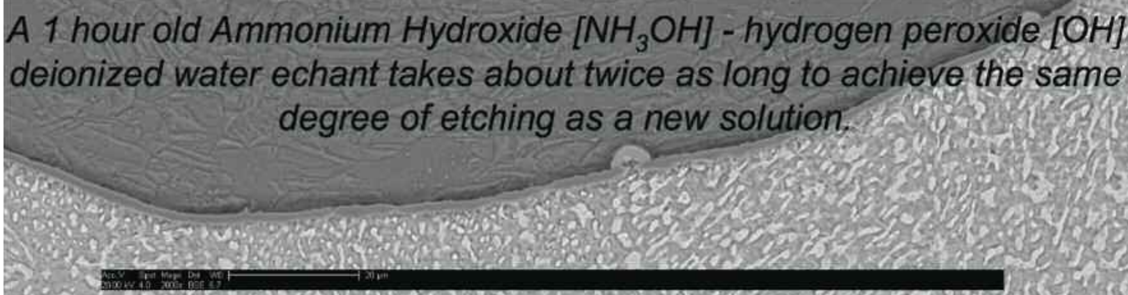
Figure 15: J. Song et al., IITC Proc., 2000, p. 55

Figure 16: T.Y. Tsui et al., MRS Proc., vol. 863, 2005, p. B4.1

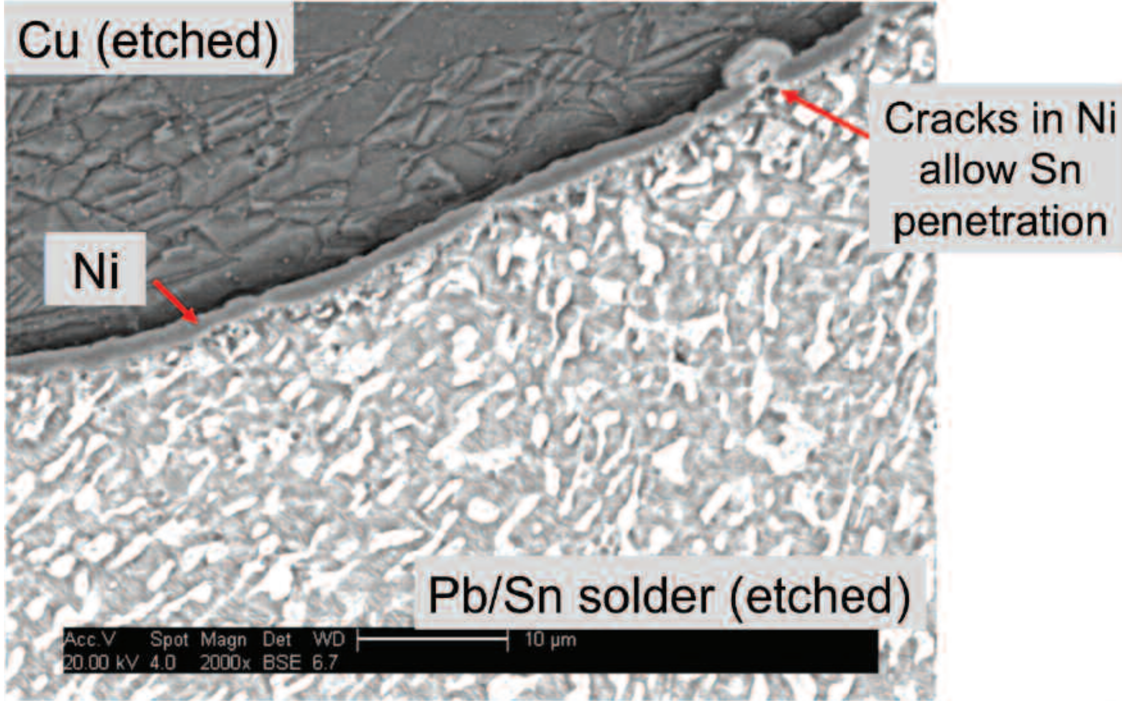
Technical Tidbit

Etching A Cross-Sectioned Surface

Etching a cross-sectioned surface can be a useful technique for highlighting features and making them easier to identify. With this technique, the chemical etchants can be applied by swabbing or dipping. The typical dip times are 15 to 45 seconds, followed by immediate immersion in a small beaker of deionized water to stop the etching. One can then dry the sample with compressed nitrogen or air. We should note that some etchants react immediately after mixing and some etchants will lose their strength over time.



Here is a high magnification SEM image showing the interface between the copper metal and the lead-tin solder. Note the nickel barrier on the copper. This particular sample shows cracks in the nickel barrier, allowing tin penetration into the copper layer.



Ask the Experts

Q: Why do some manufacturers add strontium to their capacitors?

A: Strontium is sometimes added to a discrete capacitor to give it better temperature characteristics. The strontium can help maintain a more fixed capacitance over a temperature range.

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Spotlight: CMOS, BiCMOS, and Bipolar Process Integration

OVERVIEW

Semiconductor and integrated circuit developments continue to proceed at an incredible pace. For example, today's mixed-signal chips perform a wide range of applications unheard of a few years ago, including wireless applications, high speed communications, and signal processing. These challenges have been accomplished because of the integrated circuit industry's ability to track something known as Moore's Law. A corollary to Moore's Law is that frequencies on mixed-signal devices continue to rise. This has been accomplished by making devices smaller and smaller. The question looming in everyone's mind is "How far into the future can this continue?" ***CMOS, BiCMOS, and Bipolar Process Integration*** is a 3-day course that offers detailed instruction on the physics behind the operation of a modern mixed-signal integrated circuit, and the processing technologies required to make them. We place special emphasis on current issues related to designing and manufacturing the next generation devices. This course is a must for every manager, engineer and technician working in the semiconductor industry, using semiconductor components or supplying tools to the industry.

By focusing on the fundamentals of transistor operation and performance, participants will learn why advances in the industry are occurring along certain lines and not others. Our instructors work hard to explain how semiconductor devices work without delving too heavily into the complex physics and mathematical expressions that normally accompany this discipline.

Participants learn basic but powerful aspects about the semiconductor industry. This skill-building series is divided into three segments:

1. **Basic Device Operation.** Participants learn the fundamentals of transistor operation. They learn why BiCMOS devices dominate the mixed-signal industry today.
2. **Fabrication Technologies.** Participants learn the fundamental manufacturing technologies that are used to make modern integrated circuits. They learn the typical CMOS, Bipolar and BiCMOS process flows used in integrated circuit fabrication.
3. **Current Issues in Process Integration.** Participants learn how device operation is increasingly constrained by three parameters. They also learn about the impact of using new materials in the fabrication process and how those materials may create problems for the manufacturers in the future..
4. **An Overview of Issues Related to Process Integration.** Participants learn about the image of new materials, yield, reliability and scaling on technology and process integration. They receive an overview of the major reliability mechanisms that affect silicon ICs today.

COURSE OBJECTIVES

1. The seminar will provide participants with an in-depth understanding of the semiconductor industry and its technical issues.
2. Participants will understand the basic concepts behind transistor operation and performance.
3. The seminar will identify the key issues related to the continued growth of the semiconductor industry.
4. The seminar offers a wide variety of sample problems that participants work to help them gain knowledge of the fundamentals of device operation and manufacturing.

5. Participants will be able to identify basic and advanced technology features on semiconductor devices. This includes features like silicon-germanium, emitter islands, copper, and low-k dielectrics.
6. Participants will understand how reliability, power consumption and device performance are interrelated.
7. Participants will be able to make decisions about how to construct and evaluate new CMOS, BiCMOS, and bipolar technologies.

INSTRUCTIONAL STRATEGY

By using a combination of instruction by lecture, classroom exercises, and question/answer sessions, participants will learn practical information on semiconductor devices and the operation of this industry. From the very first moments of the seminar until the last sentence of the training, the driving instructional factor is **application**. We use instructors who are internationally recognized experts in their fields that have years of experience (both current and relevant) in this field. The handbook offers hundreds of pages of additional reference material the participants can use back at their daily activities.

COURSE OUTLINE

Day 1

1. Introduction
2. Basic Semiconductor Concepts
   a. Diffusion/Drift
   b. PN Junction Diodes
   c. Bipolar Junction Transistor
   d. MOS Transistor
   e. Additional Concepts
      i. Avalanche Breakdown
      ii. Zener Breakdown
      iii. Tunneling
      iv. Schottky Barriers
3. General Scaling Issues
   a. Constant Field Scaling/Constant Voltage Scaling
   b. Process Integration Issues
      i. Transistors (Ion vs Ioff, Mobility Enhancement, short channel effects, etc.)
      ii. Interconnect (RC delay, power dissipation, etc.)
   c. Limitations to Scaling

Day 2

4. Conventional CMOS
    a. Well/Substrate Engineering
    b. Device Isolation
    c. Gate Stack
    d. Contacts/Silicide
    e. Scaling Issues
    f. Basic CMOS Flow Presentation
5. Conventional BiCMOS
    a. Bipolar Transistor Fundamentals
    b. BiCMOS Process Overview
    c. Scaling and Limitations
    d. Basic BiCMOS Flow Presentation
6. Bipolar Enhancement Techniques
    a. SiGe
    b. SiGe:C
7. Power Technologies
    a. LDMOS
    b. DECMOS
    c. BCD
8. Additional Analog Circuit Elements
    a. Resistors
    b. Capacitors
    c. JFETs

Day 3

9. Interconnects
    a. Aluminum Interconnects, Issues
    b. Copper Interconnects, Issues
    c. Low-k Dielectrics
10. CMOS/Bipolar/BiCMOS Reliability Considerations
    a. Electrostatic Discharge
    b. Electromigration and Stress Migration
    c. Soft Errors, Plasma Damage
    d. Dielectric Reliability
    e. Bias Temperature Instabilities
    f. Hot Carrier Reliability
    g. Burn-In
11. Yield Considerations
    a. Yield Detractors
    b. Models
    c. Monitors
12. Conclusion/Wrap Up

You may want to stress some aspects more than others or conduct a simple one-day overview course. Many of our clients seek ongoing just-in-time training that builds in-depth, advanced levels of reliability expertise. We'll work with you to determine the best course of action and create a statement of work that emulates the very best practices of semiconductor reliability analysis.

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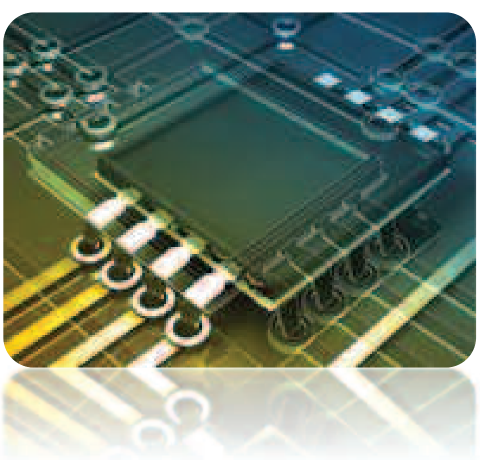

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Upcoming Courses

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Semiconductor Reliability / Product Qualification
March 26 – 29, 2018 (Mon – Thur)
Portland, Oregon, USA

Failure and Yield Analysis
April 9 – 12, 2018 (Mon – Thur)
Munich, Germany

Wafer Fab Processing
April 9 – 12, 2018 (Mon – Thur)
Munich, Germany

Semiconductor Reliability / Product Qualification
April 16 – 19, 2018 (Mon – Thur)
Munich, Germany

CMOS, BiCMOS and Bipolar Process Integration
September 10 – 12, 2018 (Mon – Tue)
San Jose, California, USA