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InfoTracks

Semitracks Monthly Newsletter

Thermal Processing, Issues and Effects, Part 2

By Christopher Henderson

There are three major factors that affect the availability of the oxidizing species. They include diffusivity, solubility and pressure. In terms of diffusivity, oxygen diffuses much faster through silicon dioxide than water molecules. The water molecule, with its angled shape, occupies more volume than the oxygen molecule. This makes it more difficult for the water molecule to move through the silicon dioxide structure. On the other hand, water is approximately 600 times more soluble in silicon dioxide than in oxygen. Silicon dioxide readily traps and holds water, while oxygen tends to diffuse away quickly. Pressure is the third factor affecting oxidation. Increasing pressure from the outside environment increases the concentration of the species in the reaction zone.

In this Issue:

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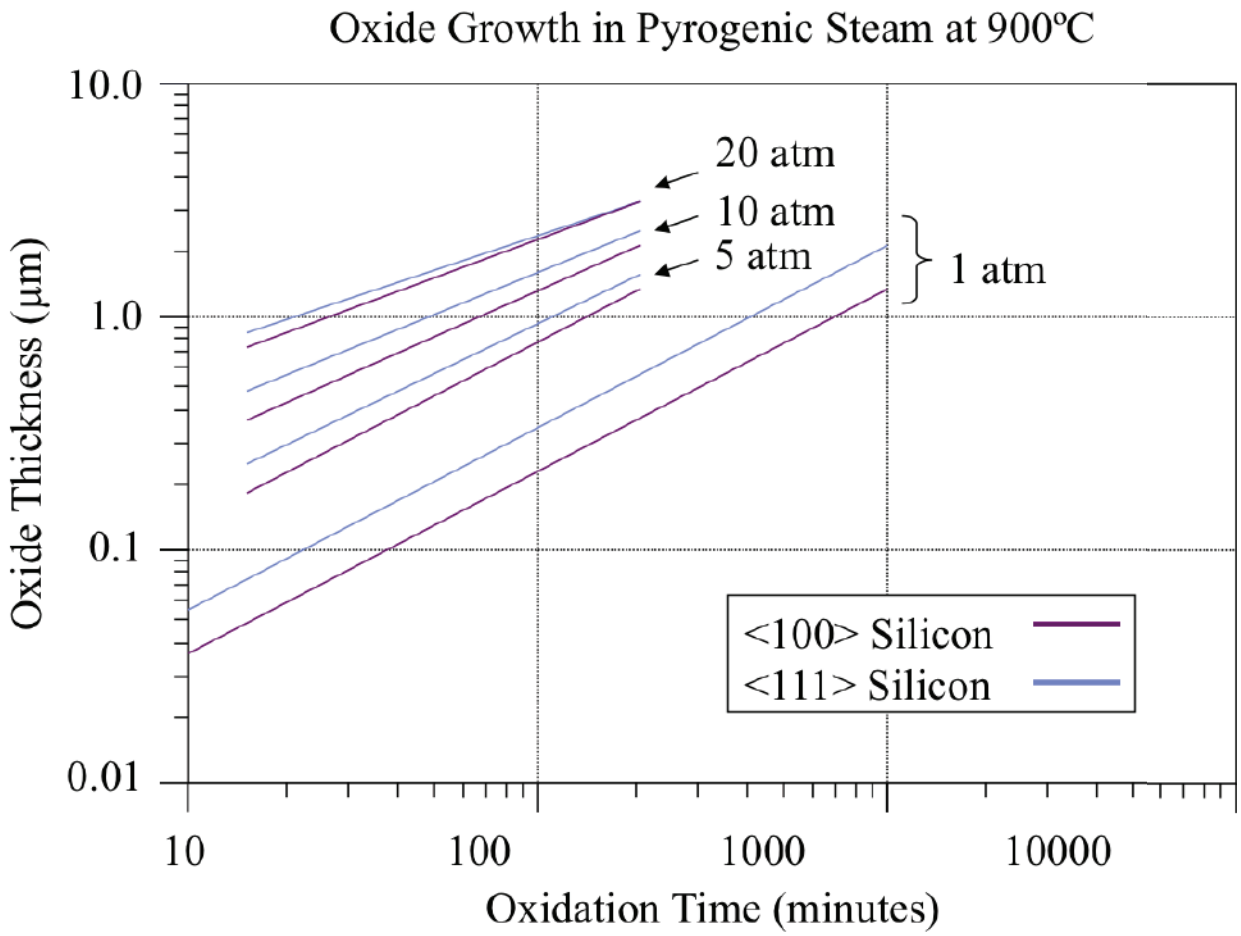
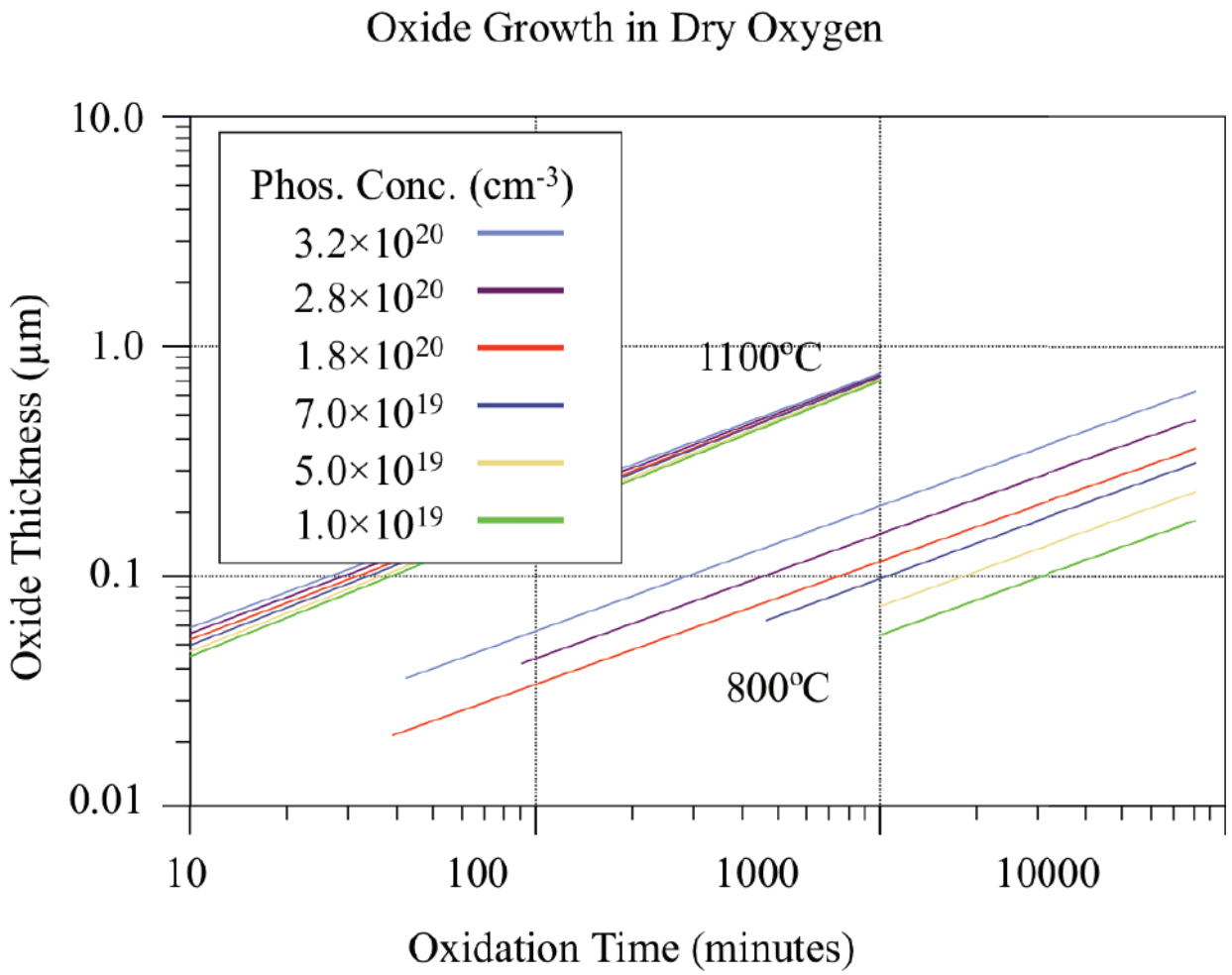
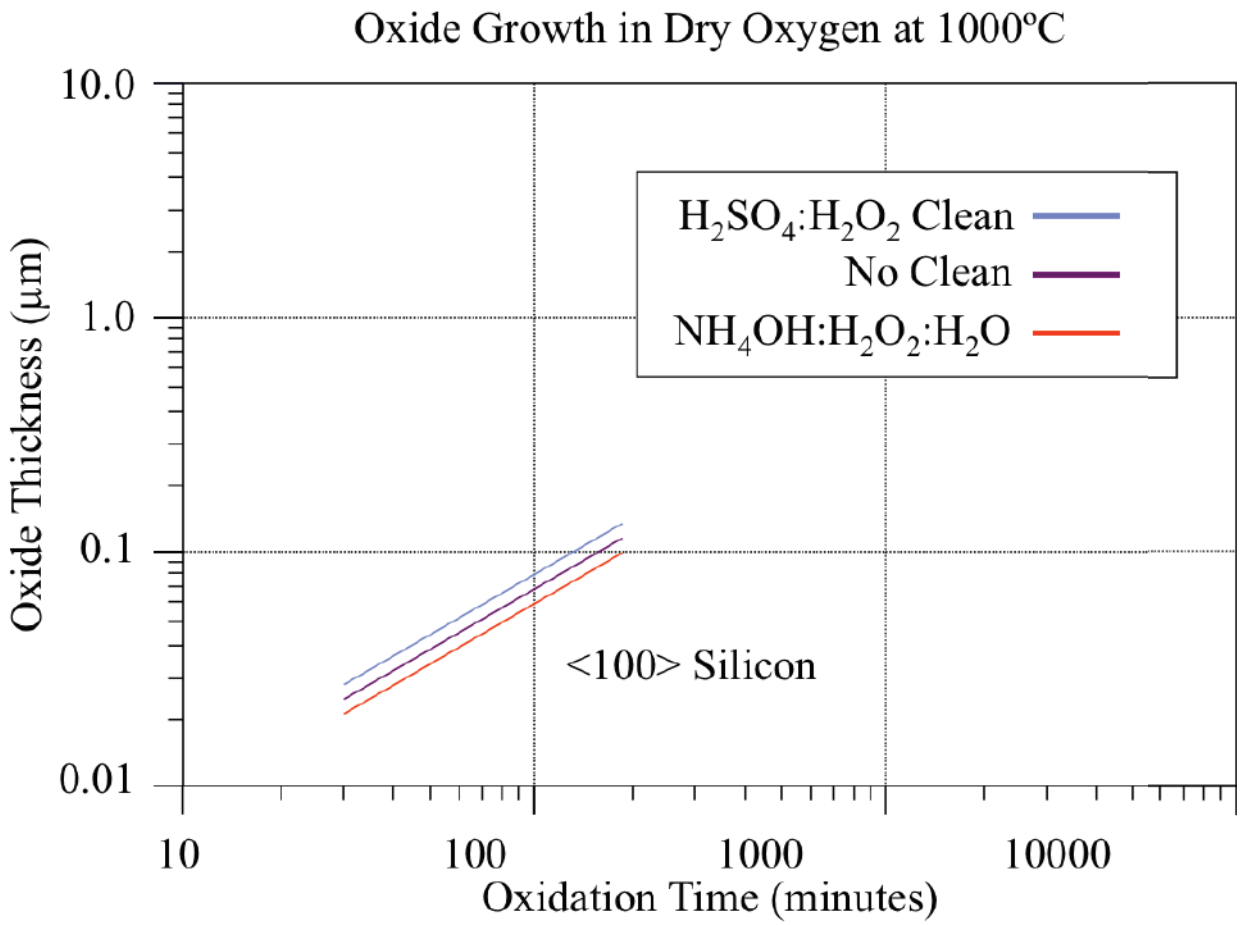


This graph shows the effects of pressure on oxide growth in pyrogenic steam. The graph shows the oxide thickness as a function of oxidation time for several different pressures. Notice that the oxide growth rate increases as the ambient pressure is increased.

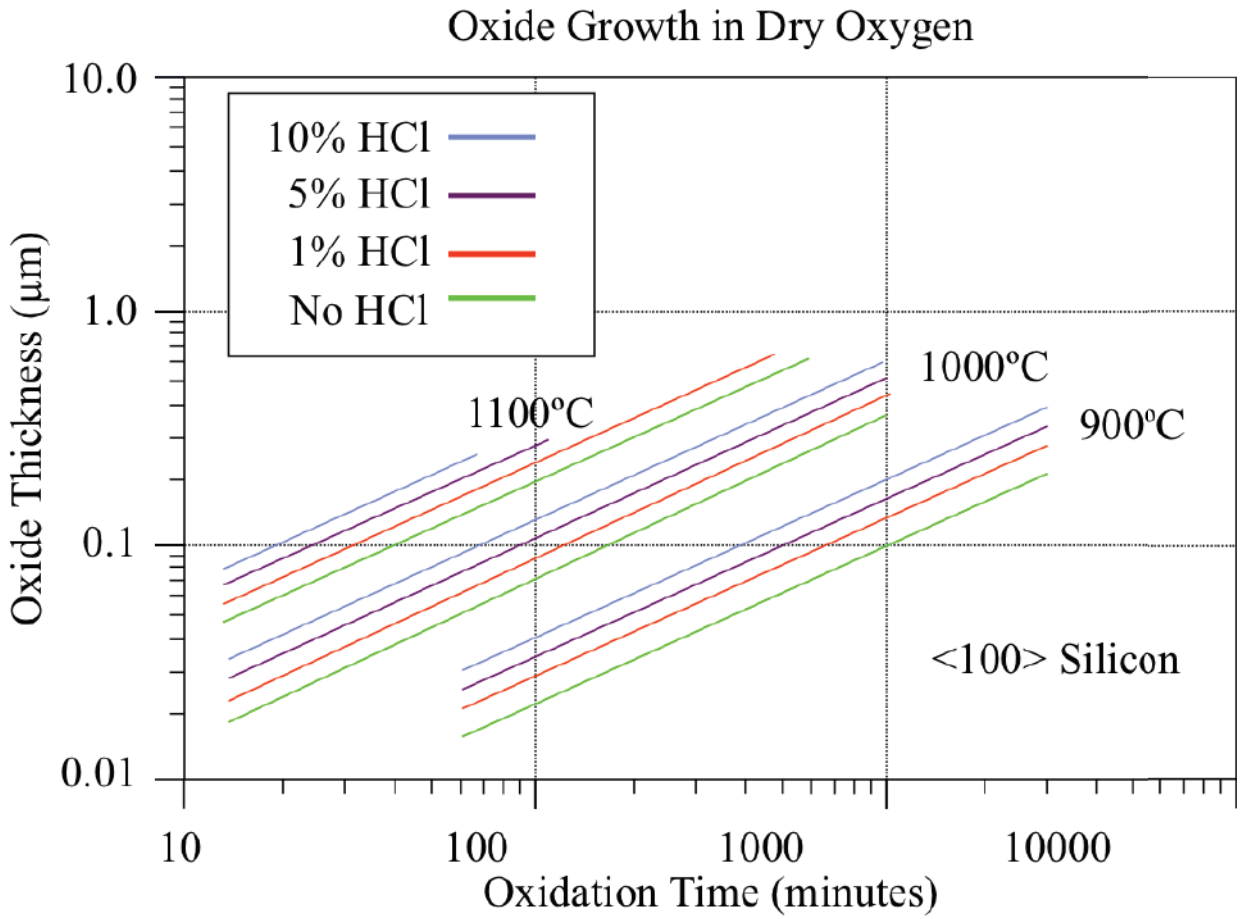
There are several factors that change the surface potential of the silicon surface. These are crystal orientation, silicon doping concentration, and surface treatment. The <111> plane oxidizes the fastest while the <100> plane oxidizes the slowest. The bonds coming out of the <111> plane more easily accept oxygen. Higher surface doping concentrations give higher oxidation rates. The silicon to silicon bonds are compressed and/or stretched by substitutional impurities. These bonds are more easily broken to accept oxygen than silicon to silicon bonds in an area where the lattice is free from impurities. Finally, surface treatments such as a hydrochloric acid treatment can increase the growth rate. The acid oxidizes the surface, allowing oxygen to bond more easily.



This graph shows the doping effects on oxidation. Notice that as the concentration of phosphorus increases, the growth rate of the oxide increases. The effect is more pronounced at lower temperatures. At higher temperatures, one can see that the oxidation lines are closely packed together.



This graph shows the effects of two different pre-treatments, and no pre-treatment of the silicon surface. The sulfuric acid – hydrogen peroxide clean oxidizes the surface, allowing faster oxide growth, while the ammonium hydroxide – hydrogen peroxide – water clean makes the surface more alkaline, reducing the growth rate.

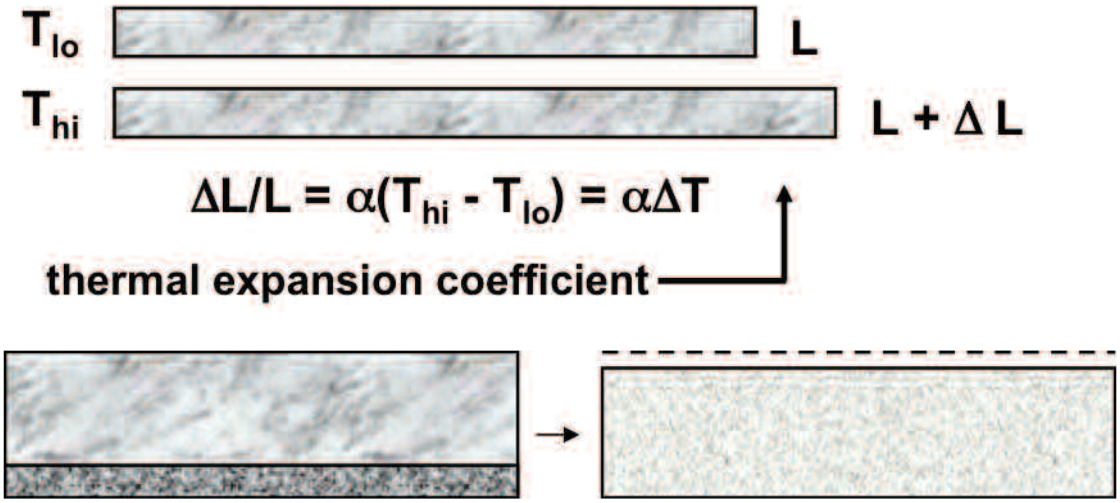


This graph shows the effects of oxide growth when the silicon surface is exposed to hydrochloric acid. Researchers have studied the effects of chlorine gas on silicon dioxide growth for a number of years, since chlorine can reduce fixed and mobile charge in the silicon dioxide, increase the lifetime of the minority carriers, and reduce the density of oxidation-induced stacking faults in the silicon below. Chlorine can also cause the oxide reaction rate to increase, but the reasons for this are not well understood. Researchers have also observed the buildup of chlorine at the silicon/silicon dioxide interface.

Technical Tidbit

Stress Voiding Prerequisites

There are three prerequisites for stress voiding: a driving force, a nucleation point—or a mechanism to initiate the growth, and a means to grow. The driving force is provided by the tensile mechanical stress that is built into the interconnect after it is deposited, cooled, and confined by the dielectrics that surround it and prevent it from relaxing. A second method that introduces stress into the system is the intermetallic reaction that can occur in aluminum systems with titanium-based shunt layers. We'll discuss both of these in more detail in a few slides. The way to start is normally provided by some type of defect. This could be as simple as a small cavity on the side of an interconnect. The means to grow is provided by nature in the form of diffusion, or mass transport away from the void along the path of least resistance, normally a grain boundary.



Let's discuss the two sources of mechanical stress in more detail. The first stress mechanism is brought on by the mismatch in coefficients of thermal expansion between the interconnect and the dielectrics that surround it. Aluminum has a much higher coefficient of thermal expansion than silicon dioxide. As the interconnect and surrounding dielectrics cool after the deposition process, a stress is induced in the line. The higher the processing temperature, the more stress is placed on the interconnect at normal temperatures. The second stress mechanism is brought on by the intermetallic reaction between aluminum and titanium. Sometimes, circuit manufacturers will react—or sinter—the aluminum with the titanium shunt layer to prevent it from delaminating and to insure a low resistance connection between the two layers. The resulting intermetallic product takes up less room than the two metals separately. If this system is again confined by the dielectrics, this places a stress in the system.

Ask the Experts

Q: I have a HAST Failure in a package with copper bond wires and a silver plated lead frame. Is there any way I can eliminate this type of failure?

A: This is a difficult situation, because you are working with two metals that exhibit galvanic corrosion characteristics. The best solution is to change out one or both of the metal surfaces with something that is less susceptible to corrosion. For copper wires, one could switch to Palladium-Coated Copper (PCC) wire, and for the silver-plated leadframe, one could switch to a material like Nickel-Palladium-Gold (NiPdAu) as a coating on the leadframe.

Spotlight: Wafer Fab Processing

OVERVIEW

Semiconductor and integrated circuit developments continue to proceed at an incredible pace. The industry as a whole has gotten to this point of incredible complexity through the process of countless breakthroughs and developments in wafer fab processing. Today's wafer fab contains some of the most complex and intricate procedures ever developed by mankind. ***Wafer Fab Processing*** is a one-day course that offers an overview look into the semiconductor manufacturing process, and the individual processing technologies required to make them. We place special emphasis on the basics surrounding each technique, and we summarize the current issues related to manufacturing the next generation devices. This course is a must for every manager, engineer and technician working in the semiconductor industry, using semiconductor components or supplying tools to the industry.

By focusing on the basics of each processing step and the issues surrounding them, participants will learn why certain techniques are preferred over others. Our instructors work hard to explain how semiconductor processing works without delving heavily into the complex physics and mathematical expressions that normally accompany this discipline.

Participants learn basic but powerful aspects about the semiconductor industry. This skill-building series is divided into three segments:

1. **Basic Processing Steps.** Each processing step addresses a specific need in IC creation. Participants learn the fundamentals of each processing step and why they are used in the industry today.
2. **The Evolution of Each Processing Step.** It is important to understand how wafer fab processing came to the point where it is today. Participants learn how each technique has evolved for use in previous and current generation ICs.
3. **Current Issues in Wafer Fab Processing.** Participants learn how many processing steps are increasingly constrained by physics and materials science. They also learn about the impact of using new materials in the fabrication process and how those materials may create problems for the manufacturers in the future.

COURSE OBJECTIVES

1. The seminar will provide participants with an overview of the semiconductor industry and its technical issues.
2. Participants will understand the basic concepts behind the fundamental wafer fab processing steps.
3. The seminar will identify the key issues related to each of the processing techniques and their impact on the continued scaling of the semiconductor industry.
4. Participants will be able to identify the basic features and principles associated with each major processing step. These include processes like chemical vapor deposition, ion implantation, lithography, and etching.
5. Participants will understand how processing, reliability, power consumption and device performance are interrelated.
6. Participants will be able to make decisions about how to construct and evaluate processing steps for CMOS, BiCMOS, and bipolar technologies.

INSTRUCTIONAL STRATEGY

By using a combination of instruction by lecture, classroom exercises, and question/answer sessions, participants will learn practical information on semiconductor processing and the operation of this industry. From the very first moments of the seminar until the last sentence of the training, the driving instructional factor is **application**. We use instructors who are internationally recognized experts in their fields that have years of experience (both current and relevant) in this field. The accompanying textbook offers hundreds of pages of additional reference material participants can use back at their daily activities.

COURSE OUTLINE

1. Raw Silicon Wafers
2. Ion Implantation
3. Thermal Processing
4. Contamination Monitoring and Control
5. Wafer Cleaning and Surface Preparation
6. Chemical Vapor Deposition
7. Physical Vapor Deposition
8. Lithography
9. Etch
10. Chemical Mechanical Polishing
11. Cu Interconnect and low-k Dielectrics
12. Leading Edge Technologies and Techniques
    a. ALD
    b. high-k gate and capacitor dielectrics
    c. metal gates
    d. SOI
    e. strained silicon
    f. plasma doping

For each of these modules, the following topics will be addressed:

1 fundamentals necessary for a basic understanding of the technique
2 its role(s) and importance in contemporary wafer fab processes
3 type of equipment used
4 challenges
5 trends

2015 IEEE International Reliability Physics Symposium

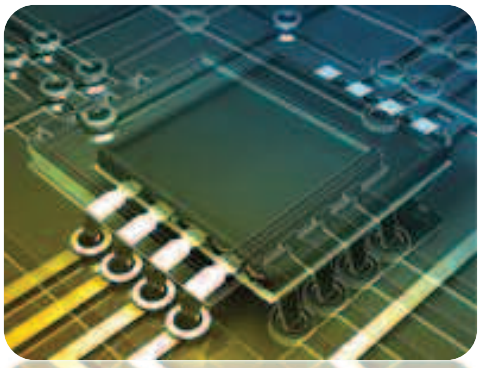
IEEE

April 19-23, 2015
Hyatt Regency Monterey Resort & Spa
Monterey, CA, USA

Registration is available at www.irps.org

Chris Henderson, IRPS Vice General Chair

Chris would be happy to meet with you and discuss any training needs you have. Contact him at henderson@semitracks.com during the symposium!



Feedback

If you have a suggestion or a comment regarding our courses, online training, discussion forums, or reference materials, or if you wish to suggest a new course or location, please call us at 1-505-858-0454 or Email us (info@semitracks.com).

To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered in the next newsletter, please contact Jeremy Henderson by Email (jeremy.henderson@semitracks.com).

We are always looking for ways to enhance our courses and educational materials.

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For more information on Semitracks online training or public courses, visit our web site!

http://www.semitracks.com

To post, read, or answer a question, visit our forums.
We look forward to hearing from you!

Upcoming Courses

(Click on each item for details)

Wafer Fab Processing
March 16 – 19, 2015 (Mon – Thur)
San Jose, California, USA

Failure and Yield Analysis
April 27 – 30, 2015 (Mon – Thur)
Munich, Germany

Semiconductor Reliability
May 4 – 6, 2015 (Mon – Wed)
Munich, Germany

EOS, ESD and How to Differentiate
May 7 – 8, 2015 (Thur – Fri)
Munich, Germany