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InfoTracks

Semitracks Monthly Newsletter

Analog Building Blocks

By Christopher Henderson

This month, we will continue our series of Feature Articles by discussing amplifiers. There are several types of amplifiers: single transistor amplifiers, Class A, Class B, and Class AB amplifiers. Single Transistor amplifiers can be used for very basic amplification needs. The Class A amplifier is popular because of its simplicity, but it is always conducting significant current and has a maximum efficiency of 25%. The Class B amplifier, also referred to as the push-pull configuration, is an improvement over the Class A amplifier in that it has zero power dissipation with zero input signal. Furthermore, its efficiency can be as high as 80%, but there is a distortion effect near the zero-input voltage in the bipolar Class B amplifier. Lastly, there is a Class AB amplifier, which reduces crossover distortion. We will go into more detail about Class B amplifiers and Class AB amplifiers in next month's Feature Article.

Let us begin with a few words about the single transistor amplifier. There are both passive and active load amplifiers, as well as common drain and common gate amplifiers. First, we will discuss the passive and active load amplifiers. The circuit on the left in Figure 1 is a passive load amplifier where resistor R is the passive load. The passive load amplifier can be replaced with the active load amplifier, also known as a common source amplifier, shown in the center of Figure 1. This amplifier uses an active load—transistor M2—in place

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of the resistor R shown in the circuit on the left. The active load configuration is advantageous in that it occupies less physical area on the semiconductor than the passive load configuration. The small signal equivalent circuit for the active load amplifier is shown on the right of Figure 1, where gm1 is the transconductance of transistor M1 and g_{m2} is the transconductance of transistor M2.

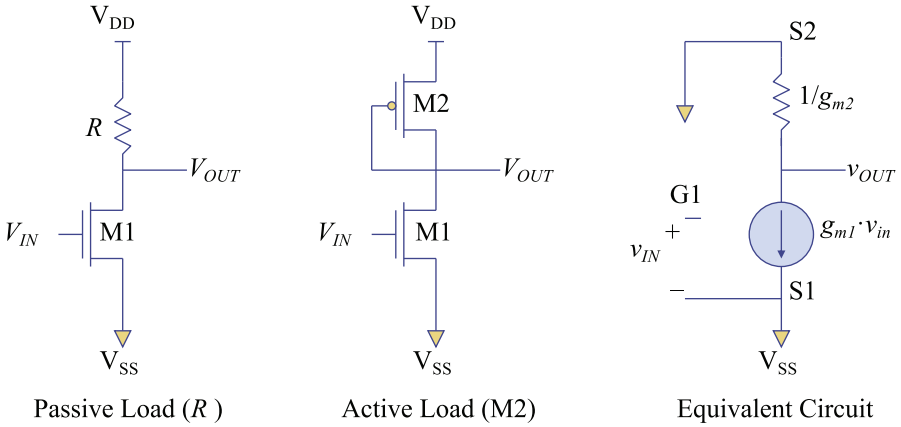


Figure 1. Passive and active load amplifiers.

We will now look at common drain amplifiers—or source followers, as they are sometimes called. These are used to lower the impedance level in the signal path. They can also perform level shifting of signals since the voltage between the gate and the source can be made arbitrarily large through correct design of the transistors. A source follower is constructed by using two transistors with the same carrier, either two n-channel transistors as shown on the right in Figure 2, or two p-channel transistors as shown on the left. The gain of the source follower is affected by the body effect in transistor M2 on the left, and transistor M1 on the right. Because the source and the body are not tied to the same potential in M2, the threshold voltage will change with body bias. This factor is referred to as "nu". The larger the source to body potential, the lower the gain of the amplifier.

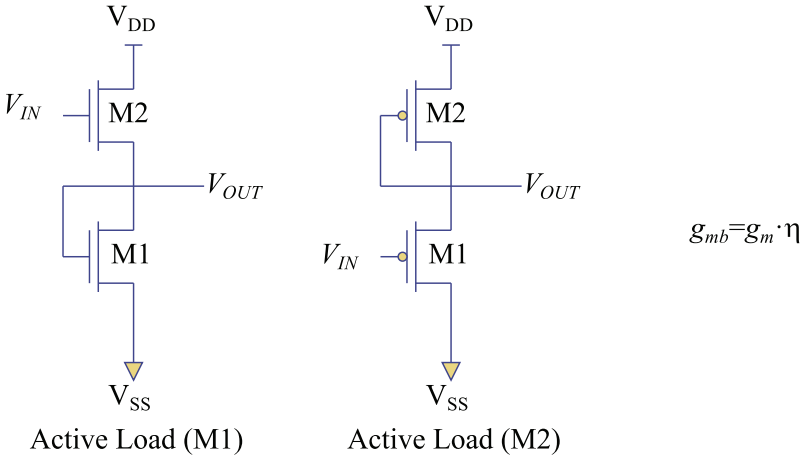


Figure 2. Common drain amplifiers (source followers).

The last configuration we will discuss here for a single transistor amplifier is the common gate amplifier (shown in Figure 3). The common gate amplifier is infrequently used. The gain of the amplifier is similar to that of the common source amplifier with an active load. Designers use this configuration less often than the common source or source follower. Designers will occasionally use this configuration in CMOS RF receivers, especially when operating at high frequencies, because of the ease of impedance matching and potential for lower noise.

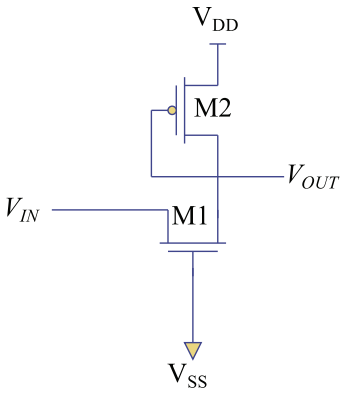
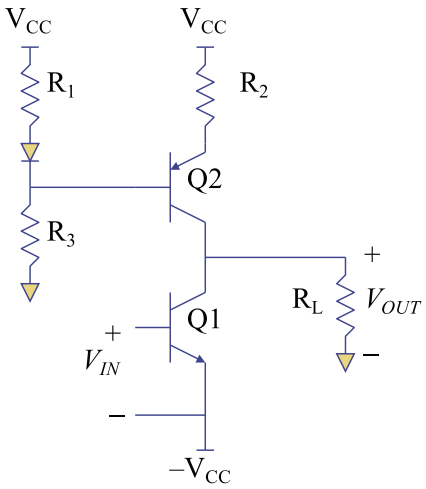


Figure 3. Common gate amplifier.

Next, we will discuss the Class A amplifier. It is one of the most common amplifier configurations. Figure 4 shows the Class A common emitter output stage. Common emitter circuits are most often used as output drivers in larger circuits. Common emitter circuits exhibit high gain characteristics. Because the transfer characteristic for this particular circuit is exponential in nature, the common emitter output stage exhibits more distortion than an emitter-follower output stage.



$$V_{OUT} = -R_L\left(I_S \exp\frac{V_{IN}}{V_T} - I_Q\right)$$

Figure 4. Class A common emitter output stage.

In Figure 5, we show the output voltage as a function of the input voltage for the Class A common emitter stage. We also refer to this type of graph as the transfer characteristic. The slope of the transfer characteristic for the common emitter stage is exponential in nature. If the slope were linear, there would be no distortion in the gain. Since the slope is non-linear, distortion is introduced into the amplification

stage. The transfer characteristic can also be affected by the load on the output. If there is a high resistance load, then Q2 will saturate, leading to a higher output voltage. If the resistance is low, then Q1 is forced into a cutoff condition. This lowers the output voltage on the positive side.

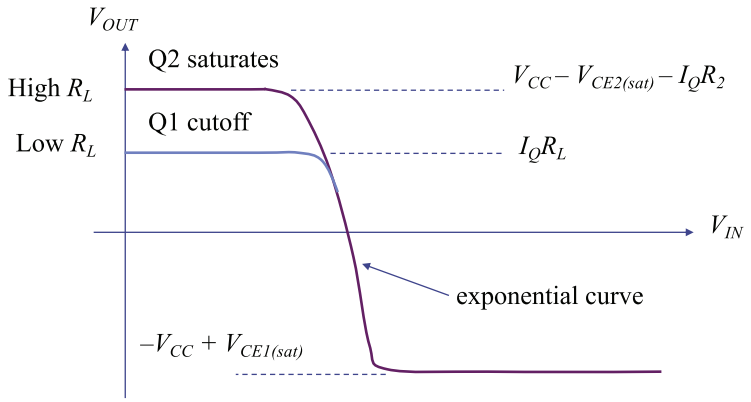


Figure 5. V_{OUT} vs. V_{IN} for Class A common emitter stage.

Let's look at a different and more popular way to implement the Class A amplifier. Figure 6 shows an example of a Class A common base output stage. In this example, the output voltage is the difference between the voltages on the collectors of Q2 and Q4. This is controlled by the input voltage, which is the difference between the voltages on the bases of Q1 and Q3.

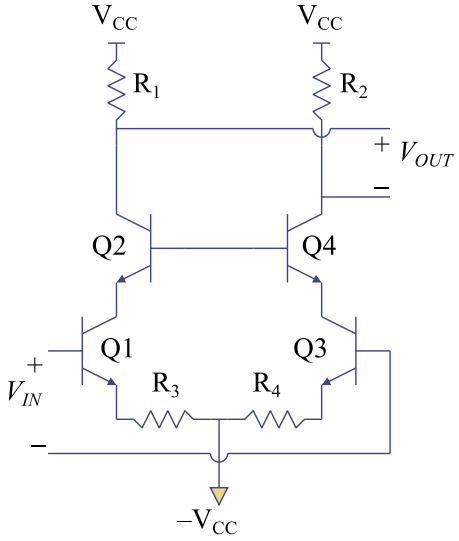


Figure 6. Class A common base output stage.

In next month's Feature Article, we will continue our discussion of amplifier circuits by talking about Class B amplifiers and Class AB amplifiers.

Technical Tidbit

Closed Loop Temperature Control and Chamber Coatings

Closed loop temperature control can help reduce particle generation from chamber coatings. Figure 1 shows an image of an advanced closed loop temperature control system for an etch tool. Each chamber in the upper portion of the image is instrumented with sensors which can be read by the main control system, located at the bottom portion of the image. The main control system can then provide feedback to the chamber heating elements to maintain a more uniform temperature.

Figure 1. 3D Model of a Closed Loop Temperature Control System for a multi-chamber instrument (image courtesy Watlow Electric Manufacturing Company).

Uniform temperature control reduces coefficient of thermal expansion mismatch effects, lowers stresses in films, and reduces laminar flow irregularities, which can all lead to particle generation. For example, to reduce the temperature change that is experienced by the chamber when the plasma is cycled

on and off, the dome is typically heated to approximately 80°C using a radiant heat lamp source. The radiant source is generally a plurality of high-power lamps mounted outside of the chamber. The lamps are mounted in an array above the dome. Typically, a reflector assembly is positioned proximate to the lamps to focus their radiant energy upon the dome surface. In a traditional system, to maintain the dome temperature at approximately 80°C during plasma cycling (i.e., during periods when the plasma is present and not present), a fan is mounted proximate to the dome to provide a continuous flow of room temperature air across the dome and thereby maintaining the dome at a constant temperature when the plasma is present. However, such a cooling technique is not very effective and the dome temperature may fluctuate as much as ±40°C depending upon the ambient room temperature. Large thermal fluctuation of the chamber surfaces causes the chamber to expand and contract such that material deposited on the chamber walls and dome during the etch process flakes and falls upon the wafer being processed. The microcontamination particles make the wafer unusable. Therefore, use of a closed loop temperature control system is important. It can reduce the temperature fluctuations, which in turn reduces particle generation.

Ask the Experts

Q: What is the purpose of a channel-stop implant?

A: A channel stop implant is a region implanted with ions to help prevent leakage between two structures, typically transistors, in a process technology. To understand this a little better, please refer to Figure 1. In the figure, we show a cross-section view of a typical wafer fabrication process, or process technology. When two transistors are placed close together, like we show in Figure 1, and there is a polysilicon or metal layer above the gap, then a parasitic transistor will form. A parasitic transistor is an unwanted transistor that is created as an unintended consequence of the layout of the actual circuitry. VLO VSIG, and VHI indicate the source, gate and drain of the parasitic transistor, and the horizontal arrow indicates the leakage path that the parasitic transistor creates between the two properly designed transistors. To suppress this leakage, process engineers can implant the opposite polarity doping in the channel, or the region between the two N-Wells. For example, if there are N-Wells on either side, like we show in Figure 1, then the channel stop implant would be a P-type implant. The pink region with the bright red border indicates the location of a channel stop implant that can suppress this leakage path between the transistors.

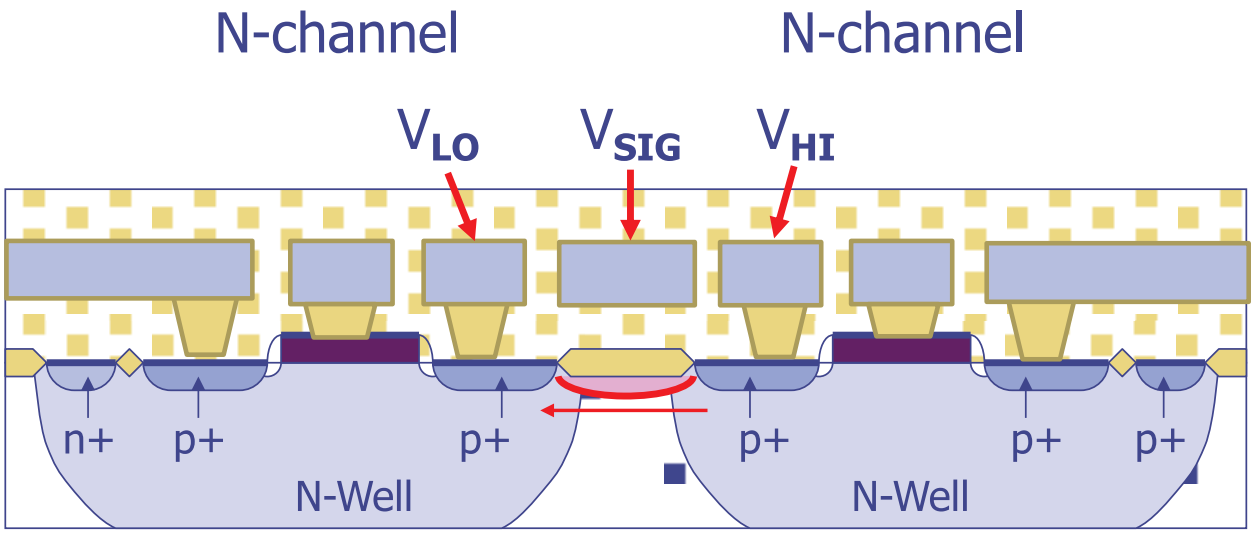


Figure 1. Cross-section Diagram Illustrating the Concept of Leakage Between Transistors and the Location of a Channel-Stop Implant.

Spotlight: Semiconductor Reliability and Product Qualification

OVERVIEW

Package reliability and product qualification continues to evolve with the electronics industry. New electronics applications require new approaches to reliability and qualification. In the past, reliability meant discovering, characterizing and modeling failure mechanisms and determining their impact on the reliability of the circuit. Today, reliability can involve tradeoffs between performance and reliability, assessing the impact of new materials, dealing with limited margins, etc. in particular, the proliferation of new package types. This requires information on subjects like: statistics, testing, technology, processing, materials science, chemistry, and customer expectations. While customers expect high reliability levels, incorrect testing, calculations, and qualification procedures can severely impact reliability. Your company needs competent engineers and scientists to help solve these problems. ***Semiconductor Reliability and Qualification*** is a four-day course that offers detailed instruction on a variety of subjects pertaining to semiconductor reliability and qualification. This course is designed for every manager, engineer, and technician concerned with reliability in the semiconductor field, qualifying semiconductor components, or supplying tools to the industry.

What Will I Learn By Taking This Class?

Participants learn to develop the skills to determine what failure mechanisms might occur, and how to test for them, develop models for them, and eliminate them from the product.

1. **Overview of Reliability and Statistics.** Participants learn the fundamentals of statistics, sample sizes, distributions and their parameters.
2. **Failure Mechanisms.** Participants learn the nature and manifestation of a variety of failure mechanisms that can occur both at the die and at the package level. These include: time-dependent dielectric breakdown, hot carrier degradation, electromigration, stress-induced voiding, moisture, corrosion, contamination, thermomechanical effects, interfacial fatigue, etc.
3. **Qualification Principles.** Participants learn how test structures can be designed to help test for a particular failure mechanism.
4. **Test Strategies.** Participants learn about the JEDEC test standards, how to design screening tests, and how to perform burn-in testing effectively.

COURSE OBJECTIVES

1. The seminar will provide participants with an in-depth understanding of the failure mechanisms, test structures, equipment, and testing methods used to achieve today's high reliability components.
2. Participants will be able to gather data, determine how best to plot the data and make inferences from that data.
3. The seminar will identify the major failure mechanisms, explain how they are observed, how they are modeled, and how they are eliminated.
4. The seminar offers a variety of video demonstrations of analysis techniques, so the participants can get an understanding of the types of results they might expect to see with their equipment.
5. Participants will be able to identify the steps and create a basic qualification process for semiconductor devices.

6. Participants will be able to knowledgeably implement screens that are appropriate to assure the reliability of a component.
7. Participants will be able to identify appropriate tools to purchase when starting or expanding a laboratory.

COURSE OUTLINE

Day 1 (Lecture Time 8 Hours)

1. Introduction to Reliability
    1. Basic Concepts
    2. Definitions
    3. Historical Information
2. Statistics and Distributions
    1. Basic Statistics
    2. Distributions (Normal, Lognormal, Exponent, Weibull)
    3. Which Distribution Should I Use?
    4. Acceleration
    5. Number of Failures

Day 2 (Lecture Time 8 Hours)

1. Overview of Die-Level Failure Mechanisms
    1. Time Dependent Dielectric Breakdown
    2. Hot Carrier Damage
    3. Negative Bias Temperature Instability
    4. Electromigration
    5. Stress Induced Voiding
2. Package Level Mechanisms
    1. Ionic Contamination
    2. Moisture/Corrosion
        1. Failure Mechanisms
        2. Models for Humidity
        3. Tja Considerations
        4. Static and Periodic stresses
        5. Exercises
    3. Thermo-Mechanical Stress
        1. Models
        2. Failure Mechanisms
    4. Interfacial Fatigue
        1. Low-K fracture
    5. Thermal Degradation/Oxidation

Day 3 (Lecture Time 8 Hours)

1. Package Attach (Solder) Reliability
    1. Creep/Sheer/Strain
    2. Lead-Free Issues
    3. Electromigration/Thermomigration
    4. MSL Testing
    5. Exercises
2. TSV Reliability Overview
3. Board Level Reliability Mechanisms
    1. Interposer
    2. Substrate
4. Electrical Overstress/ESD
5. Test Structures and Test Equipment
6. Developing Screens, Stress Tests, and Life Tests
    1. Burn-In
    2. Life Testing
    3. HAST
    4. JEDEC-based Tests
    5. Exercises

Day 4 (Lecture Time 8 Hours)

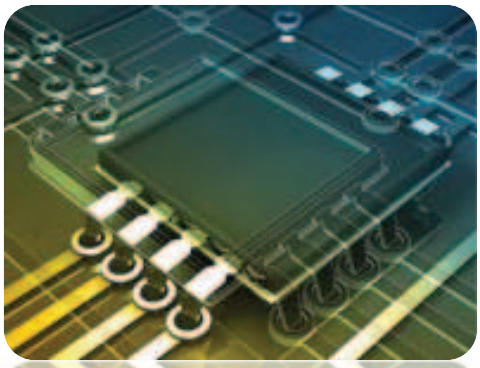
1. Calculating Chip and System Level Reliability
2. Developing a Qualification Program
    1. Process
    2. Standards-Based Qualification
    3. Knowledge-Based Qualification
    4. MIL-STD Qualification
    5. JEDEC Documents (JESD47H, JESD94, JEP148)
    6. AEC-Q100 Qualification
    7. When do I deviate? How do I handle additional requirements?
    8. Exercises and Discussion

INSTRUCTIONAL STRATEGY

By using a combination of instruction by lecture, video, problem solving and question/answer sessions, participants will learn practical approaches to the failure analysis process. From the very first moments of the seminar until the last sentence of the training, the driving instructional factor is **application**. We use instructors who are internationally recognized experts in their fields that have years of experience (both current and relevant) in this field. The handbook offers hundreds of pages of additional reference material the participants can use back at their daily activities.

The Semitracks Analysis Instructional Videos™

One unique feature of this workshop is the video segments used to help train the students. Reliability Analysis is a visual discipline. The ability to identify nuances and subtleties in graphical data is critical to locating and understanding the defect. Some tools output video images that must be interpreted by engineers and scientists. No other course of this type uses this medium to help train the participants. These videos allow the analysts to directly compare material they learn in this course with real analysis work they do in their daily activities.



Upcoming Webinars

(Click on each item for details)

Semiconductor Reliability / Product Qualification WEBINAR

4 sessions of 4 hours each
US: August 15 – 18, 2022 (Mon – Thur),
8:00 A.M. – 12:00 NOON PDT

Wafer Fab Processing WEBINAR

4 sessions of 4 hours each
US: October 3 – 6, 2022 (Mon – Thur),
8:00 A.M. – 12:00 NOON PDT

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We are always looking for ways to enhance our courses and educational materials.

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We look forward to hearing from you!