Issue 144 June 2021

InfoTracks

Semitracks Monthly Newsletter

Basic Failure Mechanisms

By Christopher Henderson

This month we continue our series of Feature Articles on Failure Mechanisms. In last month's Feature Article, we discussed Particles and Defects. This month we will discuss Die Reliability-Related Failure Mechanisms.

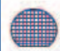
Die Reliability-Related Failure Mechanisms

In terms of reliability problems, the same logic applies here as we discussed in last month's Feature Article. Large defects would likely cause reliability problems. The medium-sized defects in the center may or may not cause reliability problems, and the small defects to the right would be unlikely to cause defects (please refer to Figure 1 in last month's article to understand these comments).

In modern ICs, many defects are no longer visible. In other words, they cannot be easily seen with an optical or scanning electron microscope. These types of defects may require the transmission electron microscope (TEM) or atomic force microscope (AFM) to identify and characterize them. Figures 1 and 2 show examples of particles that are only visible using the TEM.

In this Issue:

Page 1	Basic Failure Mechanisms
Page 7	Technical Tidbit
Page 8	Ask the Experts
Page 9	Spotlight
Page 13	Upcoming Courses



SEMITRACKS, INC.
Semiconductor, Microelectronics, Microsystems, and Nanotechnology Training

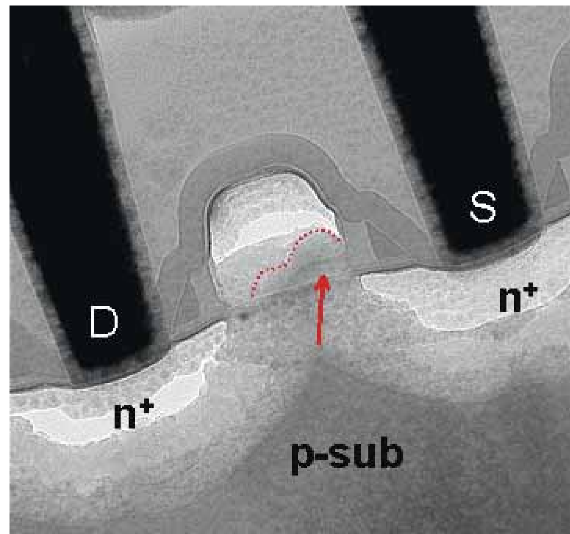


Figure 1. TEM image of wet chemically treated cross-sectional lamella of a failed pass gate n-channel transistor. A large low-doped poly-Si grain, indicated by the arrow marker, close to the source-channel interface can be observed in the failed polysilicon gate.

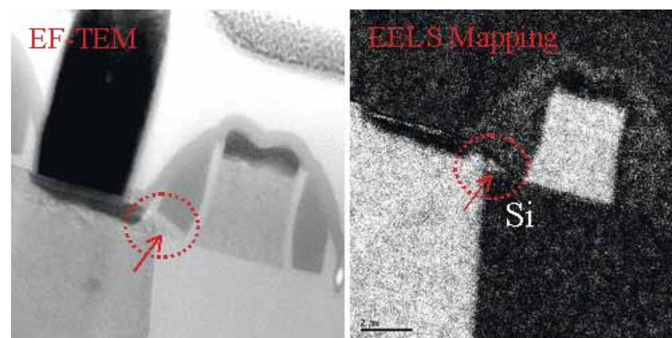


Figure 2. A silicon-rich defect buried under the transistor sidewall spacer..

Wear Out Mechanisms

Even though most failures are the result of defective conditions or process variations, sometimes the materials on the IC can simply wear out.

The symptoms of wear out include the following:

- Time Dependent Dielectric Breakdown
- Hot Carrier Degradation
- Negative Bias Temperature Instability
- Electromigration
- Stress Voiding

We will give a brief overview of each of these failure mechanisms.

Time Dependent Dielectric Breakdown (TDDB)

Time Dependent Dielectric Breakdown (TDDB) is a reliability concern for most ICs. The gate dielectric can wear out and break down over time when subjected to a high electric field, as shown in Figure 3. In a CMOS circuit, this high electric field will be present during some portion of the operation of the chip when bias is applied. While researchers disagree on what exactly is occurring at the atomic level, they believe that a combination of electric field and electron or hole movement within the gate region creates damage to the oxide structure. The damage builds up, causing increased leakage, and can eventually lead to breakdown of the oxide. The breakdown results in a short in some instances, while in thin dielectrics, the result can be a noise signature. If the leakage or noise levels are too high, then the transistor may not function properly, leading to IC malfunction. TDDB is a function of the duty cycle of the transistor, the electric field or voltage across the gate and the temperature (at least in thicker oxides). Of all of the reliability failure mechanisms, TDDB is the most common intrinsic reliability-related failure mechanism to be observed in the field.

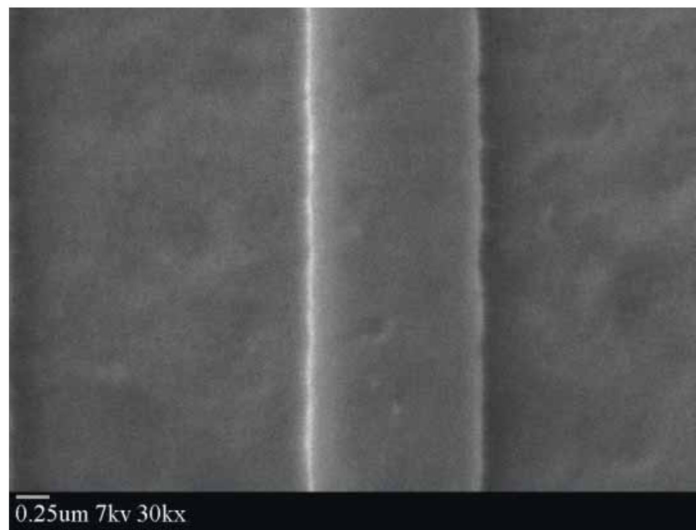


Figure 3. Results of dielectric breakdown.

Hot Carrier Degradation

Hot Carrier Degradation, sometimes referred to as Hot Carrier Effects (HCE) or Hot Carrier Injection (HCI), is another heavily studied failure mechanism. Basically, hot carrier degradation is caused by energetic electrons creating interface states at the silicon-gate dielectric interface, or damage to the gate dielectric itself. High electric fields in the drain region of the transistor exacerbate hot carrier damage, so a great deal of effort goes into lowering the electric field there. Techniques such as retrograde channels, lightly-doped drain (LDD) spacers, voltage scaling, and various design rules help to mitigate its effects. In fact, hot carrier effects are very design specific, so many design tools employ rules to help designers avoid potential problems. It is not as common to see field returns exhibiting this failure mechanism. Usually, hot carrier degradation in the field is more a function of incorrect use than wear out. Obviously an incorrectly designed part can fail from this mechanism as well.

Negative Bias Temperature Instability (NBTI)

Negative Bias Temperature Instability (NBTI) is another heavily studied failure mechanism. NBTI is particularly challenging because there are no good solutions for reducing its effects. NBTI was studied in the 1960s and 1970s when PMOS technologies were being manufactured, but work ceased during the early years of CMOS development in the 1980s and early 1990s. It wasn't until the late 1990s that this mechanism began to show up in advanced technologies (feature sizes less than 0.25µm). NBTI is basically a buildup of charge in the p-channel transistor that interferes with its operation. The drive current is reduced, the subthreshold leakage changes, and the reverse biased leakage increases. Researchers are actively studying this mechanism, and they do not fully understand its behavior and parameters yet. NBTI is thought to be a reaction-diffusion process. Energetic holes or electrons break the hydrogen bond at the silicon-dielectric interface, causing the hydrogen to diffuse through the gate. This leaves charged interface states that affect the transistor operation. NBTI is worse at higher temperatures, since higher temperatures reduce the bond strength. NBTI is also worse in dielectrics containing nitrogen. The nitrogen-silicon bond is not as strong as the nitrogen oxygen bond. Unfortunately, though, very thin silicon dioxide dielectrics require nitrogen to prevent a phenomenon called boron penetration—a condition where boron diffuses from the heavily doped polysilicon gate into the transistor channel.

Electromigration

Electromigration, sometimes abbreviated as EM, is yet another heavily studied failure mechanism. EM is basically the movement of atoms in a high electron flow regime. This occurs in interconnect lines when the current densities are between 1×10^6 amps/cm^2 and 1×10^7 amps/cm^2. As demonstrated in Figure 4, atom movement in the interconnect can result in opens or shorts.

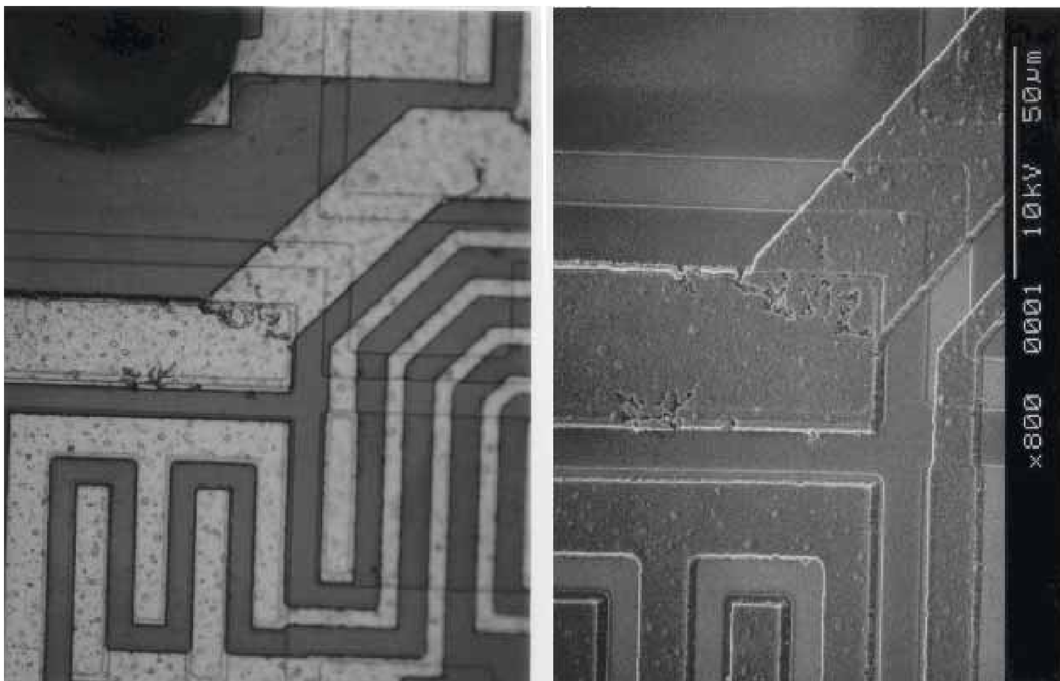


Figure 4. Optical (left) and SEM (right) electromigration images show voiding at the entrance to the contact..

Electromigration can be controlled through the choice of appropriate materials, processing techniques, and design constraints. In ICs that use aluminum interconnects, engineers use sputter metal rather than evaporated metal, and include a small percentage of copper. Sputtered metal contains larger grain sizes, providing less opportunity for the atoms to move along the grain boundaries. The copper accumulates at the grain boundaries, inhibiting movement somewhat. Process engineers also use a sandwich structure for the metallization (*e.g.,* Ti-AlCu-TiN). The titanium and titanium nitride are less susceptible to electromigration, even though they have a much higher resistance. They serve as a shunt path in case a void forms in the aluminum-copper layer. In ICs that use copper interconnects, engineers must tightly control the top interface between the copper and the barrier layer, since EM in copper tends to occur on the surface. The CMP and subsequent capping process are critical to achieving good EM performance. Finally, design engineers use layout rules to ensure that the current densities are not so high as to cause EM. Because of these developments in understanding EM, this mechanism is observed less and less often in field use.

Stress-Induced Voiding

Stress induced voiding, also called stress voiding or stress migration, is a lesser-known failure mechanism that can result in open interconnect, as shown in Figure 5. Stress voiding can occur because of differences in the coefficients of thermal expansion between the metal layers and the dielectrics, or because of volume contraction resulting from sintering (alloying) processes. If the voids grow big enough, they will result in a resistance increase or open in the circuit, causing an electrical failure.

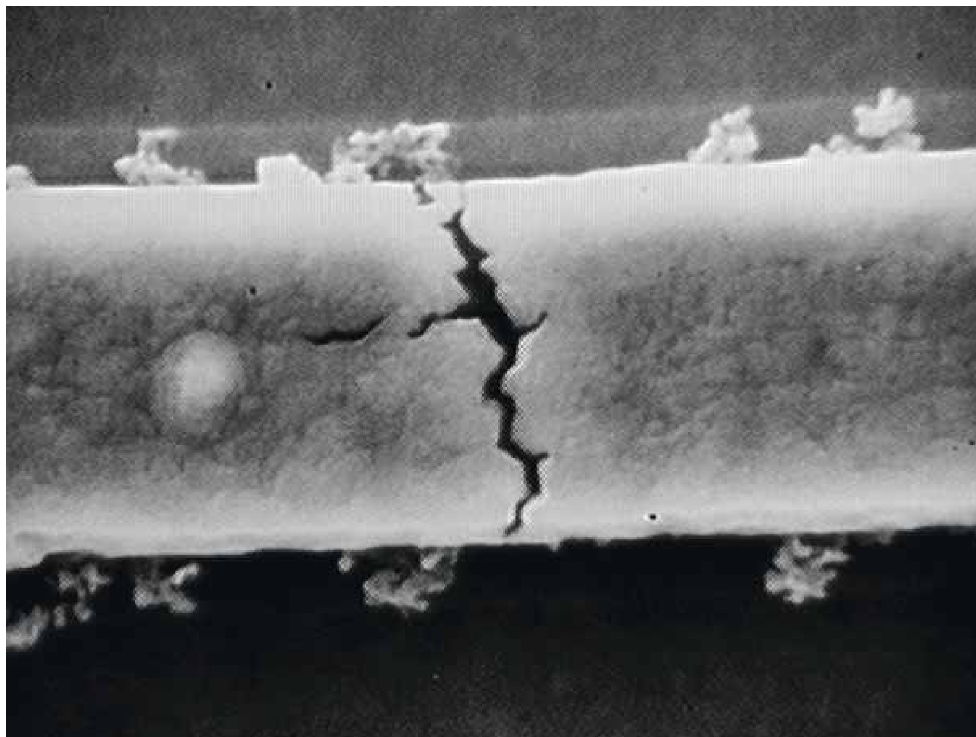


Figure 5. Cracked interconnect caused by stress-induced voiding.

Stress voiding does not require power to occur; ICs sitting in storage can be affected by this mechanism. Basically, stress is present in the metal system at all times. If there is some type of defect that induces a stress gradient, the atomic movement will ensue. Stress voiding occurs in both aluminum and copper metallization systems. Although some companies have been severely affected by this mechanism, many have never experienced this problem. The quality of the sidewalls of the metal, the dielectric layers, and the vias are critical in controlling this mechanism. The key is to eliminate possible nucleation sites for voids on the interconnect sidewalls and in the vias. Stress voiding is difficult to characterize through accelerated testing, since there are two competing phenomena driving stress voiding. Although atom movement increases with temperature, the stress in the IC goes down with temperature increases. Therefore, most companies concentrate on eliminating stress voiding through process control, rather than attempting to characterize reliability through accelerated testing.

In next month's Feature Article, we will cover Package-Related Failure Mechanisms.

Technical Tidbit

Self-Heating in FinFETs

In this month's Technical Tidbit, we will cover a reliability issue that is now prevalent in FinFET technologies: self-heating. Self-heating is a phenomenon where the transistor is unable to efficiently dissipate its own heat from operation, leading to higher temperatures. The higher temperatures in turn, degrade the reliability of the transistors and the overall reliability of the integrated circuit.

Self-heating tends to strongly impact failure mechanisms with positive activation energies. Hot carrier effects, especially in the PMOS transistor, can be exacerbated by self-heating effects. Bias Temperature Instability recovery is thermally dependent. Electromigration is also strongly dependent on temperature, so any interconnect segments in close proximity to hot fins could be affected. There is more limited impact on failure mechanisms like Time Dependent Dielectric Breakdown. While we normally think about TDDB as a bias-driven failure mechanism, the bond-breaking mechanism associated with TDDB has a strong thermal component. As such, devices experiencing self-heating will have degraded TDDB lifetimes. In addition, functional stress tests, like burn-in or HTOL have the potential to push devices into temperature ranges that are higher than normal. While extreme temperatures are unlikely, thermal runaway might happen in extreme cases. While FinFET self-heating isn't specifically a failure mechanism, it contributes to a number of failure mechanisms, reducing the reliability of the IC.

To summarize the self-heating issue, taller, narrower fins confine the heat in the fins more tightly, leading to higher temperatures in the silicon fins themselves. Dielectric materials surround the fins on their sides, and there is limited heat dissipation through these materials. The only efficient path to remove heat is through the bottom of the fin, so the taller and narrower the fin is, the less efficient the heat removal path. In a bulk FinFET process, the heat can at least dissipate through the fin body down to the substrate. However, in an SOI FinFET process, there is an isolation oxide, which not only provides electrical isolation, but also causes thermal insulation. As such, the primary path to dissipate heat in an SOI FinFET process is through the source/drain contacts into the metal stack. This path is even less efficient than dissipation into the substrate for a bulk FinFET process, so an SOI FinFET has more self-heating than a bulk FinFET process. Figure 1 indicates the heat dissipation properties and paths.

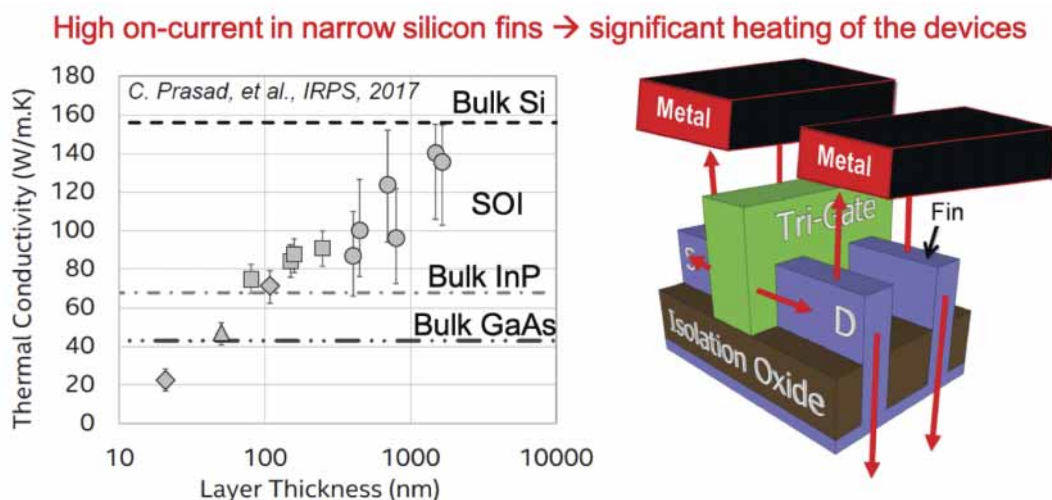


Figure 1. Graph shows FinFET Thermal Conductivity as a Function of Layer Thickness; Diagram shows the Thermal Paths for Heat Dissipation in the FinFET.

Ask the Experts

Q: Which technique is more likely to replace the FinFET: nanowires or nanosheets?

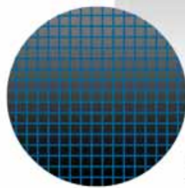
A: That is the question to which many would like to know the answer! It is not certain right now which approach will be preferred. Samsung has demonstrated nanowires for their 3nm technology, and IBM has demonstrated nanosheets for their 2nm technology. While nanowires provide better control of the channel, nanosheets allow larger drain currents within the individual transistors. Ultimately, it will be a mixture of performance and cost that will drive the outcome of this decision.

Learn from the Experts...

...wherever you are.

-Learn at your own pace.
-Eliminate travel expenses.
-Personalize your experience.
-Search a wealth of information.

Visit us at www.semitracks.com for more information.



SEMITRACKS, INC.

Semiconductor, Microelectronics, Microsystems, and Nanotechnology Training

Spotlight: Semiconductor Reliability and Product Qualification

OVERVIEW

Package reliability and product qualification continues to evolve with the electronics industry. New electronics applications require new approaches to reliability and qualification. In the past, reliability meant discovering, characterizing and modeling failure mechanisms and determining their impact on the reliability of the circuit. Today, reliability can involve tradeoffs between performance and reliability, assessing the impact of new materials, dealing with limited margins, etc. in particular, the proliferation of new package types. This requires information on subjects like: statistics, testing, technology, processing, materials science, chemistry, and customer expectations. While customers expect high reliability levels, incorrect testing, calculations, and qualification procedures can severely impact reliability. Your company needs competent engineers and scientists to help solve these problems. ***Semiconductor Reliability and Qualification*** is a four-day course that offers detailed instruction on a variety of subjects pertaining to semiconductor reliability and qualification. This course is designed for every manager, engineer, and technician concerned with reliability in the semiconductor field, qualifying semiconductor components, or supplying tools to the industry.

What Will I Learn By Taking This Class?

Participants learn to develop the skills to determine what failure mechanisms might occur, and how to test for them, develop models for them, and eliminate them from the product.

1. **Overview of Reliability and Statistics.** Participants learn the fundamentals of statistics, sample sizes, distributions and their parameters.
2. **Failure Mechanisms.** Participants learn the nature and manifestation of a variety of failure mechanisms that can occur both at the die and at the package level. These include: time-dependent dielectric breakdown, hot carrier degradation, electromigration, stress-induced voiding, moisture, corrosion, contamination, thermomechanical effects, interfacial fatigue, etc.
3. **Qualification Principles.** Participants learn how test structures can be designed to help test for a particular failure mechanism.
4. **Test Strategies.** Participants learn about the JEDEC test standards, how to design screening tests, and how to perform burn-in testing effectively.

COURSE OBJECTIVES

1. The seminar will provide participants with an in-depth understanding of the failure mechanisms, test structures, equipment, and testing methods used to achieve today’s high reliability components.
2. Participants will be able to gather data, determine how best to plot the data and make inferences from that data.
3. The seminar will identify the major failure mechanisms, explain how they are observed, how they are modeled, and how they are eliminated.
4. The seminar offers a variety of video demonstrations of analysis techniques, so the participants can get an understanding of the types of results they might expect to see with their equipment.
5. Participants will be able to identify the steps and create a basic qualification process for semiconductor devices.

6. Participants will be able to knowledgeably implement screens that are appropriate to assure the reliability of a component.
7. Participants will be able to identify appropriate tools to purchase when starting or expanding a laboratory.

COURSE OUTLINE

Day 1 (Lecture Time 8 Hours)

1. Introduction to Reliability
    1. Basic Concepts
    2. Definitions
    3. Historical Information
2. Statistics and Distributions
    1. Basic Statistics
    2. Distributions (Normal, Lognormal, Exponent, Weibull)
    3. Which Distribution Should I Use?
    4. Acceleration
    5. Number of Failures

Day 2 (Lecture Time 8 Hours)

1. Overview of Die-Level Failure Mechanisms
    1. Time Dependent Dielectric Breakdown
    2. Hot Carrier Damage
    3. Negative Bias Temperature Instability
    4. Electromigration
    5. Stress Induced Voiding
2. Package Level Mechanisms
    1. Ionic Contamination
    2. Moisture/Corrosion
        1. Failure Mechanisms
        2. Models for Humidity
        3. Tja Considerations
        4. Static and Periodic stresses
        5. Exercises
    3. Thermo-Mechanical Stress
        1. Models
        2. Failure Mechanisms
    4. Interfacial Fatigue
        1. Low-K fracture
    5. Thermal Degradation/Oxidation

Day 3 (Lecture Time 8 Hours)

1. Package Attach (Solder) Reliability
    1. Creep/Sheer/Strain
    2. Lead-Free Issues
    3. Electromigration/Thermomigration
    4. MSL Testing
    5. Exercises
2. TSV Reliability Overview
3. Board Level Reliability Mechanisms
    1. Interposer
    2. Substrate
4. Electrical Overstress/ESD
5. Test Structures and Test Equipment
6. Developing Screens, Stress Tests, and Life Tests
    1. Burn-In
    2. Life Testing
    3. HAST
    4. JEDEC-based Tests
    5. Exercises

Day 4 (Lecture Time 8 Hours)

1. Calculating Chip and System Level Reliability
2. Developing a Qualification Program
    1. Process
    2. Standards-Based Qualification
    3. Knowledge-Based Qualification
    4. MIL-STD Qualification
    5. JEDEC Documents (JESD47H, JESD94, JEP148)
    6. AEC-Q100 Qualification
    7. When do I deviate? How do I handle additional requirements?
    8. Exercises and Discussion

INSTRUCTIONAL STRATEGY

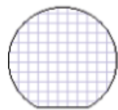
By using a combination of instruction by lecture, video, problem solving and question/answer sessions, participants will learn practical approaches to the failure analysis process. From the very first moments of the seminar until the last sentence of the training, the driving instructional factor is **application**. We use instructors who are internationally recognized experts in their fields that have years of experience (both current and relevant) in this field. The handbook offers hundreds of pages of additional reference material the participants can use back at their daily activities.

The Semitracks Analysis Instructional Videos™

One unique feature of this workshop is the video segments used to help train the students. Reliability Analysis is a visual discipline. The ability to identify nuances and subtleties in graphical data is critical to locating and understanding the defect. Some tools output video images that must be interpreted by engineers and scientists. No other course of this type uses this medium to help train the participants. These videos allow the analysts to directly compare material they learn in this course with real analysis work they do in their daily activities.

You may want to stress some aspects more than others or conduct a simple one-day overview course. Many of our clients seek ongoing just-in-time training that builds in-depth, advanced levels of reliability expertise. We'll work with you to determine the best course of action and create a statement of work that emulates the very best practices of semiconductor reliability analysis.

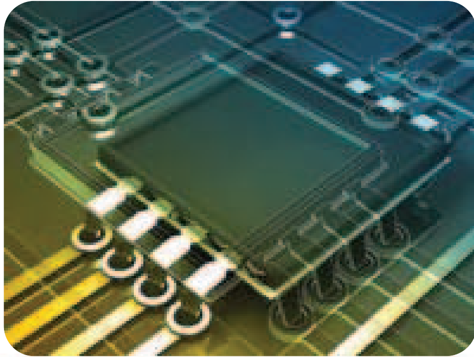
Our instructors are active in the field and they practice the disciplines daily. Please give us a call (505) 858-0454 or drop us an e-mail (info@semitracks.com).



SEMITRACKS INC.

Semiconductor, Microelectronics, Microsystems and Nanotechnology Training

6501 Wyoming NE, Suite C215
Albuquerque, NM 87109-3971
Tel. (505) 858-0454
Fax (866) 205-0713
e-mail: info@semitracks.com



Feedback

If you have a suggestion or a comment regarding our courses, online training, discussion forums, or reference materials, or if you wish to suggest a new course or location, please call us at 1-505-858-0454 or Email us (info@semitracks.com).

To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered in the next newsletter, please contact Jeremy Henderson by Email (jeremy.henderson@semitracks.com).

We are always looking for ways to enhance our courses and educational materials.

~

For more information on Semitracks online training or public courses, visit our web site!

http://www.semitracks.com

To post, read, or answer a question, visit our forums.
We look forward to hearing from you!

Upcoming Webinars

(Click on each item for details)

Semiconductor Reliability / Product Qualification

4 sessions of 4 hours each
Europe: August 30 – September 2, 2021
(Mon – Thur), 1:00 P.M. – 5:00 P.M. CET