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InfoTracks

Semitracks Monthly Newsletter

Reliability Test Equipment: Wafer Level, Part 2

By Christopher Henderson

In Part 2, we will continue to cover reliability test equipment. The appropriate test equipment is essential for conducting reliability studies. In addition, one must know how to set up the equipment and understand issues related to cabling, noise, and long-term testing.

Figure 7. Illustration of Keithley Instruments' rack-mounted system.

Like Agilent, Keithley also offers a variety of instruments that one can use for wafer-level testing. Figure 7 shows an example of Keithley's rack-mounted system. Keithley sells both UNIX and PC-based systems. Today, PC-based systems are the most common because of their lower cost. In fact, the SCS-4200 system is now PC-based as well. It is a Windows-based system that can make

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measurements and store the files locally. It can also be connected to a network to allow files to be easily shared. Keithley also sells a number of different switch matrices that allow the user to build a system appropriate for his or her application.

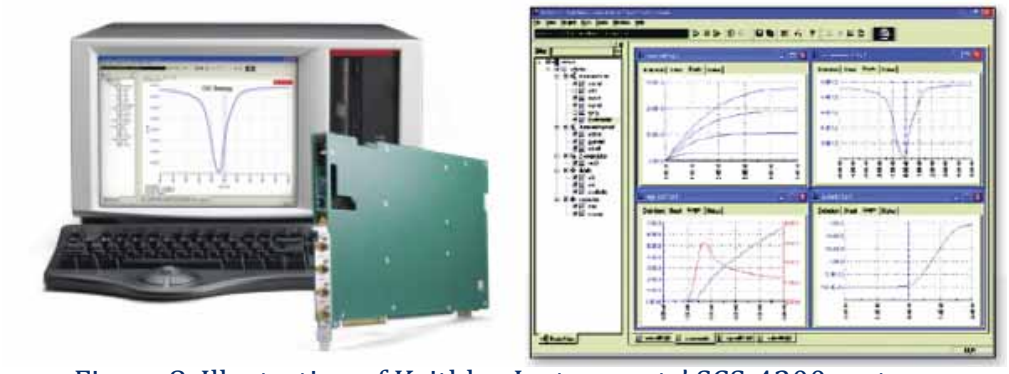


Figure 8. Illustration of Keithley Instruments' SCS-4200 system.

As illustrated in Figure 8, the Keithley SCS-4200 makes an attractive alternative to the Agilent 4070 and 4080 series for those who can get by without needing the lowest noise levels. It is straightforward to use the system with an existing probe station for engineering measurements. It can also be interfaced with automated probe systems for high throughput measurements. It uses Keithley Interactive Test Environment (KTEI) Software for its interface.

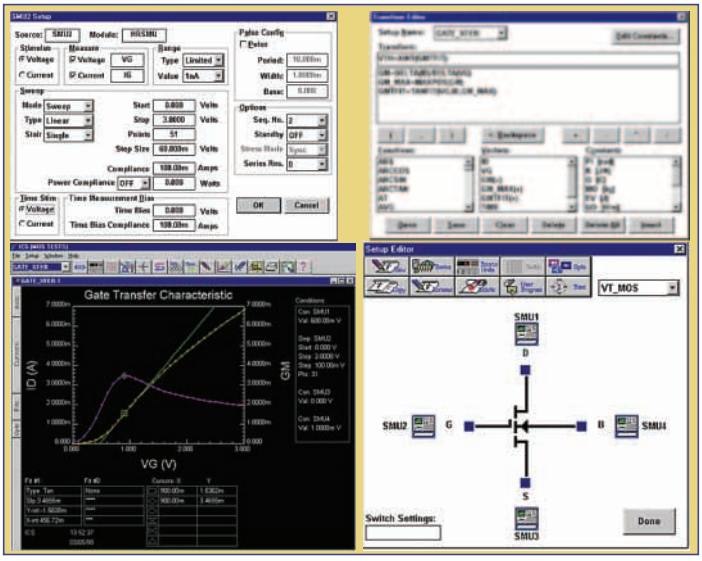


Figure 9. Illustration of Metrics ICS software.

The main competitor to Agilent's Interactive Characterization System (ICS) and Keithley's KTEI software is Metrics Technology. As shown in Figure 9, Metrics sells a version of ICS that is quite versatile. The main advantage to the Metrics software is that it costs less than Agilent's software. Furthermore, it can be connected to a variety of semiconductor parameter analyzers, including Agilent 4140 series, 4150

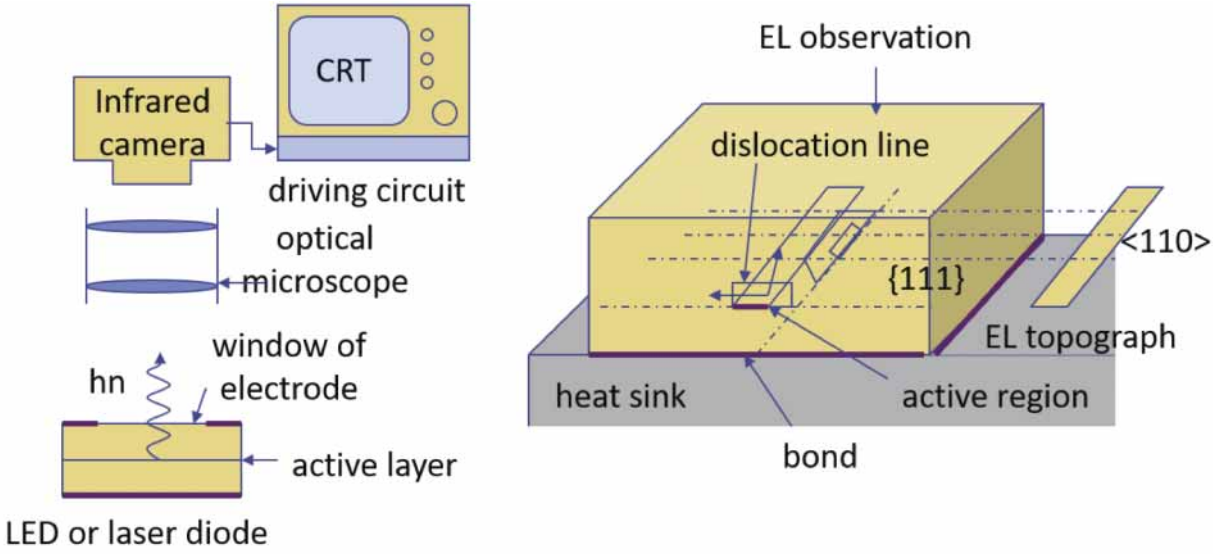
series, Keithley 4200 series, and Tektronix curve tracers. The interface is quite similar to Agilent's software, making it easy to go back and forth between the two. Metrics also sells a software package for performing capacitance-voltage measurements called I/CV and one for performing wafer-level reliability that includes algorithms for Time-Dependent Dielectric Breakdown V-RAMP and J-RAMP tests; hot carrier and NBTI measurements; Gummel characteristics; charge pumping measurements; and many more.

We will conclude our discussion of Reliability Test Equipment in the July Newsletter.

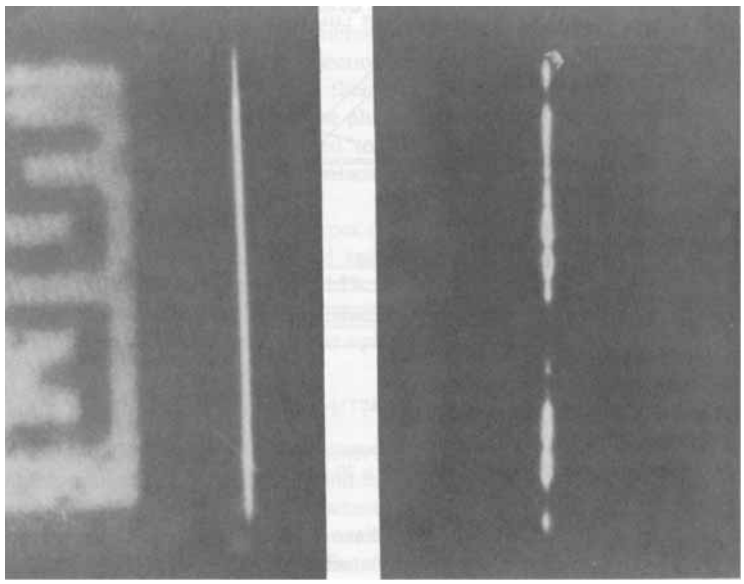
Technical Tidbit

Electroluminescence

In this month's technical tidbit, we will discuss Electroluminescence.

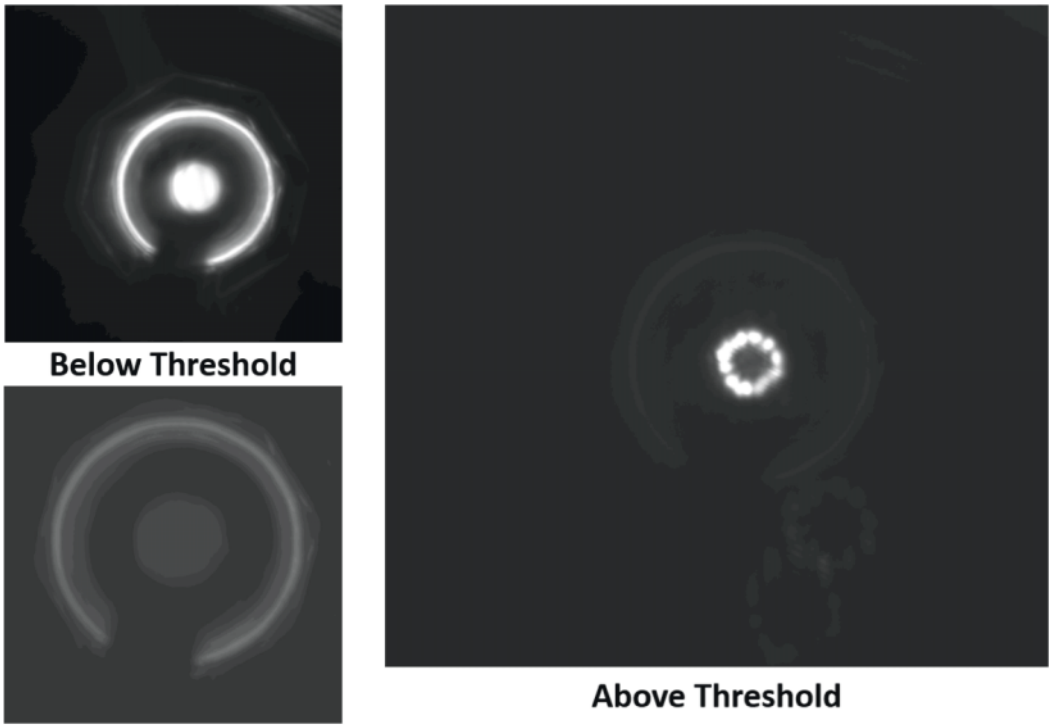


An important technique for optoelectronics and silicon photonics analysis is electroluminescence (EL). Electroluminescence is the equivalent to photon emission microscopy in standard integrated circuit failure analysis. One applies power to the device and collects an emission pattern. One can improve the interpretation of the data by collecting spectral information as well. The image on the left shows the electroluminescence observation system. The image on the right shows an illustration of an elongation model for the <110> crystallographic plane dislocation network.



Let's look at an example of electroluminescence. These images show active stripe electroluminescence observed through the window of a degraded laser showing dark regions. The left image shows the electroluminescence stripe of an undegraded laser, while the right image shows electroluminescence from a degraded laser after aging. We can see that the emission pattern changed during the accelerated aging tests. The EL test allows engineers to localize the dark regions for further materials characterization.

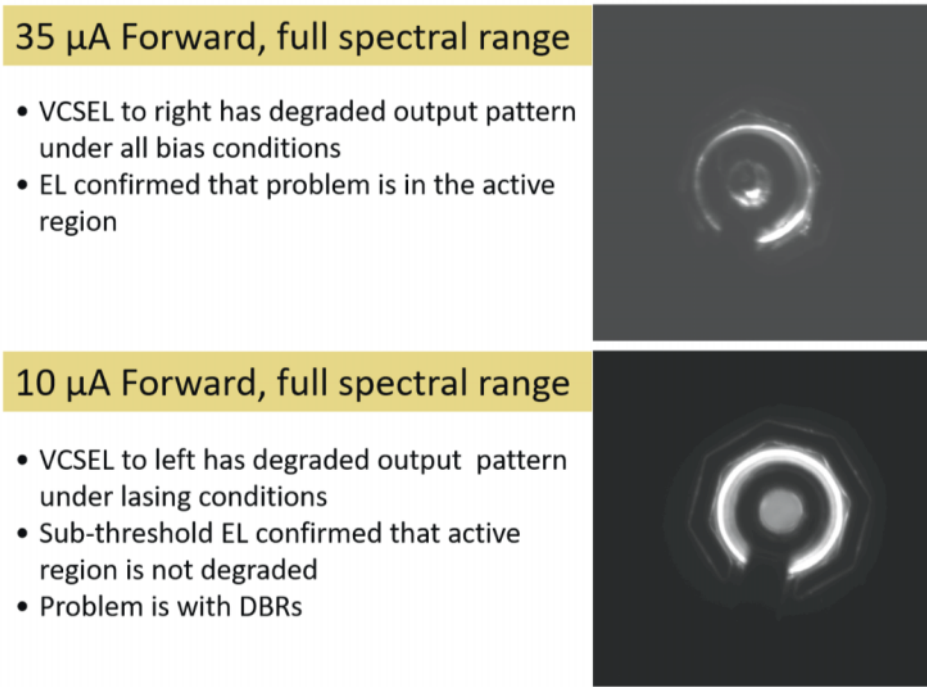
Engineers perform electroluminescence imaging with a liquid nitrogen-cooled silicon array CCD camera. These systems can be designed with negligible thermal noise, making them suitable for sub-threshold electroluminescence imaging. The electroluminescence image can be used to determine the spatial location of the emission. Emission patterns from degraded VCSELs are often non-uniform patterns, but they correlate well to Laser Scan Microscope (LSM) data.



Below Threshold

Above Threshold

Here we show an example set of EL images from a degraded VCSEL. The below-threshold images are on the left, and the above-threshold image is on the right. This set of images indicates the problem is in the contact.



In this example, we show electroluminescence images from a VCSEL. The image at the upper image shows a VCSEL from an optical system with a degraded output pattern under all bias conditions. We are imaging the sample using 35 microamps of current in a forward biased condition under a full optical spectral range. The EL image confirms that the problem is in the active region, based on the changes in intensity in the active region. The lower image also shows a VCSEL from an optical system with degraded output under lasing conditions, but this sub-threshold EL image confirms that the active junction is not degraded. In this case, the problem was with the distributed Bragg Reflectors elsewhere in the optical system.

Ask the Experts

Q: Is there a reason not to have a 90° bend in an RDL trace?

A: Yes, sometimes sharp bends can produce reflections and changes in transmission coefficients. There are a variety of techniques to minimize these effects, including: using 45 degree bends in traces, cropping corners at 45 degrees, using notches or other physical structures to reduce reflections, and using curved RDL traces.

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Spotlight: Advanced Device Physics

Semiconductor device physics is fundamental to understanding the operation of today's integrated circuits. This course offers an in-depth look into how semiconductors operate at a fundamental level. This is a detailed course that will help the student understand the physics of semiconductor materials; and the equations used to describe the operation of pn junctions, bipolar junction transistors, and Metal Oxide Semiconductor (MOS) transistors. We also cover many of the non-ideal effects associated with these devices, such as parasitic resistance and capacitance, bipolar effects like the Early Effect and the Kirk Effect, as well as MOS transistor effects like channel length modulation and punch-through.

This course is authored by Badih El-Kareh PhD, a 40-year industry veteran with work experience at IBM, Texas Instruments, and numerous other companies through his consulting firm PIYE. He is an award-winning developer of CMOS, BiCMOS, Bipolar and memory processes that are still in high volume production to this day.

Please note that this is Part One of a two-part course. The second part will be available in early 2021. We will make the second part available to our early subscribers of Part One for no additional charge once it becomes available. For more information on how to subscribe to Part One of this course, please click here: https://www.semitracks.com/online-training/premium-courses/advanced-device-physics

Presentations:

1.1 Properties of the Silicon Crystal

1.2 Two-Carrier Concept and Doping

1.3 Distribution of Electrons and Holes in Silicon

1.4 The Conduction Process

1.5 Test Structures and Characterization

Quiz: Properties of the Silicon Crystal

2.1 Fabrication of a PN Junction

2.2 PN Junction at Thermal Equilibrium

2.3 PN Junction in Forward Bias

2.4 PN Junction in Reverse Bias

2.5 Characterization of PN Junctions

3.1 Rectifying Contacts, Schottky-Barrier Diode

3.2 SBD Characterization and Applications

3.3 Ohmic Contacts

4.1 Introduction to Bipolar Junction Transistors
4.2 Bipolar Junction Transistor DC Parameters
4.3 Graded Base and High Current and High-Level Injection
4.4 Frequency Response and Transistor Switching
4.5 Advanced Bipolar Transistors
4.6 Characterization of Bipolar Transistors

5.1 Junction Field-Effect Transistor
5.2 The MOS Structure
5.3 Surface Effects on PN Junctions
5.4 Introduction to MOSFETs
5.5 MOSFET Characteristics
5.6 Nonuniform Channels and Small Size MOSFET Effects
5.7 Advanced MOSFET Technologies
5.8 Complementary Metal Oxide FETs, CMOS

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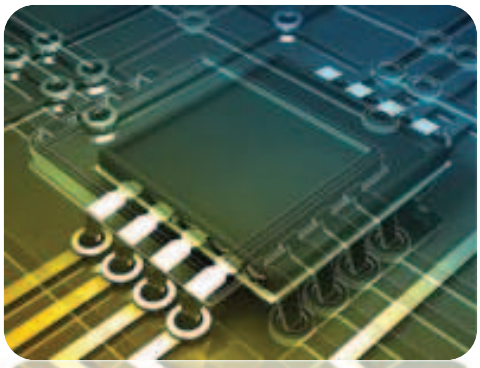

Upcoming Courses

(Click on each item for details)

Due to the CoronaVirus, the dates for these courses are in the process of being rescheduled. For questions about courses, please contact us at info@semitracks.com

Wafer Fab Processing
Date To Be Determined
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Semiconductor Reliability / Product Qualification
Date To Be Determined
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IC Packaging Technology
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