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InfoTracks

Semitracks Monthly Newsletter

Overview of Statistical Process Control Part 4

By Christopher Henderson

In part 4 of our discussion of statistical process control, we continue with our overview of process monitoring and control. We also discuss the process capability indices.

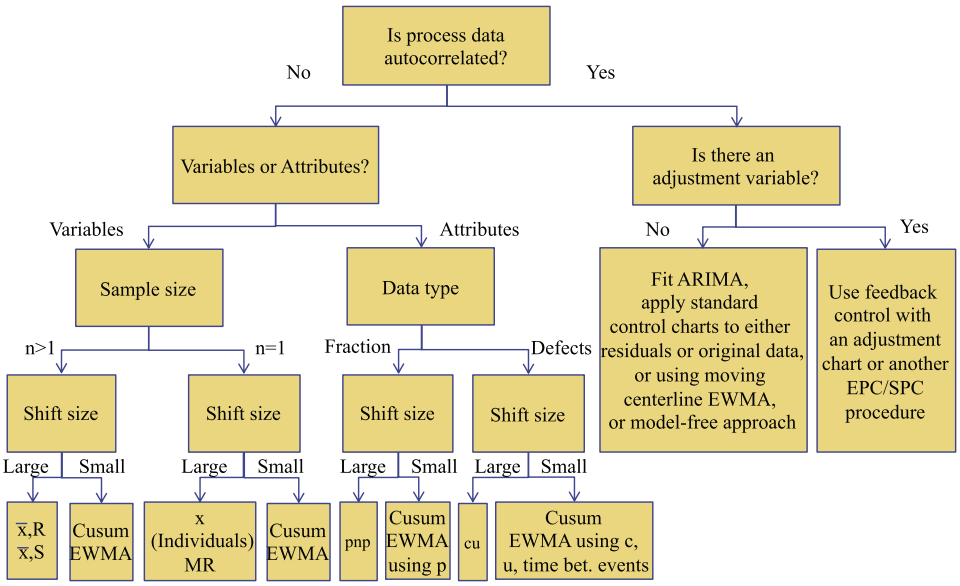

Figure 14. Process monitoring and control.

In summary, we can use a variety of plots to examine and control our manufacturing process. But which method is best? This table in Figure 14 provides a place to start. It's not a perfect way to make your

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decisions, but will give you a good place to start. In this table we use several acronyms. ARIMA stands for Autoregressive Integrated Moving Average, EPC standard for Engineering Process Control, and SPC of course stands for Statistical Process Control.

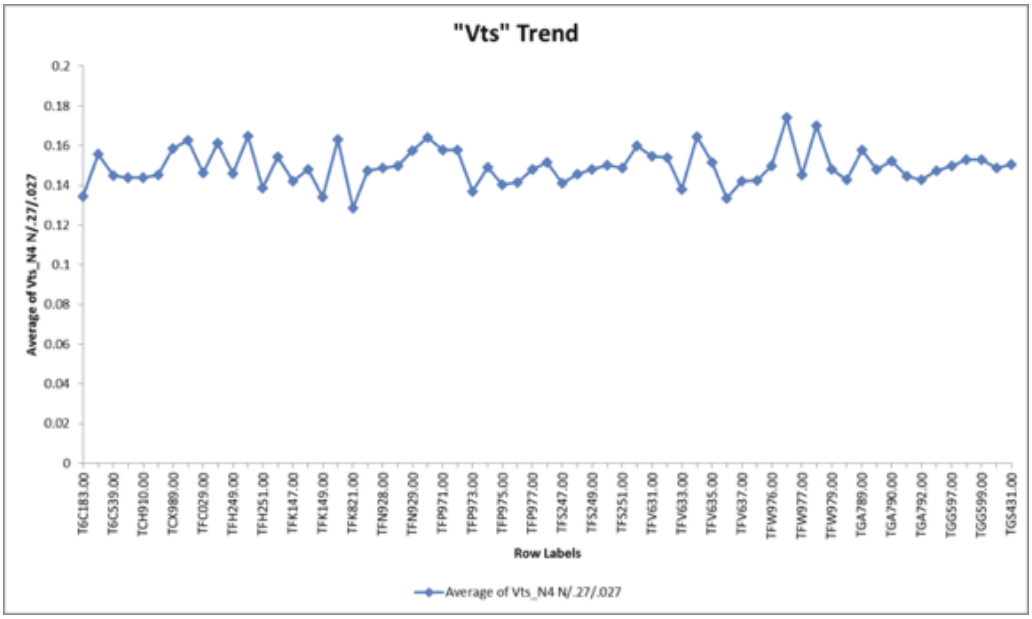


Figure 15. Statistical Process Control (SPC) chart example.

As an example, in Figure 15 we show an example Statistical Process Control Chart. This can be done in time, or by lot number. We also refer to these types of charts as trend charts.

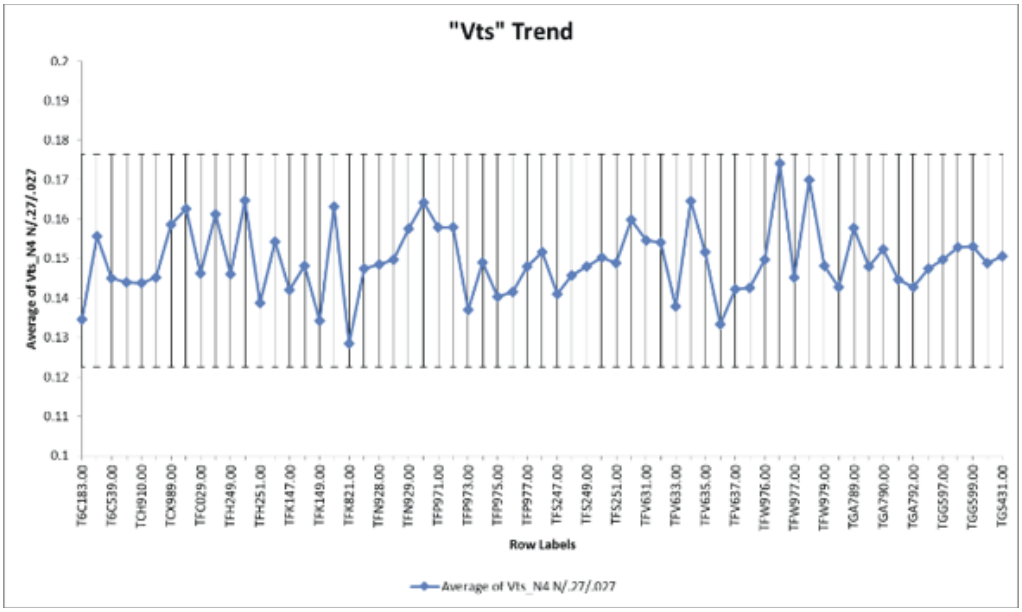


Figure 16. Statistical Process Control (SPC) chart example with limits.

In Figure 16 we show the same SPC chart as in Figure 15, but with limits shown as error bars. In this case we can see that the process is in control.

Process Capability Index or Cpk is an important topic for Product and Manufacturing Engineers to know. Cpk is an index in the form of a simple number which measures how close a process is running to its specification limits relative to the natural variability of the process. The Cpk index is part of a series of indices that measure how much natural variation a process experiences relative to its specification limits, and permits the engineer to compare different processes to one another with respect to their overall control. The larger the index number, the less likely any particular data point will be outside the specification limits. However, a large index is not necessarily a good thing, so engineers may tighten the limits if there is a large Cpk. If Cpk is too large, one never sees an indication that prompts action to fix or optimize the process.

Calculations	Description
$C_p = \frac{USL - LSL}{6\sigma}$	Estimates what the process is capable of producing if the process mean were to be centered between the specification limits. Assumes process output is approximately normally distributed.
$C_{p,lower} = \frac{\mu - LSL}{3\sigma}$	Estimates process capability for specifications that consist of lower limit only (e.g., strength). Assumes process output is approximately normally distributed.
$C_{p,upper} = \frac{USL - \mu}{3\sigma}$	Estimates process capability for specifications that consist of upper limit only (e.g., concentration). Assumes process output is normally distributed.
$C_{pk} = min\left[\frac{USL - \mu}{3\sigma}, \frac{\mu - LSL}{3\sigma}\right]$	Estimates what the process is capable of producing, considering that the process mean may not be centered between the specification limits. (If the process mean is not centered, $\hat{C}_p$ overestimates process capability.) $\hat{C}_{pk}$<0 if the process mean falls outside of the specification limits. Assumes process output is approximately normally distributed.
$C_{pm} = \frac{C_p}{\sqrt{1 + \left(\frac{\mu - T}{\sigma}\right)^2}}$	Estimates process capability around a target, T. $\hat{C}_{pm}$ is always greater than zero. Assumes process output is approximately normally distributed. $\hat{C}_{pm}$ is also known as the Taguchi capability index.
$C_{pkm} = \frac{C_{pk}}{\sqrt{1 + \left(\frac{\mu - T}{\sigma}\right)^2}}$	Estimates process capability around a target, T, and accounts for an off-center process mean. Assumes process output is approximately normally distributed.

Figure 17. Process capability indices.

This table in Figure 17 describes the process capability indices and the equations to calculate them. Although there are a number of indices, Cpk is the most popular. Process capability indices assume that one is dealing with normally distributed data, and that may not always be the case. It's important to remember though that some data might have an upper bound, but no lower bound, or vice-versa. An example of this might be quiescent power supply current (IDDQ), or maximum frequency (Fmax). IDDQ typically has an upper bound but no lower bound, whereas Fmax typically has a lower bound but no upper bound.

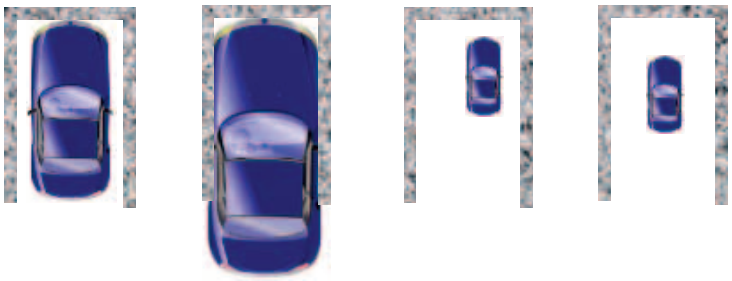


Figure 18. Cpk analogy example.

Let's use a car and a garage as an analogy. The garage will define the specification limits, and the car will define the output of the process. We show four scenarios with cars and garages. If my car is only a little bit smaller than the garage, then I need to park it right in the middle of the garage (center of the specification) if you want to get all of the car in the garage. This is similar to a Cpk of 1. It is a marginal outcome. If my car is wider than the garage, it does not matter how I try to center it, because it will not fit. This is similar to a Cpk of less than 1. It is an unacceptable outcome. If my car is a lot smaller than the garage, it doesn't matter if I park it exactly in the middle, because it will fit and have plenty of room on either side. This is similar to a Cpk of greater than 1. If I can always park my smaller car in the center and with little variation, then this is equivalent to the highest Cpk value, or a value that is much greater than 1. Cpk describes the relationship between the size of the car, the size of the garage, and how far away from the middle of the garage I parked the car.

Cpk Value		Acceptance
<1.00	$< 3\sigma/3\sigma$	Unacceptable
1.00	$3\sigma/3\sigma$	Marginal
1.33	$4\sigma/3\sigma$	OK
1.67	$5\sigma/3\sigma$	Good
2.00	$6\sigma/3\sigma$	Excellent
>2.00	$> 6\sigma/3\sigma$	

Figure 19. Acceptable and unacceptable values.

So what is an acceptable value? Clearly, values that are below 1 will be unacceptable, and a value of 1 will be marginal, but what about larger values? In general, in semiconductor manufacturing we would like to see values equal to or greater than 2.00. This would constitute excellent process capability. A value of 1.33 would be acceptable, and a value of 1.67 would be good. These numbers will obviously vary depending on the process and the type of testing performed to generate the data. Some procedures like trim tests will have lower Cpks, but that is not necessarily a problem, as the purpose of trimming is to improve Cpk.

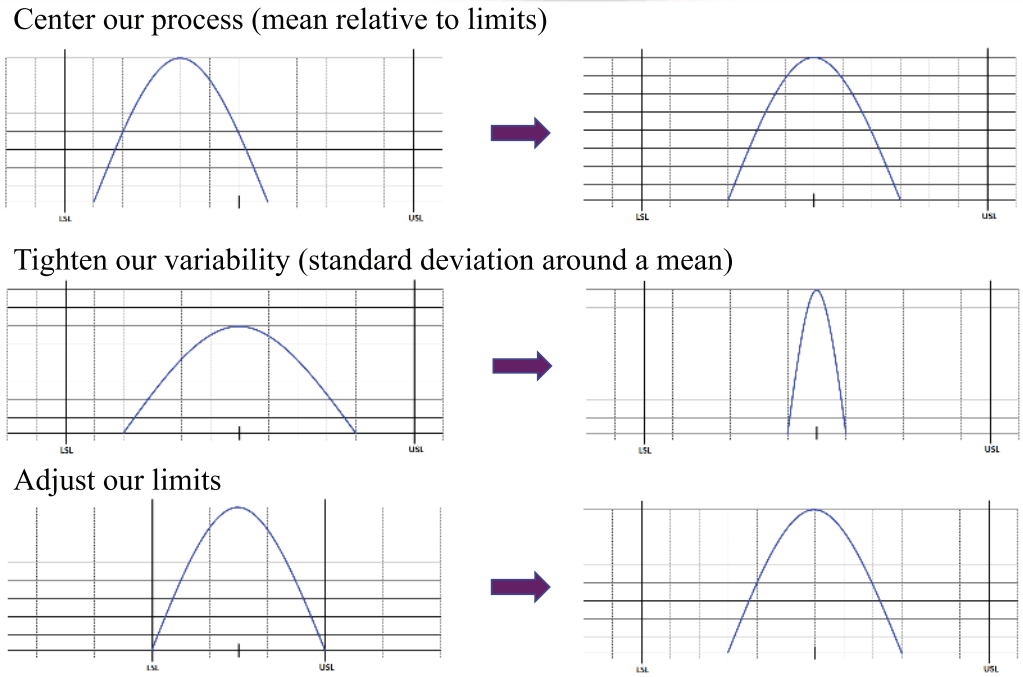


Figure 20. Improving Cpk value.

So what can we do to improve a Cpk value? In order, we should first try to center the process relative to the upper and lower statistical limits. Next, we should try and tighten our process such that it exhibits less variability. Third, we could consider adjusting our limits, but this is only something to do if all else fails with the first two options.

A parameter closely related to Cpk is Ppk, or process performance index. This is an estimate of the process capability of a process during its initial setup, before it is in a state of statistical control.

$$P_{pk} = min\left[\frac{USL-\mu}{3\sigma}, \frac{\mu-LSL}{3\sigma}\right]$$

Like Cpk, Ppk is calculated with the same basic equation, the minimum of the USL minus the mean over 3σ and the mean minus the LSL over 3σ. Like Cpk, Ppk values can have upper or lower limits missing.

$$P_{p,lower} = \frac{\mu-LSL}{3\sigma} \qquad P_{p,upper} = \frac{USL-\mu}{3\sigma}$$

Technical Tidbit

Solder Bump Electromigration

This month's technical tidbit discusses solder bump electromigration. Solder bump electromigration is a growing concern, as many new IC designs use Wafer Level Chip Scale Packaging (WLCSP) processes. ICs that draw higher levels of current, such as power management ICs, can lead to increased failure rates in the solder bumps.

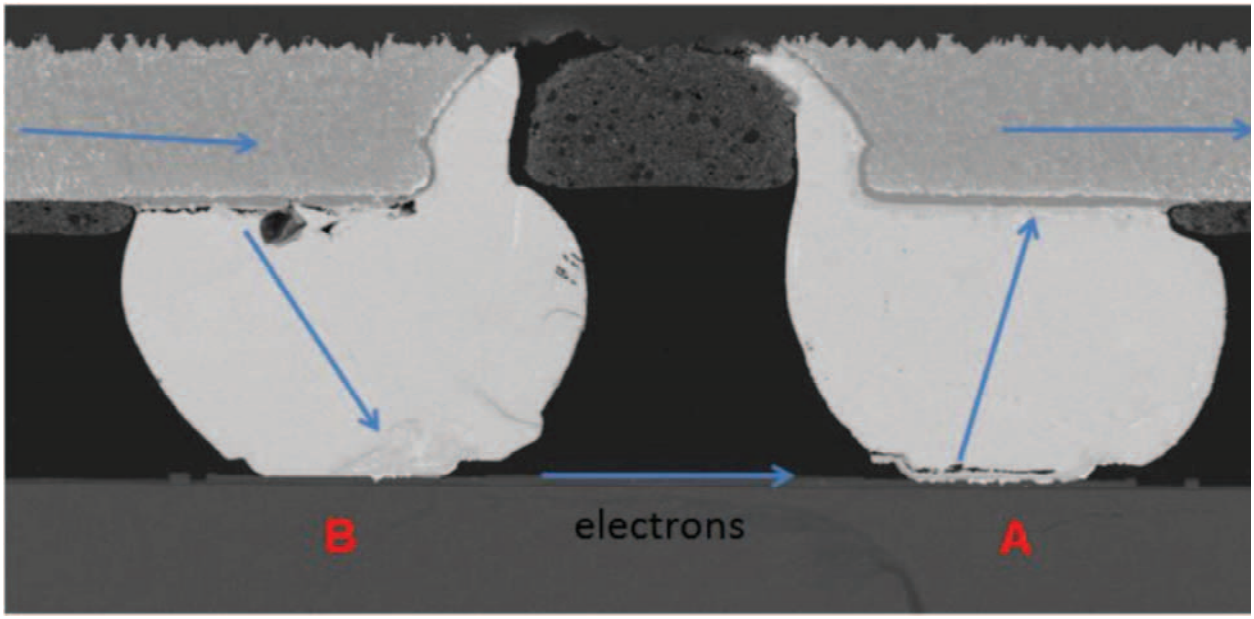


Figure 1.

Electromigration is a concern at the interface between the solder bump and the Printed Circuit Board (PCB) pad metallization, as well as the interface between the IC Under Bump Metallization (UBM) layer and the solder bump. Figure 1 shows voiding in a test chip at both the PCB pad/solder joint interface, and the UBM/solder joint interface. Voiding is the primary concern, although pileup of material at the opposite interface could lead to shorting.

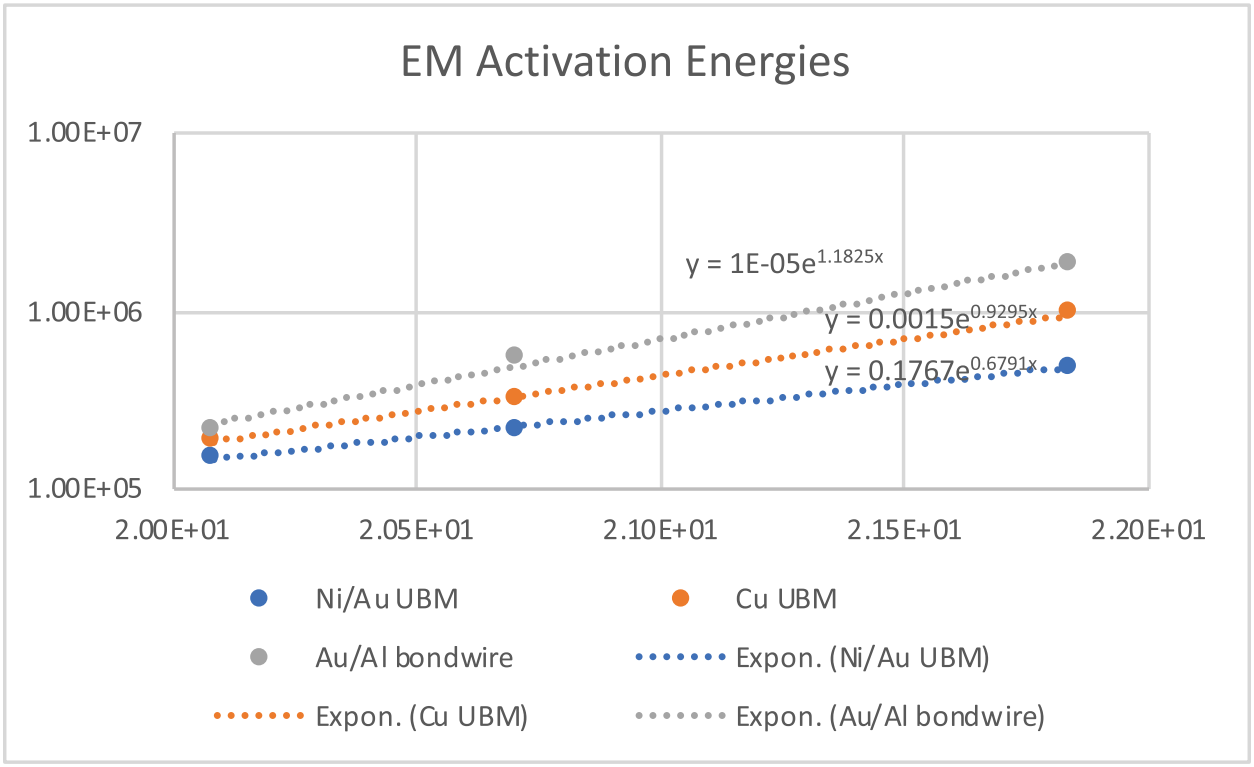


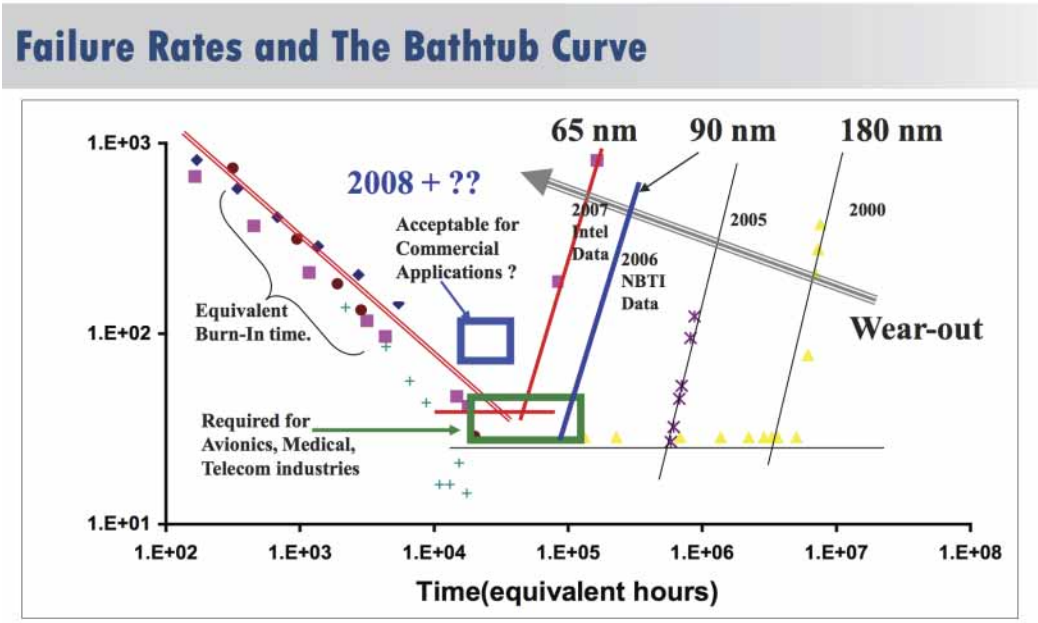
Figure 2.

The activation energies vary significantly, depending on the metal interface. In this example in Figure 2, we show a graph of the Mean Time to Failure (MTTF) as a function of 1/KT. We have plotted the data in such a manner that the slope of the lines approximates the activation energies. We show the activation energies for a Ni/Au UBM, a Cu UBM, and an Au/Al bondwire interface for comparison purposes. Notice that the activation energy for the Ni/Au UBM is lower, around 0.68eV, and the activation energy for the Cu UBM is higher, around 0.93eV. The Au/Al interface is approximately 1.18eV. This would indicate that a Cu UBM will provide better electromigration solder joint performance.

Ask the Experts

Q: Is there any data showing the behavior of the right side of the Bathtub Curve?

A: There isn't a lot of published data, but Craig Hillman of DfR Solutions (now part of ANSYS) has given presentations showing data from Intel regarding this curve (see the graph nearby). One definitely sees a trend toward shorter lifetimes with more advanced technologies.



Spotlight: Introduction to Processing

OVERVIEW

Semiconductor and integrated circuit developments continue to proceed at an incredible pace. The industry as a whole has gotten to this point of incredible complexity through the process of countless breakthroughs and developments in wafer fab processing. Today's wafer fab contains some of the most complex and intricate procedures ever developed by mankind. ***Introduction to Processing*** is a 2-day course that offers an overview look into the semiconductor manufacturing process, and the individual processing technologies required to make them. We place special emphasis on the basics surrounding each technique, and we summarize the current issues related to manufacturing the next generation devices. This course is a must for every manager, engineer and technician working in the semiconductor industry, using semiconductor components or supplying tools to the industry.

By focusing on the basics of each processing step and the issues surrounding them, participants will learn why certain techniques are preferred over others. Our instructors work hard to explain how semiconductor processing works without delving heavily into the complex physics and mathematical expressions that normally accompany this discipline.

Participants learn basic but powerful aspects about the semiconductor industry. This skill-building series is divided into three segments:

1. **Basic Processing Steps.** Each processing step addresses a specific need in IC creation. Participants learn the fundamentals of each processing step and why they are used in the industry today.
2. **The Evolution of Each Processing Step.** It is important to understand how wafer fab processing came to the point where it is today. Participants learn how each technique has evolved for use in previous and current generation ICs.
3. **Current Issues in Wafer Fab Processing.** Participants learn how many processing steps are increasingly constrained by physics and materials science. They also learn about the impact of using new materials in the fabrication process and how those materials may create problems for the manufacturers in the future.
4. **Current Issues in Assembly and Packaging.** Participants learn how packaging is a key enabler for semiconductor components. They also learn why we are seeing an explosion of different packaging types.

COURSE OBJECTIVES

1. The seminar will provide participants with an overview of the semiconductor industry and its technical issues.
2. Participants will understand the basic concepts behind the fundamental wafer fab processing steps.
3. The seminar will identify the key issues related to each of the processing techniques and their impact on the continued scaling of the semiconductor industry.
4. Participants will be able to identify the basic features and principles associated with each major processing step. These include processes like chemical vapor deposition, ion implantation, lithography, and etching.

5. Participants will understand how processing, reliability, power consumption and device performance are interrelated.
6. Participants will be able to make decisions about how to construct and evaluate processing steps for CMOS, BiCMOS, and bipolar technologies.
7. The seminar will provide an introduction to the packaging process and discuss the fundamental drivers behind the current developments in packaging.

INSTRUCTIONAL STRATEGY

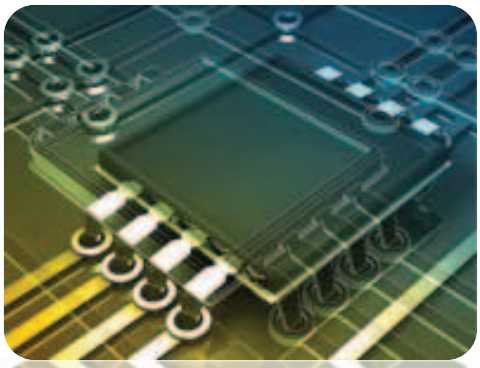
By using a combination of instruction by lecture, classroom exercises, and question/answer sessions, participants will learn practical information on semiconductor processing and the operation of this industry. From the very first moments of the seminar until the last sentence of the training, the driving instructional factor is **application**. We use instructors who are internationally recognized experts in their fields that have years of experience (both current and relevant) in this field. The accompanying textbook offers hundreds of pages of additional reference material participants can use back at their daily activities.

COURSE OUTLINE

1. Raw Silicon Wafers
2. Ion Implantation
3. Thermal Processing
4. Contamination Monitoring and Control
5. Wafer Cleaning and Surface Preparation
6. Chemical Vapor Deposition
7. Physical Vapor Deposition
8. Lithography
9. Etch
10. Chemical Mechanical Polishing
11. Cu Interconnect and low-k Dielectrics
12. Leading Edge Technologies and Techniques
    a. ALD
    b. High-k gate and capacitor dielectrics
    c. Metal gates
    d. SOI
    e. Strained silicon
    f. Plasma doping

13. Overview of Semiconductor Packaging
    a. Purpose of the package
    b. Drivers
    c. Types of Packages
    d. Packaging Processes

For each of these modules, the following topics will be addressed:
1) fundamentals necessary for a basic understanding of the technique
2) its role(s) and importance in contemporary wafer fab processes
3) type of equipment used
4) challenges
5) trends



Upcoming Courses

(Click on each item for details)

Failure and Yield Analysis
July 8 – 11, 2019 (Mon – Thur)
Singapore

Semiconductor Reliability / Product Qualification
July 15 – 18, 2019 (Mon – Thur)
Singapore

Introduction to Processing
July 23 – 24, 2019 (Tue – Wed)
Singapore

Wafer Fab Processing
April 14 – 17, 2020 (Tue – Fri)
Munich, Germany

Semiconductor Reliability / Product Qualification
April 14 – 17, 2020 (Tue – Fri)
Munich, Germany

Failure and Yield Analysis
April 20 – 23, 2020 (Mon – Thur)
Munich, Germany

IC Packaging Technology
April 27 – 28, 2020 (Mon – Tue)
Munich, Germany

Advanced CMOS/FinFET Fabrication
April 30, 2020 (Thur)
Munich, Germany

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To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered in the next newsletter, please contact Jeremy Henderson by Email (jeremy.henderson@semitracks.com).
We are always looking for ways to enhance our courses and educational materials.

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We look forward to hearing from you!