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Oxidation Part 1

By Christopher Henderson

In this new series, we will discuss the subject of oxidation. Oxidation is a key aspect of the semiconductor process. The fact that one can easily grow an oxide on top of a silicon wafer is one of the main reasons that the industry has been able to make cheap, reliable semiconductor components. We will discuss the following topics. First, we will discuss oxidation kinetics. These are the physical properties associated with the process of oxidation. We'll cover the process of oxidation, the theory behind oxidation and the Deal/Grove model of oxidation, and the equipment used for oxidation. Next, we will discuss the factors that affect oxidation. We'll talk briefly about the properties of the silicon/silicon dioxide interface and oxide traps. Next, we'll discuss oxidation systems in more detail. And finally, we'll end with a brief discussion of future gate dielectric materials. We begin with oxidation kinetics in this month's article.

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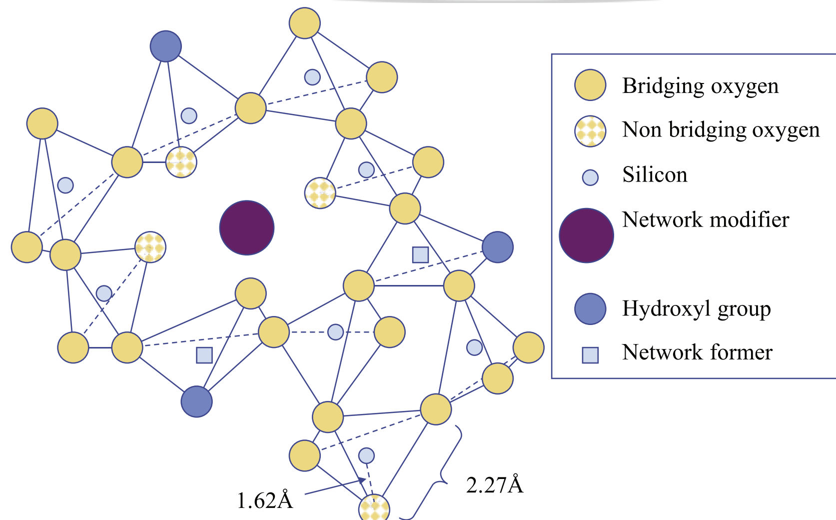


Figure 1. Properties of silica glass.

The glass or amorphous state of silicon dioxide is called fused silica. This state is not thermally stable below about 1700°C. This means that it will slowly convert into a crystalline form. The good news is that this process is so slow below 1000°C that for all intents and purposes, it does not occur. The structure of fused silica glass is moderately complex, as evidenced by the image shown here. Basically, the structure is composed of units of one silicon atom and four oxygen atoms loosely bound together by the oxygen atoms. There are bridging and non-bridging oxygen atoms in the structure. The distance between the silicon atom and the oxygen atoms is 1.62 Angstroms, while the distance between oxygen atoms is 2.27 Angstroms. The network formers are the doping species like phosphorus and boron. Network modifiers are the mobile ionic species like sodium, potassium, and lead. Because this structure is quite loose, various deposition conditions can lead to various properties.

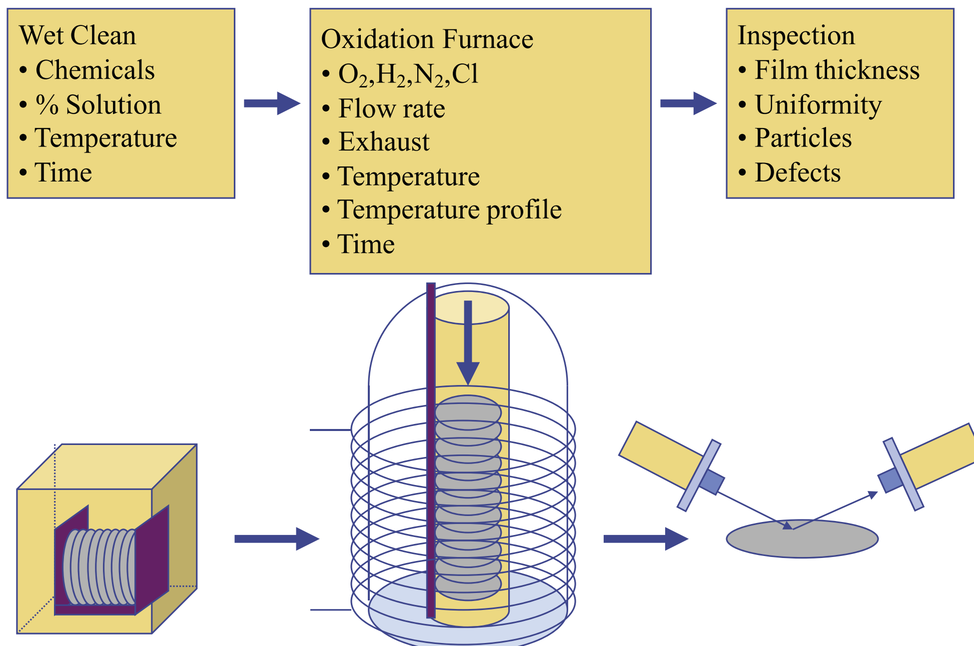


Figure 2. Thermal oxidation process sequence.

This diagram shows an overview of the thermal oxidation process. Before oxidation begins, the wafers are cleaned using a prescribed procedure. Next, the wafers are placed in the oxidation furnace. Gases such as oxygen, hydrogen, nitrogen, and chlorine might be introduced to achieve different growth rates, stoichiometry, and properties. Other parameters such as flow rate, exhaust rate, temperature, the temperature profile and time can be used to obtain a particular thickness or quality to the oxide. After the oxidation is complete, the oxide layer is inspected for film thickness, uniformity, particles or other types of defects.

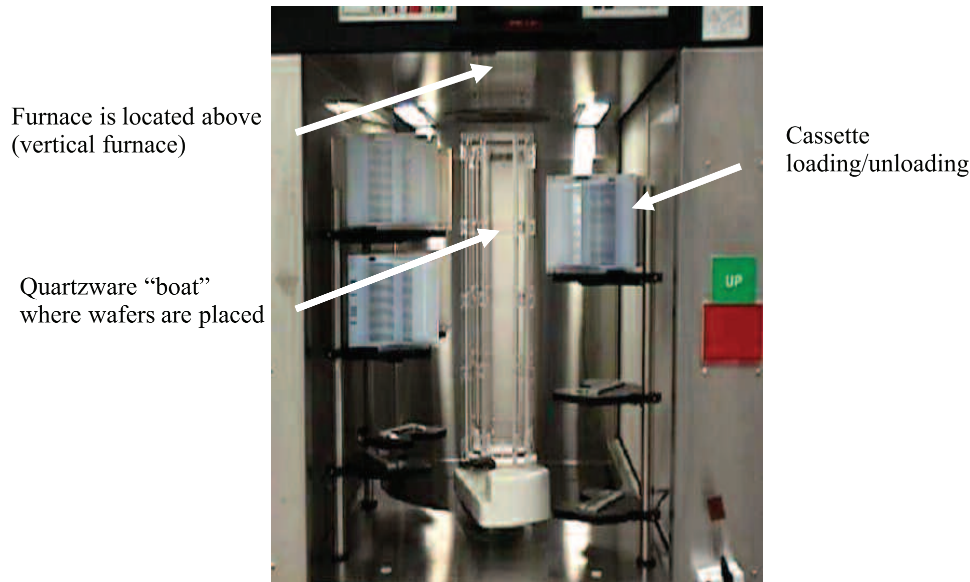


Figure 3. Vertical oxidation furnace.

This image shows an example of an oxidation furnace. This particular furnace is a vertical furnace. Most furnaces manufactured today are vertical furnaces, since the temperature profiles can be more easily controlled. Vertical furnaces also take up less room inside the clean room. Given the high cost of clean room space, this makes the vertical furnace the preferred tool. The quartzware rack where the wafers sit during the oxidation process is indicated by the red arrow. The quartzware is often referred to as a boat, since it is shaped much like a boat hull. The cassette mechanism for loading and unloading wafers is indicated by the green arrow. The cassettes are normally made from a material that does not easily generate particles, like teflon.

The oxidation process is used for several key steps in the manufacture of a semiconductor device. Probably the most important step is the gate dielectric. The gate dielectric is the foundation of the MOS transistor. In order to create state-of-the-art, functional integrated circuits one must be able to grow a high-quality gate dielectric. Oxidation is also used to form the isolation between transistors. The LOCOS—or Local Oxidation of Silicon—process relies on oxidation to form the silicon dioxide isolation layer. Oxidation is also used in the shallow trench isolation process to create the oxide layers on the sidewalls of

the trench. Oxidation is used to mask for ion implantation. It is also used to grow a feature called a pad oxide that provides stress relief between the silicon and silicon nitride layers. Oxidation is also used to create tunnel oxides, capacitor dielectrics, and sacrificial oxide layers.

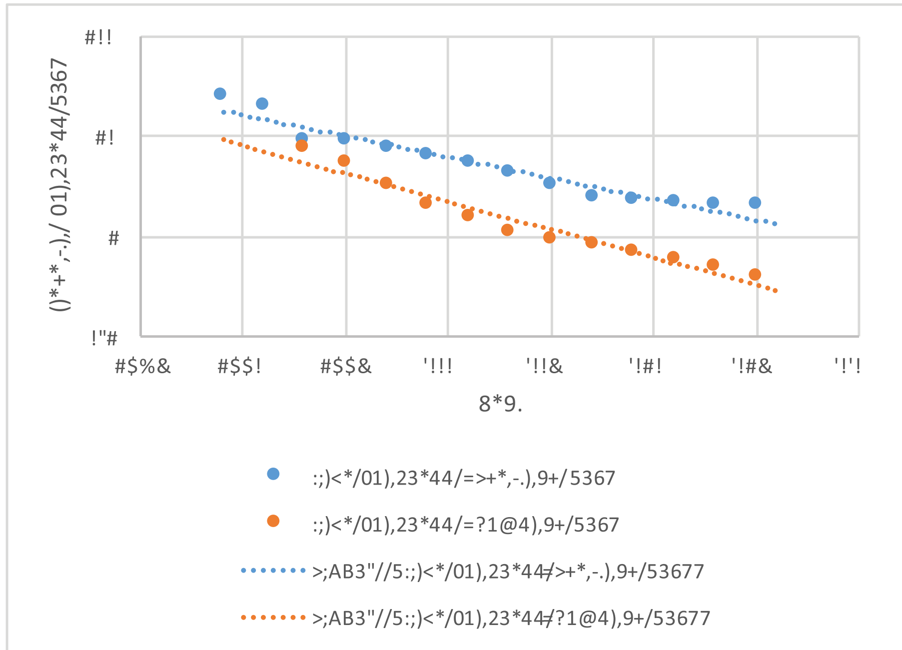


Figure 4. Gate dielectric thickness trends.

As Moore's Law continues, the thickness of the gate oxide has continued to decrease. This data shows the gate oxide thickness as a function of technology. In 1989 at the 1.2μm feature size, the gate oxide thickness was approximately 20 nanometers. By 2003 at the 90nm feature size, the gate oxide thickness was approximately 1.2nm or 12 Angstroms. By 2005 we were rapidly approaching the situation where the gate oxide thickness was on the order of just a few layers of atoms. Although silicon dioxide has been an excellent gate dielectric, it has been replaced in the last few years.

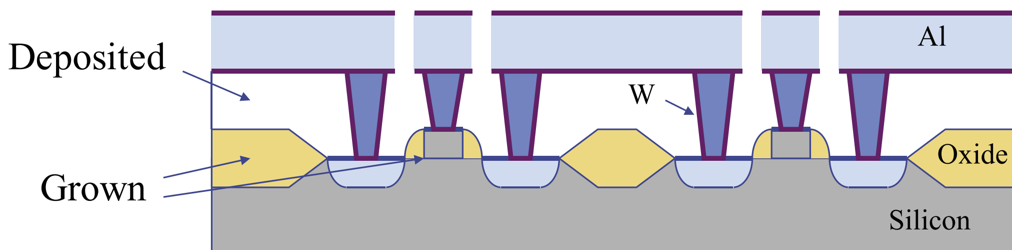


Figure 5. SiO_2 formation.

The process of silicon dioxide formation is straightforward. One exposes the silicon surface to an oxidizing environment at high temperatures. The environment might consist of oxygen, or steam might be used to accelerate the growth process. High temperatures also help to accelerate the process, allowing moderately thick films of up to 1μm to be grown in a time frame of several hours or less. The results are

reproducible, and the oxide film can be quite uniform. When we discuss thermal oxidation, we are talking about grown oxides as opposed to deposited oxides. Grown oxides are in direct contact with the silicon surface, while deposited oxides are used at higher levels in the process, like interlevel dielectrics.

Item	Value
Melting point (^oC)	~ 1600
Density (g/cm^3)	2.2 (6.6 x 10^{22} atoms/cm^3)
Refractive index	1.46
Dielectric constant	3.9
Band gap (eV)	9
Si/SiO_2 Barrier (eV)	3.1 for electrons, 4.6 for holes
Dielectric strength (V/cm)	10^7 (10 V for 100 Å oxide)
Stress (on Si) (Mpa)	< 400
Thermal expansion coefficient ($^oC^{-1}$)	5 x 10^{-7}
Thermal conductivity (W/cm-K)	0.014
DC resistivity (Ω-cm)	10^{14} ! 10^{16}
Etch rate in buffered HF (Å/min)	1000
Note: Buffered HF 34.6% (wt.) NH_4F, 6.8% (wt.) HF, 58.6% H2O	

Figure 6. Properties of SiO_2.

Here are some of the more common properties of silicon dioxide. As we mentioned earlier, its structure is amorphous and dependent on the oxidation conditions. It has a very high melting point and low density. The bandgap of silicon dioxide is rather high, making it a formidable barrier to electrons as well as holes. The resistivity of an oxide layer is quite high, ranging from 10 to the 14 up to 10 to the 18 ohms per centimeter. Thermally grown oxide can be removed using a buffered hydrofluoric acid etch. A standard etch (listed at the bottom of the table) will remove approximately 1000 Angstroms per minute.

Here is a breakdown of the pre-oxidation steps. First, wafers undergo a series of wet cleaning processes. The first of these cleans is the Piranha etch. This is an aggressive etch that removes organic contamination and particles. The next clean is the standard clean one or SC-1. This etch removes particles. This is followed by an SC-2 clean which removes inorganic contaminants. This is followed by a quick etch in hydrofluoric acid to remove the native oxide that grows during normal storage conditions. The wafers are then loaded immediately into the furnace for the oxidation process. The growth of the oxide occurs right at the silicon/silicon dioxide interface. Initially, the rate of the reaction is limited by the rate of the surface reaction. As the oxide layer grows, the reaction becomes limited by the diffusion of the oxygen to the silicon surface.

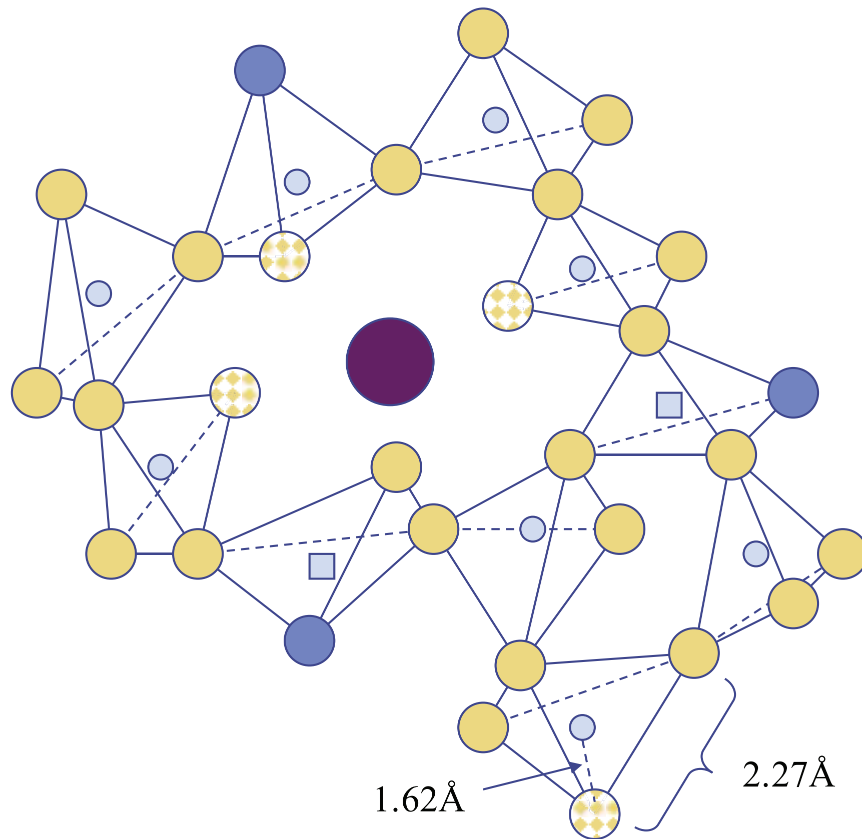


Figure 7. Formation of SiO_2.

As the silicon dioxide is formed, silicon bonds are broken at the surface of the silicon. Oxygen atoms insert themselves between the silicon atoms. The resulting silicon-oxygen bonds take up more room than the silicon-silicon bonds. This causes an expansion in the material. Silicon dioxide occupies 227% of the original space occupied by the silicon.

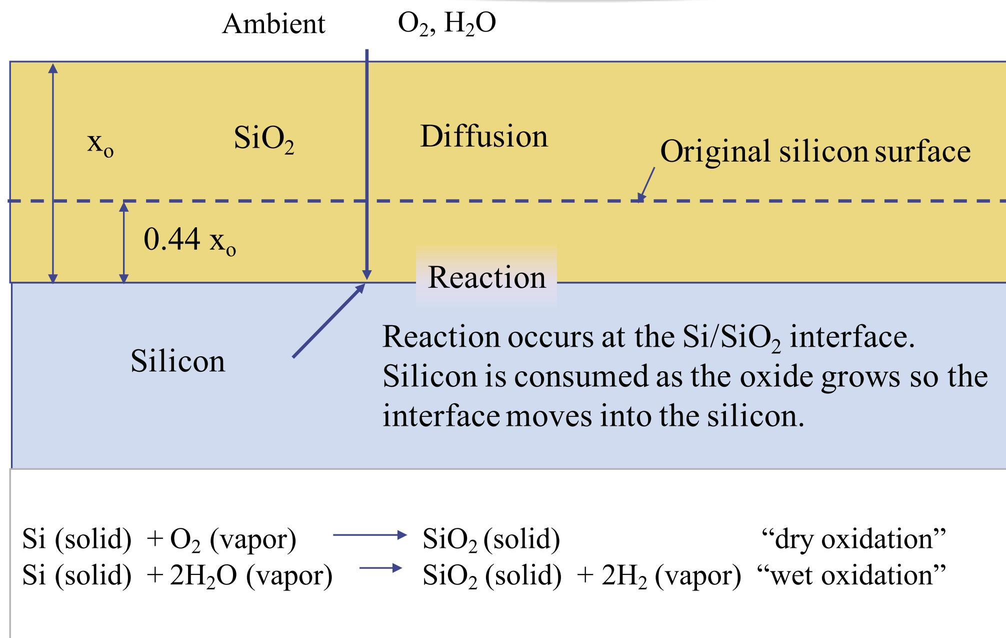
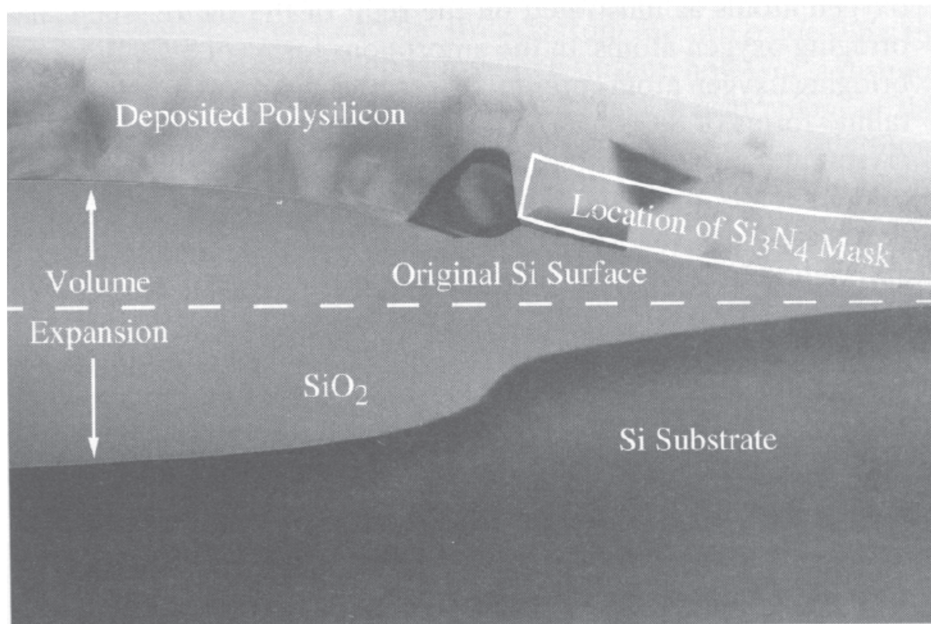


Figure 8. Oxidation kinetics.

This diagram shows the oxidation process. Oxygen from the oxygen or steam in the furnace diffuses through the oxide, reaching the silicon surface. Once at the silicon surface, the oxygen or steam reacts with the silicon, producing silicon dioxide. The reaction consumes the silicon, so the silicon/silicon dioxide interface moves into the silicon. As the oxide grows, the original silicon surface is at a point that is 44% of the thickness of the oxide. The reactions for both an oxygen-generated oxide and a steam-generated oxide are shown at the bottom. The steam reaction creates hydrogen gas. Hydrogen is a fast diffuser in silicon dioxide, so it rapidly diffuses out of the oxide.



Left: Figure 9. Example showing SiO_2 formation.

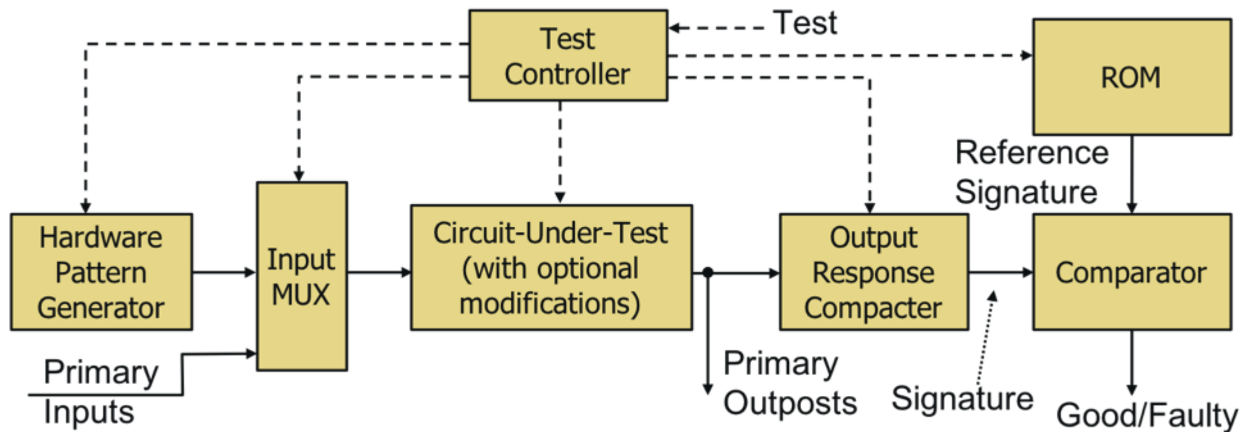
Figure 9 shows a cross-sectional image of the silicon dioxide growth. Notice that the silicon dioxide has consumed a portion of the silicon, expanding down into the silicon itself. The original silicon surface is shown by the dotted line. There is even some growth of the oxide beneath the edge of the silicon nitride mask.

To be continued in next month's issue.

Technical Tidbit

Basic Built-In Self Test Architecture

In this month's technical tidbit we will describe the basics of a Built-In Self Test (BIST) architecture. BIST is a common method for testing complex integrated circuits. BIST has the advantage that it reduces the complexity of the test system needed to test the IC. It also has the possibility of being able to exercise the IC under conditions that more closely approximate customer use conditions.



This figure shows a basic BIST architecture. A test controller controls the behavior of the built-in self test circuitry. The test controller can be activated externally through the "Test" pin. The test controller operates the hardware pattern generator. The hardware pattern generator can generate digital logic, or if one includes digital-to-analog converters, analog waveforms as well. The inputs from the hardware pattern generator are then multiplexed through an input multiplexer, where they become inputs to the circuit under test. The outputs of the circuit can either go to other functional circuits, or in the case of the BIST architecture, into the output response compactor. For a digital circuit, this might be a Linear Feedback Shift Register (LFSR). This signature can then be presented to the comparator to check against the value stored in memory. We should note that BIST cannot test wires and transistors from the primary input pins to the input multiplexor or from the primary outputs to the output pins, only circuits between the input multiplexor and the output response compactor. BIST can help reduce the cost of test, but the disadvantage is additional area and complexity.

Ask the Experts

Q: Does the bathtub curve work for situations where a component is in storage for a portion of its life?

A: The bathtub curve is designed to be a general concept for operating devices, whereas a component in storage describes a specific non-operating condition. With that said though, there are failure mechanisms that affect components in storage, so it is appropriate from a general perspective to think about the bathtub curve applying to components in storage, and not just components in operation.

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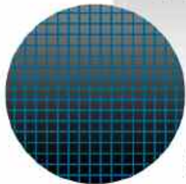

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Spotlight: Wafer Fab Processing

OVERVIEW

Semiconductor and integrated circuit developments continue to proceed at an incredible pace. The industry as a whole has gotten to this point of incredible complexity through the process of countless breakthroughs and developments in wafer fab processing. Today's wafer fab contains some of the most complex and intricate procedures ever developed by mankind. ***Wafer Fab Processing*** is a 4-day course that offers an in-depth look into the semiconductor manufacturing process, and the individual processing technologies required to make them. We place special emphasis on the basics surrounding each technique, and we delve into the current issues related to manufacturing the next generation devices. This course is a must for every manager, engineer and technician working in the semiconductor industry, using semiconductor components or supplying tools to the industry.

By focusing on the basics of each processing step and the issues surrounding them, participants will learn why certain techniques are preferred over others. Our instructors work hard to explain how semiconductor processing works without delving heavily into the complex physics and mathematical expressions that normally accompany this discipline.

Participants learn basic but powerful aspects about the semiconductor industry. This skill-building series is divided into three segments:

1. **Basic Processing Steps.** Each processing step addresses a specific need in IC creation. Participants learn the fundamentals of each processing step and why they are used in the industry today.
2. **The Evolution of Each Processing Step.** It is important to understand how wafer fab processing came to the point where it is today. Participants learn how each technique has evolved for use in previous and current generation ICs.
3. **Current Issues in Wafer Fab Processing.** Participants learn how many processing steps are increasingly constrained by physics and materials science. They also learn about the impact of using new materials in the fabrication process and how those materials may create problems for the manufacturers in the future.

COURSE OBJECTIVES

1. The seminar will provide participants with an in-depth understanding of the semiconductor industry and its technical issues.
2. Participants will understand the basic concepts behind the fundamental wafer fab processing steps.
3. The seminar will identify the key issues related to each of the processing techniques and their impact on the continued scaling of the semiconductor industry.
4. The seminar offers a wide variety of sample problems that participants work to help them gain knowledge of the fundamentals of wafer fab processing.
5. Participants will be able to identify the basic features and principles associated with each major processing step. These include processes like chemical vapor deposition, ion implantation, lithography, and etching.
6. Participants will understand how processing, reliability, power consumption and device performance are interrelated.

7. Participants will be able to make decisions about how to construct and evaluate processing steps for CMOS, BiCMOS, and bipolar technologies.

INSTRUCTIONAL STRATEGY

By using a combination of instruction by lecture, classroom exercises, and question/answer sessions, participants will learn practical information on semiconductor processing and the operation of this industry. From the very first moments of the seminar until the last sentence of the training, the driving instructional factor is **application**. We use instructors who are internationally recognized experts in their fields that have years of experience (both current and relevant) in this field. The accompanying textbook offers hundreds of pages of additional reference material participants can use back at their daily activities.

COURSE OUTLINE

Day 1

1. Module 1: Basics & Fundamentals; Semiconductor Devices and ICs
    a. Acronyms
    b. Common Terminology
    c. Brief History
    d. Semiconductor Materials
    e. Electrical Conductivity
    f. Semiconductor Devices
    g. Classification of ICs & IC Processes
    h. Integrated Circuit Types
2. Module 2: Crystallinity, Crystal Defects, Crystal Growth
    a. Crystallinity
    b. Crystal Defects
    c. Crystal Growth
    d. Controlling Crystal Defects
3. Module 3: Basic CMOS Process Flow
    a. Transistors and Isolation
    b. Contacts/Vias Formation
    c. Interconnects
    d. Parametric Testing
4. Module 4: Ion Implantation 1 (The Science)
    a. Doping Basics
    b. Ion Implantation Basics
    c. Dopant Profiles
    d. Crystal Damage & Annealing
5. Module 5: Ion Implantation 2 (Equipment, Process Issues)
    a. Equipment
    b. Process Challenges
    c. Process Monitoring & Characterization
    d. New Techniques

Day 2

6. Module 6: Thermal Processing
    a. Overview of Thermal Processing
    b. Process Applications of SiO2
    c. Thermal Oxidation
    d. Thermal Oxidation Reaction Kinetics
    e. Oxide Quality
    f. Atomistic Models of Thermal Diffusion
    g. Thermal Diffusion Kinetics
    h. Thermal Annealing
    i. Thermal Processing Hardware
    j. Process Control
7. Module 7: Contamination Monitoring and Control
    a. Contamination Forms & Effects
    b. Contamination Sources & Control
    c. Contamination Characterization & Measurement
8. Module 8: Wafer Cleaning
    a. Wafer Cleaning Strategies
    b. Chemical Cleaning
    c. Mechanical Cleaning
9. Module 9: Vacuum, Thin Film, & Plasma Basics
    a. Vacuum Basics
    b. Thin Film Basics
    c. Plasma Basics
10. Module 10: CVD 1 (Basics, LPCVD, Epitaxy)
    a. CVD Basics
    b. LPCVD Films
    c. LPCVD Equipment
    d. Epi Basics
    e. Epi Process Applications
    f. Epi Deposition Process
    g. Epi Deposition Equipment

Day 3

11. Module 11: PVD
    a. PVD (Physical Vapor Deposition) Basics
    b. Sputter Deposition Process
    c. Sputter Deposition Equipment
    d. Al-Based Films
    e. Step Coverage and Contact/Via Hole Filling
    f. Metal Film Evaluation
12. Module 12: Lithography 1 (Photoresist Processing)
    a. Basic Lithography Process
    b. Photoresist Materials

   c. Photoresist Process Flow
   d. Photoresist Processing Systems
13. Module 13: Lithography 2 (Image Formation)
   a. Basic Optics
   b. Imaging
   c. Equipment Overview
   d. Actinic Illumination
   e. Exposure Tools
14. Module 14: Lithgroaphy 3 (Registration, Photomasks, RETs)
   a. Registration
   b. Photomasks
   c. Resolution Enhancement Techniques
   d. The Evolution of Optical Lithography
15. Module 15: Etch 1 (Basics, Wet Etch, Dry Etch)
   a. Etch Basics
   b. Etch Terminology
   c. Wet Etch Overview
   d. Wet Etch Chemistries
   e. Types of Dry Etch Processes
   f. Physics & Chemistry of Plasma Etching

Day 4

16. Module 16: Etch 2 (Dry Etch Applications and Equipment)
   a. Dry Etch Applications
   b. SiO2
   c. Polysilicon
   d. Al & Al Alloys
   e. Photoresist Strip
   f. Silicon Nitride
   g. Dry Etch Equipment
   h. Batch Etchers
   i. Single Wafer Etchers
   j. Endpoint Detection
   k. Wafer Chucks
17. Module 17: CVD 2 (PECVD)
   a. CVD Basics
   b. PECVD Equipment
   c. CVD Films
   d. Step Coverage
18. Module 18: Chemical Mechanical Polishing
   a. Planarization Basics
   b. CMP Basics

c. CMP Processes
d. Process Challenges
e. Equipment
f. Process Control

19. Module 19: Copper Interconnect, Low-k Dielectrics
    a. Limitations of “Conventional” Interconnect
    b. Copper Interconnect
    c. Cu Electroplating
    d. Damascene Structures
    e. Low-k IMDs
    f. Cleaning Cu and low-k IMDs
20. Module 20: Leading Edge Technologies & Techniques
    a. Process Evolution
    b. Atomic Layer Deposition (ALD)
    c. High-k Gate and Capacitor Dielectrics
    d. Ni Silicide Contacts
    e. Metal Gates
    f. Silicon on Insulator (SOI) Technology
    g. Strained Silicon
    h. Hard Mask Trim Etch
    i. New Doping Techniques
    j. New Annealing Techniques
    k. Other New Techniques
    l. Summary of Industry Trends

References:

Wolf, Microchip Manufacturing,
Doering & Nishi, Semiconductor Manufacturing Technology, 2nd ed.
Wolf, Silicon Processing, Vol. 4
Wolf, Silicon Processing, Vol. 1, 2nd ed.

You may want to stress some aspects more than others or conduct a simple one-day overview course. Many of our clients seek ongoing just-in-time training that builds in-depth, advanced levels of reliability expertise. We’ll work with you to determine the best course of action and create a statement of work that emulates the very best practices of semiconductor reliability analysis.

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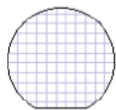

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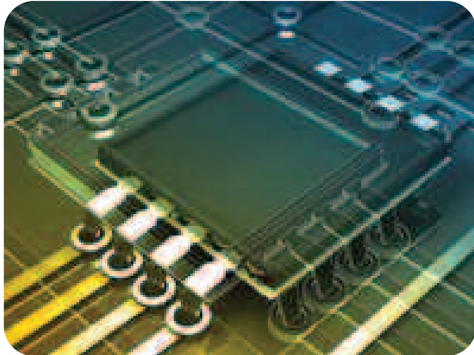

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