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Die Attach—Part III

By Christopher Henderson

Let's move on and discuss eutectic die attach. There are a number of different eutectic die attach materials; some of the more common ones include Au-Si, Au-Sn, Pb-Sn, and In-Sn. Die attach typically comes in a preform, since these materials melt at high temperatures. This image shows some examples of these die attach preforms.

Die attach preforms

Eutectic die attach can be quite useful in certain applications where the application requires higher reliability. Eutectic materials are typically more stable in high temperatures, don't have issues with outgassing, and can be picked to better match the coefficient of thermal expansion of the die and other packaging materials.

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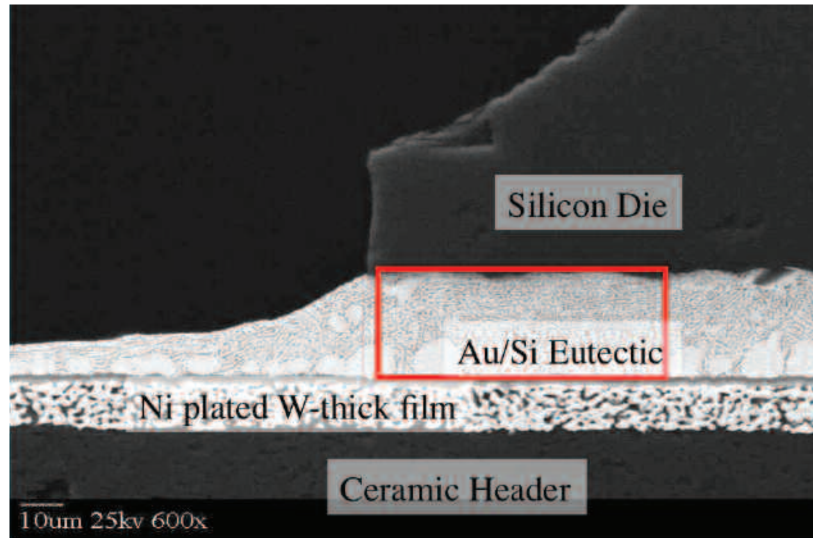
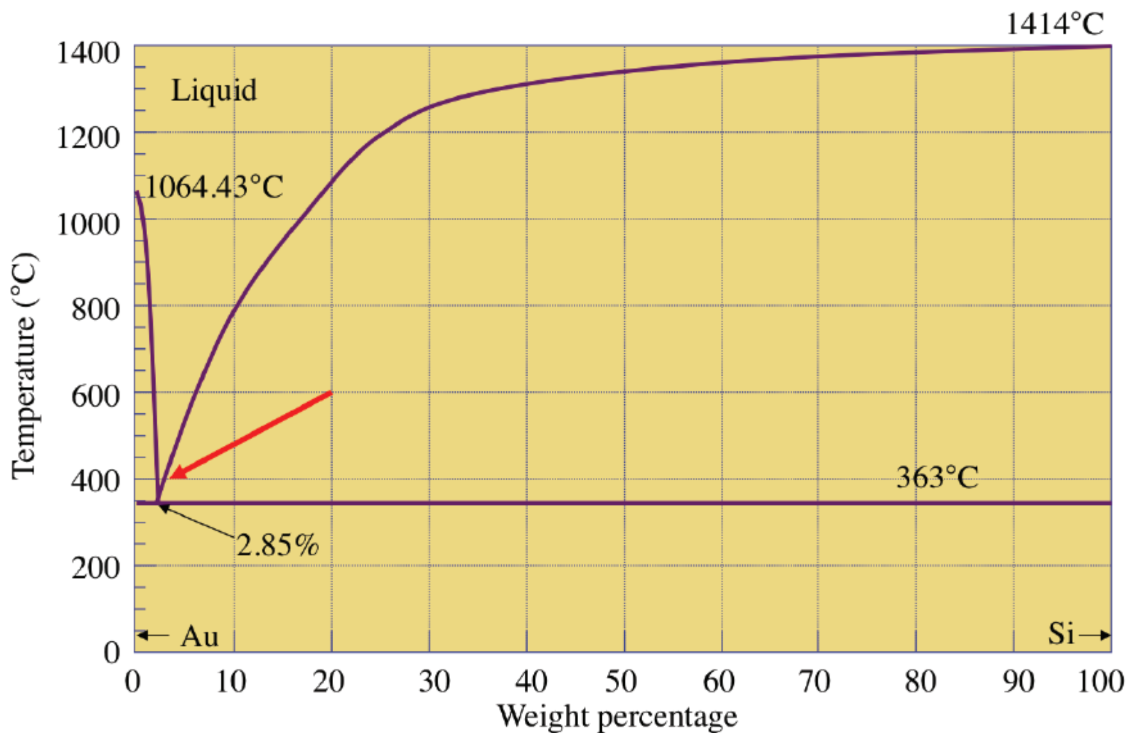
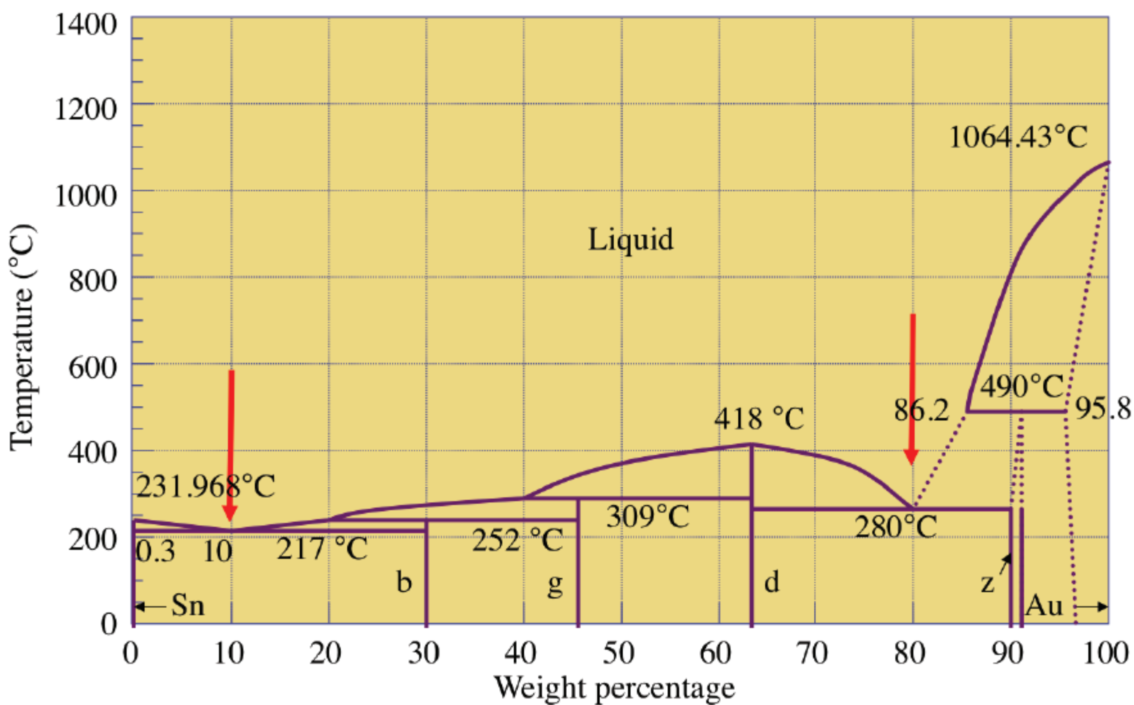


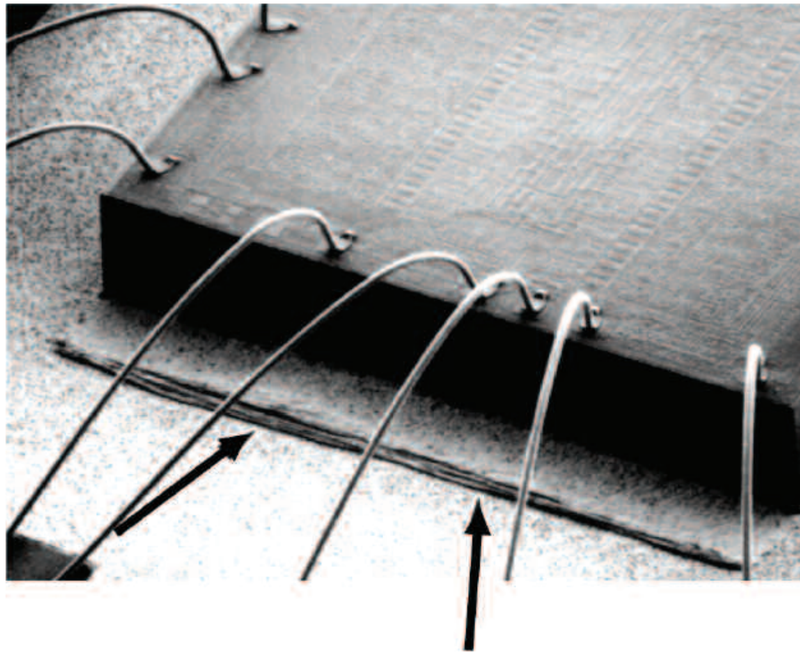
Eutectic die attaches can work particularly well with ceramic packages. This provides both mechanical and electrical connection between the die and the package substrate. This SEM image shows a cross-sectional view of a gold-silicon eutectic bond. The darker dots are the silicon embedded in the gold material. Although the gold silicon eutectic process requires a higher temperature, the electrical and mechanical properties of the connection are more stable and reliable than a silver-filled epoxy bond.



Gold and silicon individually each have very high melting temperatures. However, when they are mixed in the right proportions, the melting temperature decreases dramatically. This graph shows the phase diagram for the gold silicon two-metal system. At a concentration of 97.15% gold and 2.85% silicon, the melting temperature reaches a minimum of 363 degrees centigrade. This minimum point is known as the eutectic point, or the lowest point at which the materials will remain in their liquid state. This ratio varies for different materials. However, this is low enough to work with some fully processed dice.



We show the phase diagram for the gold-tin system here. There are two distinct minima in the melting point. One is 280 degrees centigrade at 80% gold – 20% tin, and the other is 232 degrees centigrade at 10% gold – 90% tin. The lower temperature minimum is the one most commonly used for die attach operations, since it involves lower temperatures. Each eutectic material will have its own phase diagram and minima.



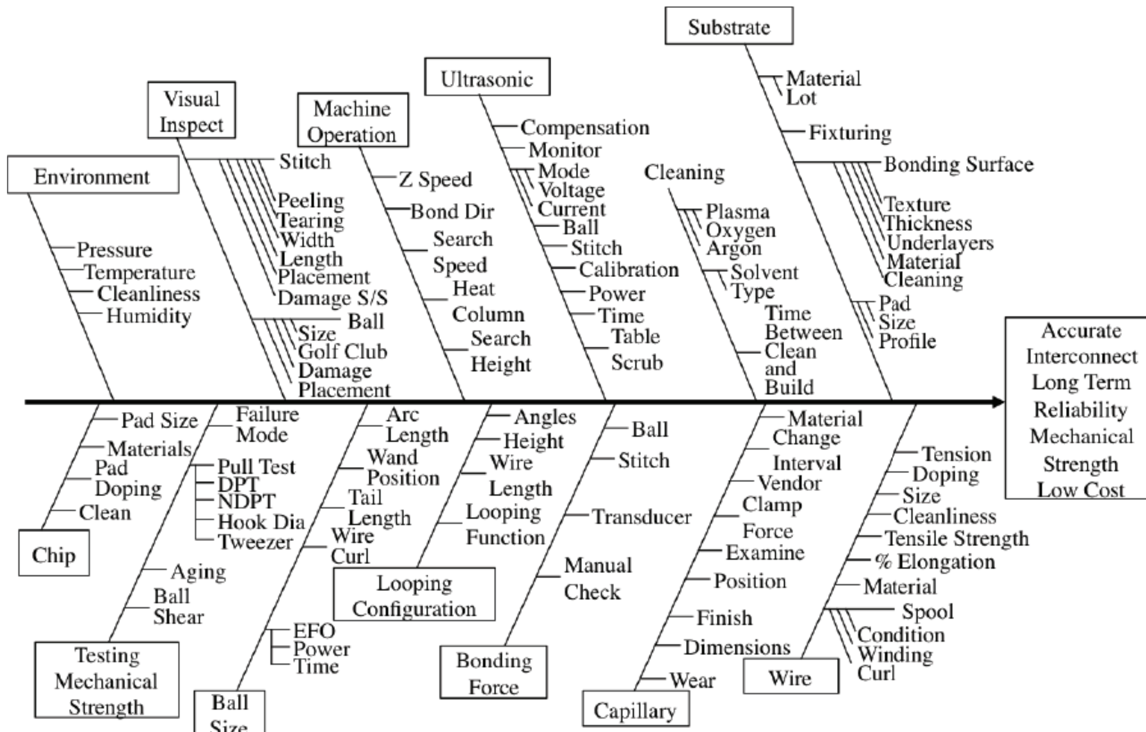
One problem that can occur during the eutectic die attach process is poor wetting to the die and/or the package well. As a result, the die attach can separate from the die and the package well, becoming a loose particle. This SEM image shows an example of this. The arrows indicate the loose die attach particle. During vibration, this sliver can move and become lodged across bondwires, or the bondwires and the substrate, causing an electrical short.

In conclusion, we discussed die attach materials. There are two basic classes of materials: the epoxy-based materials that use a conductive filler particle like silver for electrical connections, and eutectic materials, which rely on a minimum in the phase diagram to achieve a low temperature for attach. We also discussed some of the basic steps in the manufacturing process, as well as a few things that can go wrong during manufacturing that create failures.

Technical Tidbit

Bonding Variables

Wirebonding is, on the surface, what appears to be a simple operation. The bonding tool melts the end of the wire, presses it to the bond pad, uses ultrasonic energy to help aid in the bonding process, spools out the wire to the leadframe, presses the wire to the leadframe, uses ultrasonic energy to aid in the bonding process, sets a clamp to tear the wire, moves to the next pad, and repeats the process. In reality though, the process involves a number of variables.



This fishbone diagram shows many of the variables that factor into a high quality, high reliability thermocompression bond. There are several major factors, including the environment, machine operation, ultrasonics, cleaning, the substrate, the chip, the ball size, the looping configuration, bonding force, the capillary and the wire. All of these factors must be understood and controlled to produce a high quality bond. Quite often, the assembly house will set of a design of experiments to define the impact of the variables on the overall bonding process. This data can be used to optimize the bonding process and create a more robust and reliable bond.

Ask the Experts

Q: I have read that one can achieve different threshold voltage for mosfets by using different oxide thickness or different doping of source drain. However, threshold voltage depends on substrate doping, not on source or drain doping, correct??

A: There are three normal methods for creating transistors with different thresholds.

1. Adjust the thickness of the gate oxide.
2. Adjust the doping levels in the channel. This is usually referred to as a threshold adjust implant.
3. Connect the transistor in such a way as to control the body bias. Drain/Source doping would have an extremely minor effect on the threshold voltage.

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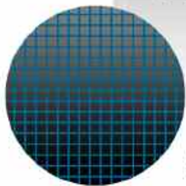

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Spotlight: Wafer Fab Processing

OVERVIEW

Semiconductor and integrated circuit developments continue to proceed at an incredible pace. The industry as a whole has gotten to this point of incredible complexity through the process of countless breakthroughs and developments in wafer fab processing. Today's wafer fab contains some of the most complex and intricate procedures ever developed by mankind. ***Wafer Fab Processing*** is a 4-day course that offers an in-depth look into the semiconductor manufacturing process, and the individual processing technologies required to make them. We place special emphasis on the basics surrounding each technique, and we delve into the current issues related to manufacturing the next generation devices. This course is a must for every manager, engineer and technician working in the semiconductor industry, using semiconductor components or supplying tools to the industry.

By focusing on the basics of each processing step and the issues surrounding them, participants will learn why certain techniques are preferred over others. Our instructors work hard to explain how semiconductor processing works without delving heavily into the complex physics and mathematical expressions that normally accompany this discipline.

Participants learn basic but powerful aspects about the semiconductor industry. This skill-building series is divided into three segments:

1. **Basic Processing Steps.** Each processing step addresses a specific need in IC creation. Participants learn the fundamentals of each processing step and why they are used in the industry today.
2. **The Evolution of Each Processing Step.** It is important to understand how wafer fab processing came to the point where it is today. Participants learn how each technique has evolved for use in previous and current generation ICs.
3. **Current Issues in Wafer Fab Processing.** Participants learn how many processing steps are increasingly constrained by physics and materials science. They also learn about the impact of using new materials in the fabrication process and how those materials may create problems for the manufacturers in the future.

COURSE OBJECTIVES

1. The seminar will provide participants with an in-depth understanding of the semiconductor industry and its technical issues.
2. Participants will understand the basic concepts behind the fundamental wafer fab processing steps.
3. The seminar will identify the key issues related to each of the processing techniques and their impact on the continued scaling of the semiconductor industry.
4. The seminar offers a wide variety of sample problems that participants work to help them gain knowledge of the fundamentals of wafer fab processing.
5. Participants will be able to identify the basic features and principles associated with each major

processing step. These include processes like chemical vapor deposition, ion implantation, lithography, and etching.

6. Participants will understand how processing, reliability, power consumption and device performance are interrelated.
7. Participants will be able to make decisions about how to construct and evaluate processing steps for CMOS, BiCMOS, and bipolar technologies.

INSTRUCTIONAL STRATEGY

By using a combination of instruction by lecture, classroom exercises, and question/answer sessions, participants will learn practical information on semiconductor processing and the operation of this industry. From the very first moments of the seminar until the last sentence of the training, the driving instructional factor is **application**. We use instructors who are internationally recognized experts in their fields that have years of experience (both current and relevant) in this field. The accompanying textbook offers hundreds of pages of additional reference material participants can use back at their daily activities.

COURSE OUTLINE

Day 1

1. Module 1: Basics & Fundamentals; Semiconductor Devices and ICs
   a. Acronyms
   b. Common Terminology
   c. Brief History
   d. Semiconductor Materials
   e. Electrical Conductivity
   f. Semiconductor Devices
   g. Classification of ICs & IC Processes
   h. Integrated Circuit Types
2. Module 2: Crystallinity, Crystal Defects, Crystal Growth
   a. Crystallinity
   b. Crystal Defects
   c. Crystal Growth
   d. Controlling Crystal Defects
3. Module 3: Basic CMOS Process Flow
   a. Transistors and Isolation
   b. Contacts/Vias Formation
   c. Interconnects
   d. Parametric Testing
4. Module 4: Ion Implantation 1 (The Science)
   a. Doping Basics
   b. Ion Implantation Basics
   c. Dopant Profiles
   d. Crystal Damage & Annealing

5. Module 5: Ion Implantation 2 (Equipment, Process Issues)
    a. Equipment
    b. Process Challenges
    c. Process Monitoring & Characterization
    d. New Techniques

Day 2

6. Module 6: Thermal Processing
    a. Overview of Thermal Processing
    b. Process Applications of SiO2
    c. Thermal Oxidation
    d. Thermal Oxidation Reaction Kinetics
    e. Oxide Quality
    f. Atomistic Models of Thermal Diffusion
    g. Thermal Diffusion Kinetics
    h. Thermal Annealing
    i. Thermal Processing Hardware
    j. Process Control
7. Module 7: Contamination Monitoring and Control
    a. Contamination Forms & Effects
    b. Contamination Sources & Control
    c. Contamination Characterization & Measurement
8. Module 8: Wafer Cleaning
    a. Wafer Cleaning Strategies
    b. Chemical Cleaning
    c. Mechanical Cleaning
9. Module 9: Vacuum, Thin Film, & Plasma Basics
    a. Vacuum Basics
    b. Thin Film Basics
    c. Plasma Basics
10. Module 10: CVD 1 (Basics, LPCVD, Epitaxy)
    a. CVD Basics
    b. LPCVD Films
    c. LPCVD Equipment
    d. Epi Basics
    e. Epi Process Applications
    f. Epi Deposition Process
    g. Epi Deposition Equipment

Day 3

11. Module 11: PVD
    a. PVD (Physical Vapor Deposition) Basics
    b. Sputter Deposition Process
    c. Sputter Deposition Equipment
    d. Al-Based Films
    e. Step Coverage and Contact/Via Hole Filling
    f. Metal Film Evaluation
12. Module 12: Lithography 1 (Photoresist Processing)
    a. Basic Lithography Process
    b. Photoresist Materials
    c. Photoresist Process Flow
    d. Photoresist Processing Systems
13. Module 13: Lithography 2 (Image Formation)
    a. Basic Optics
    b. Imaging
    c. Equipment Overview
    d. Actinic Illumination
    e. Exposure Tools
14. Module 14: Lithgroaphy 3 (Registration, Photomasks, RETs)
    a. Registration
    b. Photomasks
    c. Resolution Enhancement Techniques
    d. The Evolution of Optical Lithography
15. Module 15: Etch 1 (Basics, Wet Etch, Dry Etch)
    a. Etch Basics
    b. Etch Terminology
    c. Wet Etch Overview
    d. Wet Etch Chemistries
    e. Types of Dry Etch Processes
    f. Physics & Chemistry of Plasma Etching

Day 4

16. Module 16: Etch 2 (Dry Etch Applications and Equipment)
    a. Dry Etch Applications
    b. SiO2
    c. Polysilicon
    d. Al & Al Alloys
    e. Photoresist Strip
    f. Silicon Nitride
    g. Dry Etch Equipment
    h. Batch Etchers

- i. Single Wafer Etchers
- j. Endpoint Detection
- k. Wafer Chucks

17. Module 17: CVD 2 (PECVD)
    - a. CVD Basics
    - b. PECVD Equipment
    - c. CVD Films
    - d. Step Coverage
18. Module 18: Chemical Mechanical Polishing
    - a. Planarization Basics
    - b. CMP Basics
    - c. CMP Processes
    - d. Process Challenges
    - e. Equipment
    - f. Process Control
19. Module 19: Copper Interconnect, Low-k Dielectrics
    - a. Limitations of "Conventional" Interconnect
    - b. Copper Interconnect
    - c. Cu Electroplating
    - d. Damascene Structures
    - e. Low-k IMDs
    - f. Cleaning Cu and low-k IMDs
20. Module 20: Leading Edge Technologies & Techniques
    - a. Process Evolution
    - b. Atomic Layer Deposition (ALD)
    - c. High-k Gate and Capacitor Dielectrics
    - d. Ni Silicide Contacts
    - e. Metal Gates
    - f. Silicon on Insulator (SOI) Technology
    - g. Strained Silicon
    - h. Hard Mask Trim Etch
    - i. New Doping Techniques
    - j. New Annealing Techniques
    - k. Other New Techniques
    - l. Summary of Industry Trends

References:

Wolf, Microchip Manufacturing,
Doering & Nishi, Semiconductor Manufacturing Technology, 2nd ed.
Wolf, Silicon Processing, Vol. 4
Wolf, Silicon Processing, Vol. 1, 2nd ed.

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Registration is available at
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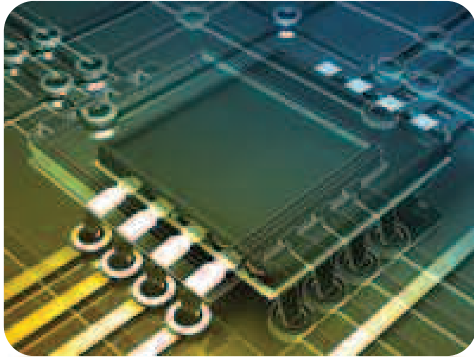
Chris Henderson will be attending and will be available for meetings. Please contact us at info@semitracks.com to schedule a meeting.



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If you have a suggestion or a comment regarding our courses, online training, discussion forums, or reference materials, or if you wish to suggest a new course or location, please call us at 1-505-858-0454 or Email us (info@semitracks.com).

To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered in the next newsletter, please contact Jeremy Henderson by Email (jeremy.henderson@semitracks.com).

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To post, read, or answer a question, visit our forums.
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Upcoming Courses

(Click on each item for details)

Wafer Fab Processing
June 27 – 30, 2016 (Mon – Thur)
San Jose, California, USA

Semiconductor Reliability
July 11 – 13, 2016 (Mon – Wed)
Singapore

EOS, ESD and How to Differentiate
July 25 – 26, 2016 (Mon – Tue)
Manila, Phillippines

Semiconductor Reliability / Product Qualification
September 12 – 15, 2016 (Mon – Thur)
Sam Jose, California