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Hot Carrier Degradation—Physics

By Christopher Henderson

One useful technique to indirectly observe the damage created by hot carriers is to measure the p-well current. The p-well current closely tracks the current into the gate oxide in a hot carrier stress situation. In this graph, one can see that the p-well current peaks at approximately 50% of the drain-to-source voltage. The p-well current is almost non-existent at low gate-to-source voltages, increases rapidly to its peak, and then tails off to a lower value at higher gate-to-source voltages. At low gate-to-source voltages, there is no current through the channel. At high gate-to-source values the pinch-off region decreases, precluding the possibility of electrons scattering into the p-well. The p-well current at these higher values comes solely from diffusion currents.

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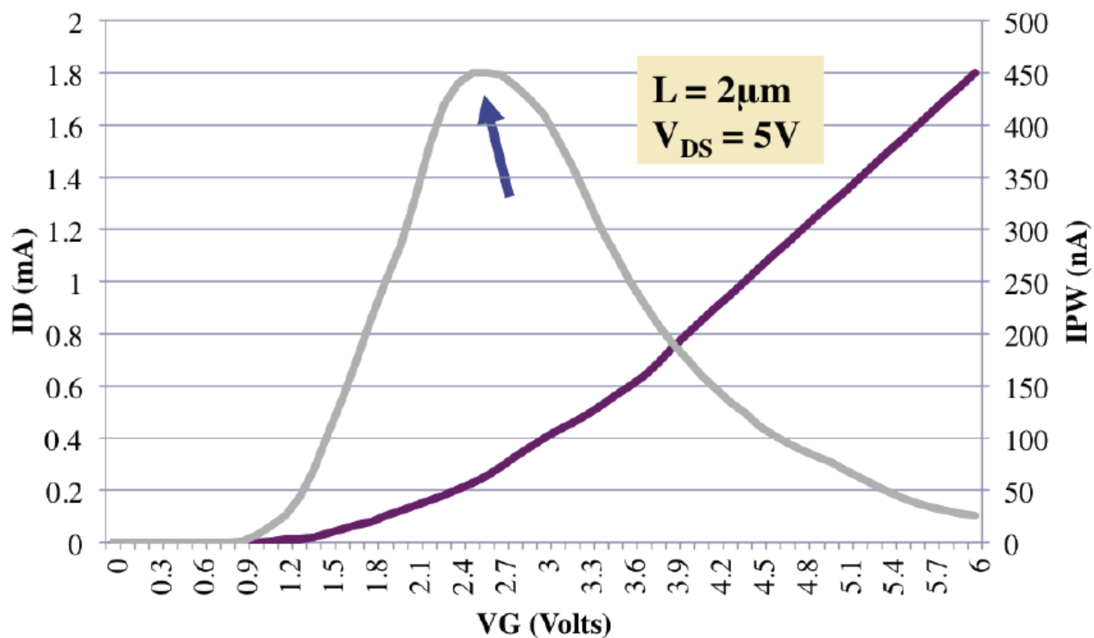

Figure 7. Hot Carrier Damage Tracks the P-well Current.

In Figure 8, we overlay a plot of light emission intensity with the p-well current. One can see that the light emission and the p-well current track fairly closely. There are some minor differences that occur because of the behavior of the transistor, but to first order they are the same. This means that p-well current is an excellent indicator of hot carrier damage. Engineers can therefore ascertain the level of hot electron damage by monitoring the p-well current. This electrical test is cost effective and straightforward to perform on a test structure. In contrast, a direct measurement of the light intensity requires sophisticated night vision camera or CCD hardware.

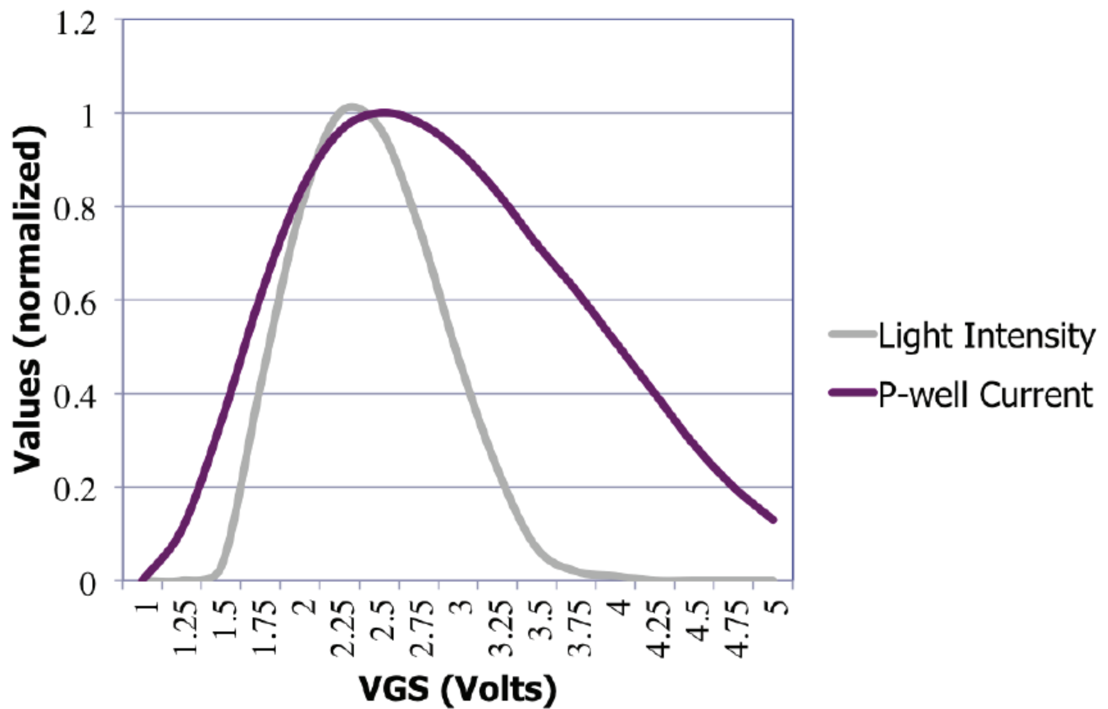

Figure 8. Light Emission and P-well Current Track.

Although light emission is an expensive and more complicated test, it can be an invaluable tool for localizing hot carrier damage, especially if one does not know where it might be occurring. In Figure 9 one can see light emission occurring in the n-channel transistors associated with the ring oscillator, and the input and output buffers to the test structure. A ring oscillator provides a worst-case scenario for digital logic, since it is running at the maximum frequency of the technology.

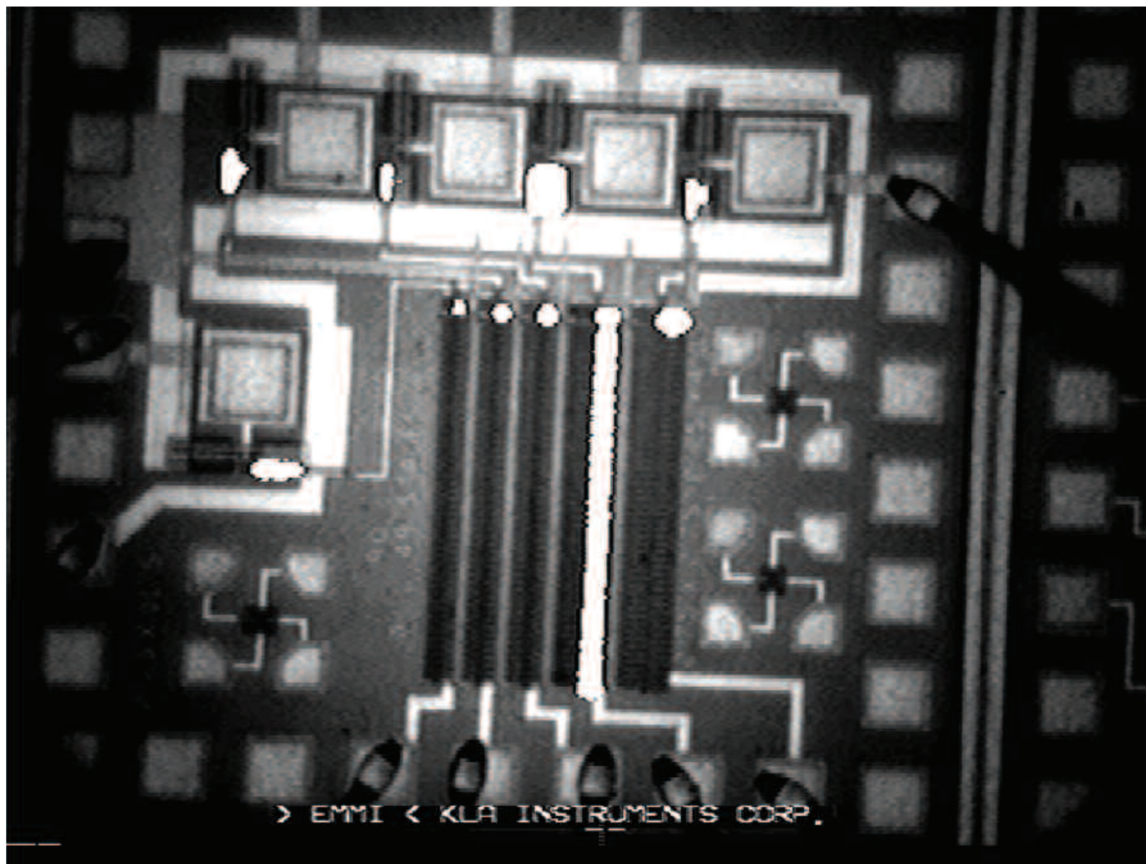

Figure 9. Light Emission Ring Oscillator (N-channel Devices in Saturation).

Classical hot carrier modeling is done using the equation $\Delta p = At^n$. Generally, one can describe the degradation as a change in a paramater, Δp. Δp is equal to A times t raised to the power n, where t represents time, A is a material dependent parameter, and n is an empirically determined exponent.

For more detailed calculations, one can model the n- and p-channel transistors separately. One uses the Eyring model for n-channel transistors, where the time to failure is given by the equation $TTF = B(I_{sub})^{-N}e^{(E_A/kT)}$. B is an arbitrary scale factor, I_{sub} is the peak substrate current during stressing, N is a current exponent that is typically between 2 and 4, and E_A is the activation energy. Please note that the apparent activation energy can be negative or positive depending on channel length and voltage.

One can use the Eyring model for p-channel transistors as well. This model was developed for transistors with gate lengths greater than a quarter micron, and is given by the equation $TTF = B(I_{gate})^{-M}e^{(E_A/kT)}$. Again, B is an arbitrary scale factor, I_{gate} is the peak gate current during stressing, M is the current exponent, and E_A is the activation energy, which is typically close to zero. One should note that a rough "rule-of-thumb" for the gate current versus voltage dependence of p-channel devices is that the peak gate current doubles for each 0.5 V increase in source-drain voltage.

The typical model for p-channel devices that have gate lengths of less than a quarter micron is $TTF = B(I_{sub})^{-N}e^{(E_A/kT)}$. The equation is similar to the long channel equation, except that substrate current is used instead of gate current. Please note that the apparent activation energy can be negative or positive depending on channel length and voltage.

Here we will work an example problem where we calculate the acceleration factor (AF, relative severity) for hot carrier injection for an office environment versus a stressed test structure environment. We assume the office = 50°C chip temperature & substrate current of 1μA and the test structure environment conditions are -40°C & 10μA substrate current (accelerated by elevating Vc) and assume a current exponent (N) of 3 and an activation energy of minus 0.15 electron-volts. The conclusion is that moving from accelerated test structure environment to the office environment will increase the time to fail value to by 8000X of the accelerated stress value, of which 1000X is due to substrate current and 8X is due to temperature.

Calculations:

AF (ratio of TF values, office/accel) = $(I_{sub}\text{ office} / I_{sub}\text{ accel})^{-N} \exp([E_A/k](1/T_{office} - 1/T_{accel}))$

AF = $(1\mu A / 10\mu A)^{-3} \exp([-0.15eV / 8.62 \times 10^{-5} eV/K](1/(273+50)K - 1/(273-40)K)$

AF(office/accel) = $1\times10^{+3} \times 8 = 8000$

Scientists studying hot carrier degradation have identified various mechanisms associated with n-channel and p-channel transistors. In n-channel transistors, hot electrons tend to generate interface states when the gate voltage is between 33 and 50% of the drain-to-source voltage. When the gate voltage is approximately 20% of the drain-to-source voltage, hole injection dominates the process. As the gate voltage approaches the drain-to-source voltage, electron injection dominates the process. In p-channel transistors, oxide electron trapping dominates a lower gate voltage, say 20% of the drain-to-source voltage. At higher gate voltages of 33 to 50% of the drain-to-source voltage, interface state generation dominates.

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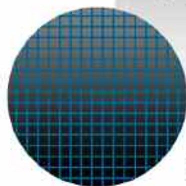

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Technical Tidbit

Coreless Substrates

In a standard build-up package, there is a core material made from FR4 or BT epoxy laminate. A build-up package requires a fan-out region to match the bump and/or the line pitch to the plated through hole pitch. We highlight this region with the yellow ellipses in Figure 1. In a coreless package there is no core material, just build-up materials. This facilitates direct signaling. Designers can use all of the layers for signals, and the approach maximizes wiring efficiency. It also reduces impedance mismatches that occur as the result of the plated-through holes. Co-planarity is also better with a coreless package. The major issue with coreless substrates is warpage. Warpage is up to four times worse with a coreless substrate due to the lack of a rigid core to hold everything in place. As a result, not many manufacturers are using coreless substrates. However, Sony uses this technology in the latest version of their Cell processor family.

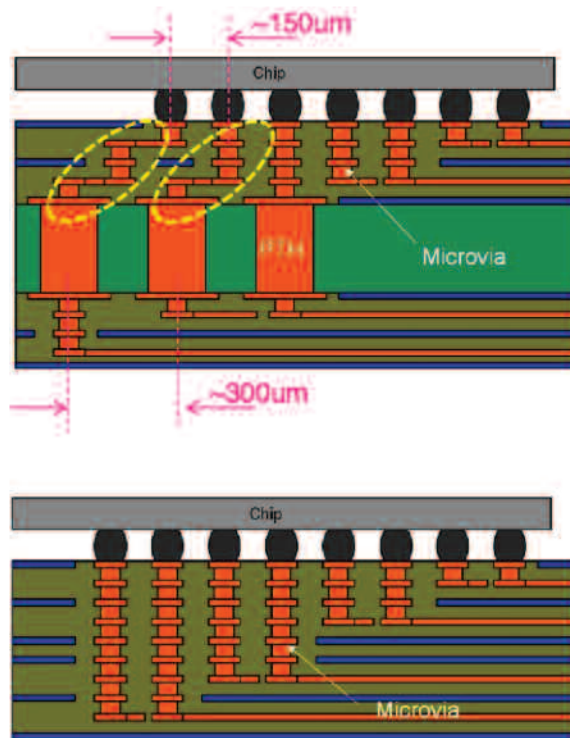

Figure 1.

The major player for coreless package build-up materials is Ajinomoto. The Ajinomoto Build-up Film—or ABF—is used extensively in the industry already on substrates with cores, and now used for coreless build-up as well (see Figure 2).

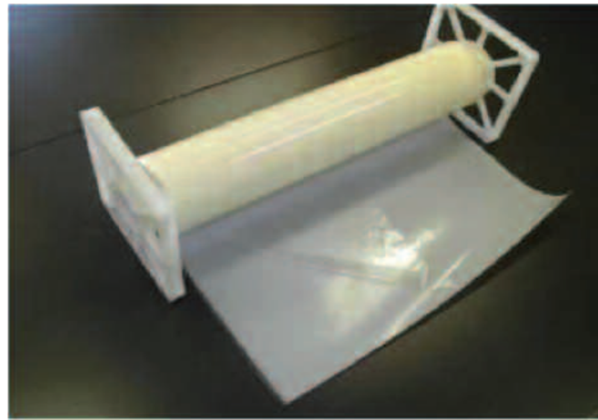

Figure 2.

ABF is a three-layer polymer system, with a polyethylene terephthalate (PET) support film, a resin layer, and a cover film (see Figure 3). One can deposit copper on the thin to create interconnect traces. Ajinomoto has evolved its ABF to remove the halogens, lower the coefficient of thermal expansion, and allow for narrower vias. It is used widely as a standard build-up material, and is now in limited use for coreless substrates.

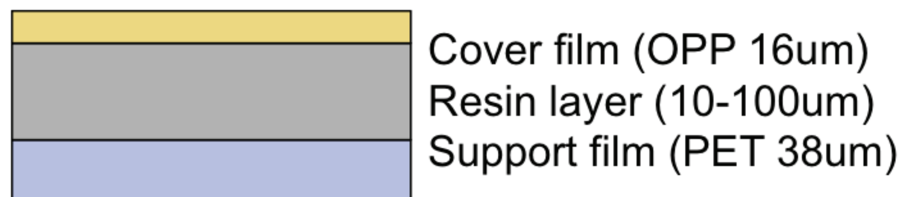

Figure 3.

Ask the Experts

Q: How fast does an underfill flow around the bumps or pillars on a device??

A: There are a number of variables involved in determining that number. They include: the viscosity of the underfill (which is dependent on the epoxy properties and the amount of filler particles), the size of the package, the number of bumps, the density of bumps (which is a function of their pitch), the height of the bumps, the temperature, other chemicals present (like adhesion promoters and flux), and so on. As a rough number though, a combination of substrate temperature, material, equipment and dispense process can show complete flow out under a 25mm square die with 60µm gap in about 35 seconds.

Spotlight: MEMS Packaging

OVERVIEW

Microelectromechanical Systems (MEMS) have captured the interest of the public with their promise to miniaturize existing systems. Although much of the excitement surrounding MEMS has died down, real applications are beginning to emerge. MEMS accelerometers for games, automotive, and wireless applications have emerged. MEMS inkjet chips are now ubiquitous, and new applications for RF and sensors are in development. One of the most challenging aspects of MEMS is packaging. Forces that normally do not affect meso-scale objects must be understood and controlled at the micro-scale. This has created a number of challenges related to the packaging of these components. ***MEMS Packaging*** is a comprehensive 2-day course that offers detailed instruction on the design and modeling of MEMS packages. We place special emphasis on surface-to-volume ratio issues, electrostatics, liquid wetting, inertia, and other parameters. This course is a must for every manager, engineer, and technician working in semiconductor packaging, using MEMS components in high performance applications or new packaging configurations, or supplying packaging tools to the industry.

WHAT WILL I LEARN BY TAKING THIS CLASS?

By focusing on the fundamentals of MEMS packaging, participants will learn why advances in the industry are occurring along certain lines and not others. Our instructor works hard to explain MEMS packaging without delving heavily into the complex physics and materials science that normally accompany this discipline.

Participants learn basic but powerful aspects about semiconductor packaging. This skill-building series is divided into four segments:

1. **MEMS Market Overview.** Participants understand the driving market forces behind MEMS packaging. They review the technology trends, the market segments, and the major manufacturers and suppliers.
2. **MEMS Technical Basics.** Participants review the basic wafer processing steps for MEMS devices, including deep reactive ion etching, wet etching, patterning, CMP, and more. They also discuss the major research activities occurring in the MEMS area.
3. **MEMS Assembly, Testing, and Packaging.** Participants learn the fundamentals of packaging concepts for MEMS devices. They learn about bonding, printing, backgrinding, structural release, wirebonding, flip chip attach, cleaning, encapsulation, and basic testing. They discuss the challenges and tradeoffs associated with each topics.
4. **MEMS Reliability.** Participants learn MEMS reliability issues and associated analysis and simulation techniques. They also learn about the physics and mechanics issues involved in reliability degradation of MEMS devices.

COURSE OBJECTIVES

1. At the end of the course, participants will understand the major issues associated with MEMS Packaging.
2. They will also know how MEMS devices are fabricated and packaged.
3. Participants should be able to identify areas within MEMS Packaging where development is occurring.
4. The attendees will gain an understanding of process activities like backgrinding, structural release, clean, and encapsulation.
5. Participants will gain a basic understanding of testing MEMS devices.
6. The participants will learn about reliability aspects of MEMS devices, in particular, reliability issues associated with the packaging process.
7. Finally, the participants can interact with the instructor to discuss specific items and directions of interest at Kulicke and Soffa regarding MEMS assembly and test.

COURSE OUTLINE

1. MEMS Market Overview (downplay this activity, but do enough to get everyone on the same page)
    - 1.1. Types of devices, applications, volumes, growth rates
    - 1.2. Technology trends
    - 1.3. Major device manufacturers
    - 1.4. Major assembly and test equipment manufacturers
2. MEMS Technical Basics
    - 2.1. Overview of Device Processing and Manufacturing Techniques
        - 2.1.1. Summary of MEMS fabrication processes
        - 2.1.2. Overview of what's going on at R&D Centers in MEMS
        - 2.1.3. Major equipment suppliers by process step
        - 2.1.4. Backend/packaging level – who is doing what?
        - 2.1.5. Environmental considerations in MEMS fabrication and assembly processes
    - 2.2. The Impact of Packages and Assembly Processes in MEMS Device Operation
    - 2.3. High-level method of operation of device types and the role of packaging for each
        - 2.3.1. Pressure Sensors and microphones
        - 2.3.2. Inertial sensors: accelerometers and gyroscopes
        - 2.3.3. Magnetic sensors: compasses and Hall sensors
        - 2.3.4. Optical MEMS: displays and imagers
        - 2.3.5. RF MEMS: switches, time bases, and relays
        - 2.3.6. Fluidic MEMS: ink jets, Lab on a chip, DNA analysis

3. Assembly, Packaging and Testing Processes (this should be the major portion of the course)
    3.1. Material topics for MEMS packaging
        3.1.1. Classes of materials used in MEMS packaging
        3.1.2. Critical material parameters for MEMS packages
    3.2. Bonding, Joints and Adhesion Processes
        3.2.1. Theory of bonding and adhesion
        3.2.2. Wafer bonding
        3.2.3. Thermocompression bonding and welding
        3.2.4. Soldering and brazing
        3.2.5. Sealing glasses and frit bonding
        3.2.6. Polymer bonding processes
    3.3. Printing, Plating and Dispensing
        3.3.1. Screen and stencil printing
        3.3.2. Metallic plating
        3.3.3. Dispensing processes
    3.4. Wafer Backgrind, Singulation and MEMS Release
        3.4.1. MEMS structural release
        3.4.2. Wafer backgrinding processes
        3.4.3. Wafer singulation (dicing) topics
        3.4.4. Interaction and tradeoffs between release and singulation
    3.5. Considerations in MEMS Die Attach
        3.5.1. Die attach process overview
        3.5.2. Unique factors in MEMS die attach
        3.5.3. Interaction between MEMS types/structure and process requirements
        3.5.4. MEMS die attach materials and processes
    3.6. Wirebonding MEMS devices
        3.6.1. Wirebond process overview
        3.6.2. Unique factors in MEMS wirebonding
        3.6.3. Interaction between MEMS types/structure and process requirements
        3.6.4. MEMS wirebonding materials and processes
    3.7. Flip Chip technologies as applied to MEMS
        3.7.1. Flip Chip process overview
        3.7.2. Unique factors in MEMS Flip Chip
        3.7.3. Flip chip materials and processes for MEMS
    3.8. Hermetic package assembly
        3.8.1. Principles of hermeticity, permeability and outgassing
        3.8.2. Vacuum and specialty gas sealing and gettering
        3.8.3. Hermetic packages styles
    3.9. Non-Hermetic Package Assembly
        3.9.1. Molding and encapsulation
        3.9.2. Plastic and substrate package styles

3.10. Chip Scale and Wafer Scale Packages
3.10.1. Wafer-level packaging process overview
3.10.2. Types of wafer-level packages
3.10.3. Thru-Silicon Vias (TSVs)
3.11. Tradeoffs in MEMS Packaging and Assembly Processes
3.11.1. Hermetic vs. non-hermetic packages
3.11.2. Wirebond vs. flip chip vs. TSV
3.11.3. Integration of MEMS release in the assembly process
3.11.4. Wafer-scale vs. component scale packaging
3.11.5. One chip vs. two chip solutions – what are the drivers?
3.12. MEMS Inspection
3.12.1. Special Cleaning Requirements
3.13. MEMS Test Considerations
3.13.1. Wafer-level MEMS testing considerations
3.13.2. MEMS testing during product development
3.13.3. End of Line MEMS testing
3.14. Throughput requirements per process step
3.14.1. Handling formats and systems
3.14.2. Handoffs between steps
4. MEMS Reliability
4.1. Overview of reliability and qualification test types
4.2. Typical failure mechanisms
4.3. Materials related issues
4.4. Process related issues
4.5. Assembly equipment features that improve reliability

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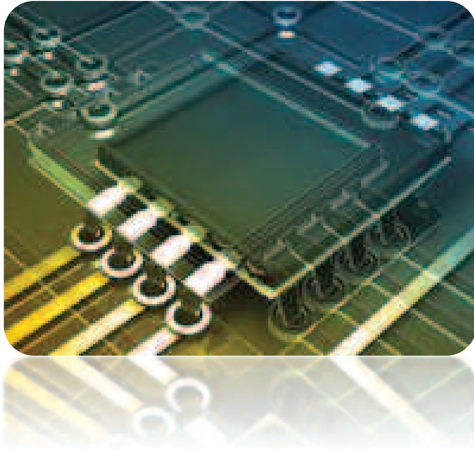
Chris Henderson will be attending and will be available for meetings. Please contact us at info@semitracks.com to schedule a meeting.



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Product Qualification
September 9 – 10, 2015 (Wed – Thur)
Munich, Germany

MEMS Packaging and Reliability
September 14 – 15, 2015 (Mon – Tues)
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