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Time Domain Reflectometry

By Christopher Henderson

In this section we will discuss time domain reflectometry. Time Domain Reflectometry, or TDR, is a technique finding increased use as a fault localization tool for devices with more complex packaging, such as wafer chip scale packaging, stacked packages, and devices with substrates or interposers. First we'll discuss the hardware and components associated with Time domain reflectometry. Next, we'll discuss the waveforms and how one can calculate a distance to an open or resistive change. We'll then discuss how to interpret the waveforms produced by TDR. Last, we'll introduce electro-optical TDR and describe how it can improve interpretation and localization of failures.

Time domain reflectometry is a technique that is becoming more common as a failure analysis technique. It is an electrical technique and is non-destructive. In time domain reflectometry, or TDR, an oscilloscope with a pulse shaper generates an electrical pulse. This pulse travels through the cabling to the package of the device under test. At the various material interfaces and corners, there will be some amount of reflection and transmission. A well-matched interface should have very little reflection, while a poorly matched interface would have a large reflection. In theory, the return waveform from an open solder bump, for instance, should show up as a marked change from the waveform through a good solder bump. The key challenge with this technology is resolution, interpretation, and integration with the design files.

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Figure 1 shows an example of a time domain reflectometry setup for failure analysis work. The computer on the right drives the Tektronix digital sampling oscilloscope, shown on the lower left. The module with the silver-colored cable connects to the small blue box to generate the picosecond pulse width needed for the generated pulse, while the module connected to the copper-colored cable is the sampling head for the reflected signal. The yellow cable propagates the signal to the device under test.

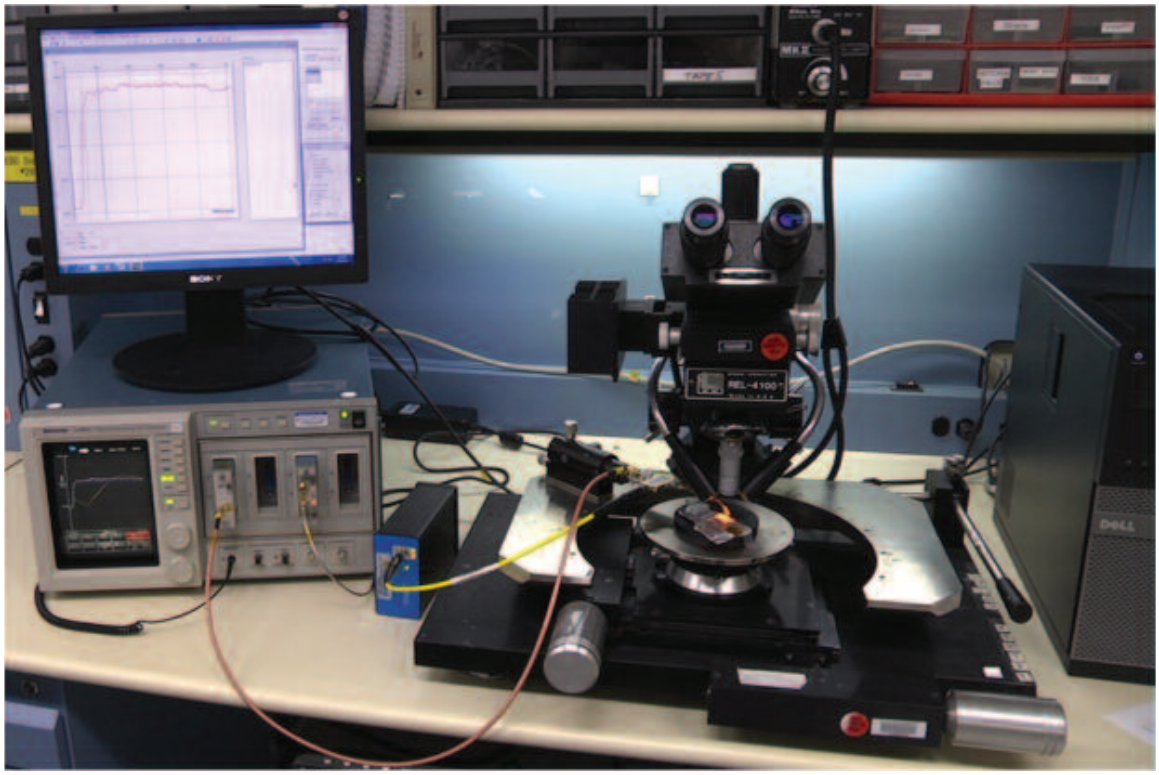

Figure 1. Time Domain Reflectometry Setup.

Figure 2 shows a closer view of the TDR probe. In this configuration, the probe is mounted to a micromanipulator head for precise positioning over a lead, pad, or bump. The device under test is mounted to a glass slide to provide isolation from the stage, leading to a more accurate signal. The two black heads near the microscope objective are simply for lighting the sample more clearly.

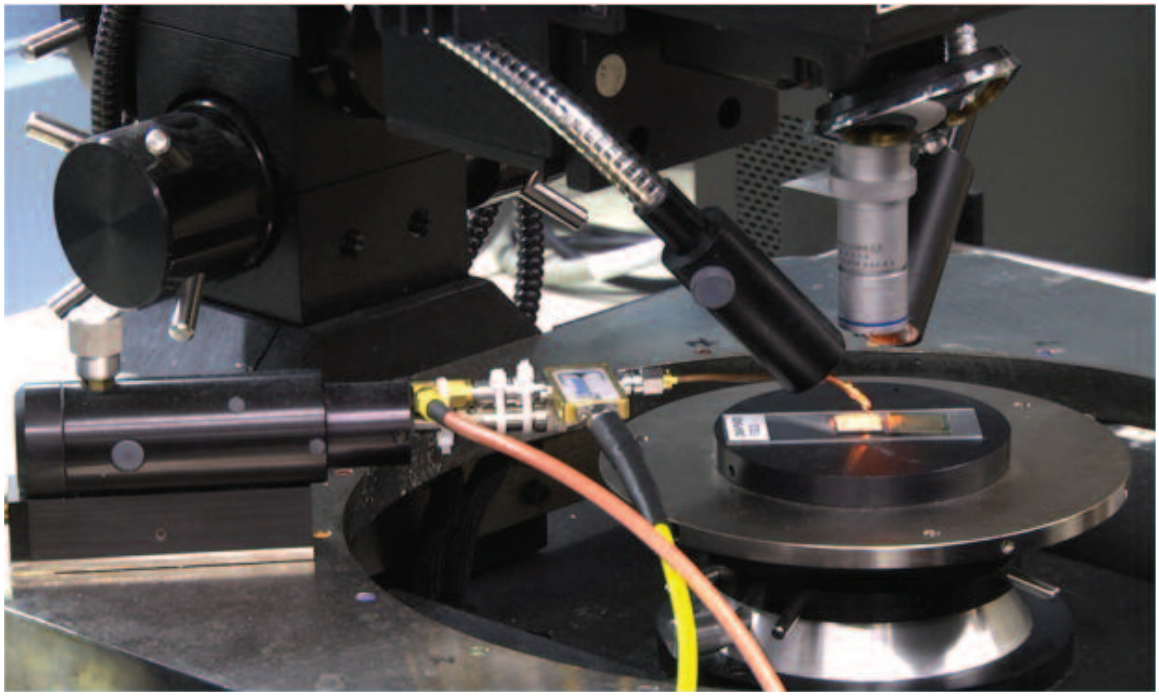

Figure 2. Closer view of the TDR probe and package.

Before discussing TDR waveforms let's briefly review the electrical waveform behavior at interfaces. If you recall from basic electronics or electricity and magnetism, a waveform will react at an interface between two different impedances by generating a transmitted component and a reflected component. The closer the impedances between the two materials, the larger the transmitted component will be. The more different the impedances, the larger the reflected component will be. For instance, at the cable to solder bump interface the match is only fair, so there will be a transmitted component and a reflected component. At the solder bump to pad interface the match might be better, so there is less of a reflected component. If, however, there is an open between the solder bump and the pad trace, the impedance is much different, leading to a mostly reflected component. This shows up as a difference in the waveform like we see on the right in Figure 3.

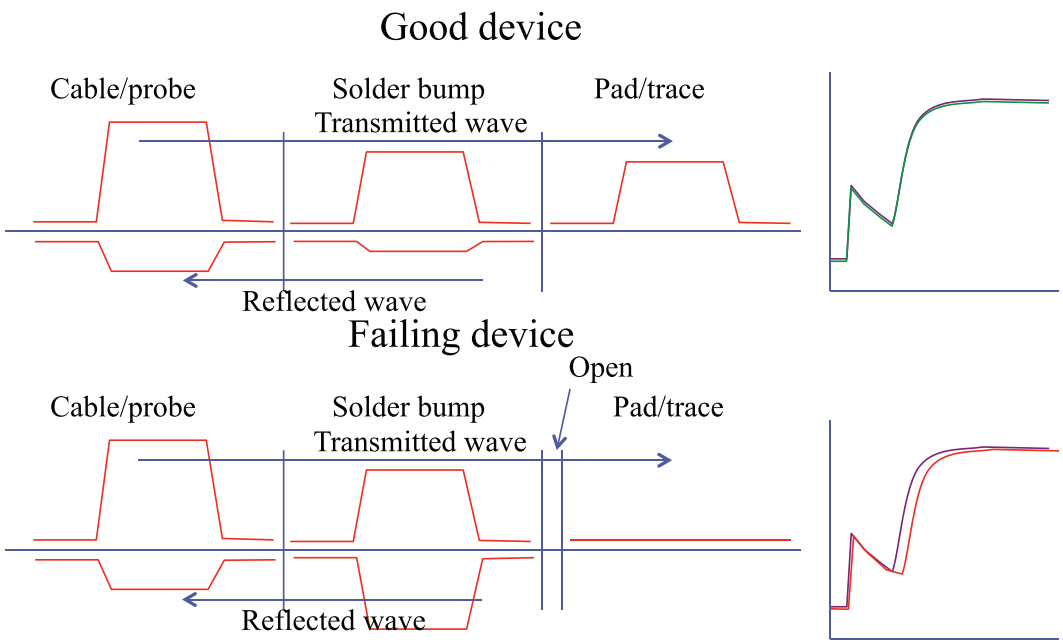

Figure 3. Basic waveforms.

Let's discuss the waveforms in more detail. Figure 4 (left) is an example of the waveform from a good device. The red trace represents the waveform from the probe when disconnected from the device. We see a waveform that steps up abruptly at just under 100 psec. This indicates that the pulse is completely reflected and returns to the oscilloscope around 100 psec after launch. The blue and green waveforms show the device under test and a comparison or golden unit. Note that the waveforms are very similar. There is an initial sharp rise that matches the red trace — this is related to the mismatch at the solder bump/probe interface. The slower rise associated with blue and green waveforms comes from multiple minor reflections at various interfaces and corners within the package up to the transistors in the I/O circuitry.

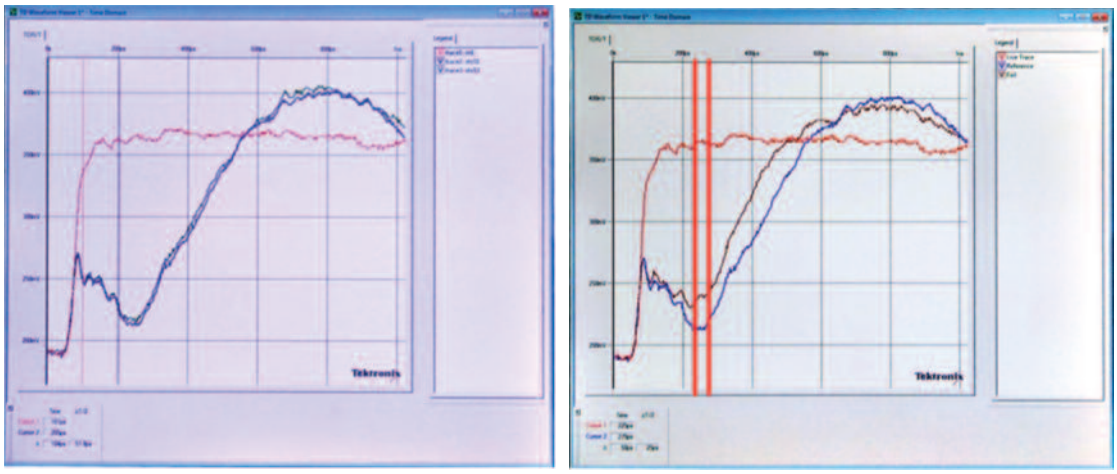

Figure 4. Waveforms from good (left) and failing (right) devices.

In Figure 4 (right) we show a comparison device, the blue signal, and a failing device, the brown signal. We position the first cursor just beyond the minimum signal point after the initial reflection from the probe/device package interface in the comparison device. We then position the second cursor just beyond the minimum signal point in the blue waveform. There is obviously some guesswork to this placement; it is not an exact science. The difference in the times will be used to calculate the distance to the defect.

Once the engineer captures the signal and establishes a time difference, he or she must relate that time difference back into a distance to establish where the open or change in resistance might be. The distance to the defect in millimeters can be calculated by

$$D = \frac{c \cdot \Delta t}{2 \times 10^{9} \cdot \varepsilon}$$

where c is the speed of light in meters per second, Δt is the estimated time difference calculated from the waveforms, and ε is the dielectric constant of the material. Different materials have different dielectric constants, so one needs to take this variable into account. We show some example materials and their dielectric constants in Table 1. As an example calculation, a Δt of 50 psec gives a distance to the open of 3.71mm in a fiberglass substrate.

Material	Dielectric Constant ε
Ceramic	9.6
FR-4	4.8
Fiberglass	4.09
Polyimide	3.5-3.8
Benzocyclobutene (BCB)	2.65
Bismaleimide Triazine (BT)	3.2-3.3

Table 1. Dielectric constants for common electronics isolation materials.

In next month's article, we'll discuss how to interpret TDR signals, and a new form of TDR called Electro-Optical TDR.

Technical Tidbit

Composition Resistors

The construction of a composition resistor is straightforward to understand. One uses machinery to hot press a cylinder of graphite and organic binders. One embeds leads in both ends of the graphite, the resistive material. The component is then covered in a thermoset polymer package and cured to create a solid cylinder-shaped component. These devices are not precise, and engineers typically use them in circuits where lower precision is acceptable. A composition resistor typically is only accurate to about 10% of its intended resistance value.

The image at the upper left shows an example of a typical composition resistor. The colored bands indicate the resistance value of the component. For more information on how to interpret the color bands, the reader show access IEC Standard 60062. There is also information on this topic at a number of websites, including Wikipedia. Most components contain four bands to list the first and second significant digits, the multiplier, and the tolerance. This component is a military component and has 5 bands; the fifth band indicates the failure rate. This particular component is a 1 megaohm resistor (red – which represents a "one" for the first significant bit, brown—which represents a "zero" for the second significant bit, blue—which represents the "six" for the 10 to the 6 multiplier, and gold—which represents a 5% tolerance. The image at the lower right shows a cross-sectional view. We can see the hot-pressed carbon element, the lead to element interface, and the thermoset compound encasing the element and the ends of the leads.

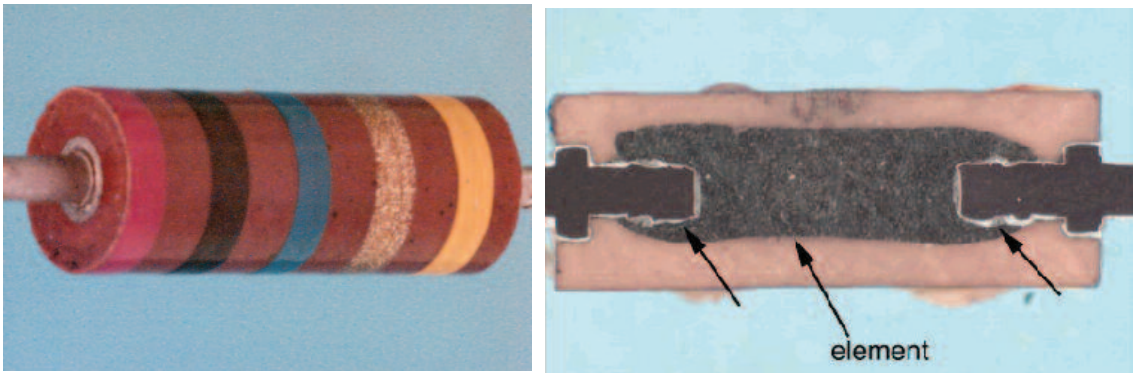

Figure 1. External view (left) and cross-section view (right) of a typical composition resistor.

Some typical failure modes for composition resistors include resistance increase due to moisture, electrical overstress damage, and mechanical damage. Moisture can lead to an increase in resistance. Moisture will penetrate through the thermoset, much like it does with a plastic encapsulated microcircuit. The moisture penetrates into the carbon element, causing swelling of the binders, leading to a change in the volume percentage of the carbon and a higher resistance. Baking most composition resistors will return the resistance back to normal. One can improve the humidity resistance through the use of coatings on the resistor component, or a conformal coating on the board. Electrical overstress is a common failure mode, and is often accompanied by signs of charring, cracking or burning at the exterior. Finally, mechanical damage can manifest itself as damage to the body of the resistor (a cracked package) or cracking at the interface between the leads and the resistive element.

Spotlight: Semiconductor Die/Wafer Level Reliability

We will be offering our Semiconductor Reliability Course in San Jose this fall. Here is an overview of the course and what topics we cover during this training.

OVERVIEW

Semiconductor reliability is at a crossroads. In the past, reliability meant discovering, characterizing and modeling failure mechanisms and determining their impact on the reliability of the circuit. Today, reliability can involve tradeoffs between performance and reliability, assessing the impact of new materials, dealing with limited margins, etc. Analysis and experimentation is now performed at the wafer level instead of the packaging level. This requires knowledge of subjects like design of experiments, testing, technology, processing, materials science, chemistry, and customer expectations. While reliability levels are at an all-time high level in the industry, rapid changes may quickly cause reliability to deteriorate. Your company needs competent engineers and scientists to help solve these problems. Semiconductor Die/Wafer Level Reliability is a 3-day course that offers detailed instruction on a variety of subjects pertaining to semiconductor reliability. This course is designed for every manager, engineer, and technician concerned with reliability in the semiconductor field, using semiconductor components, or supplying tools to the industry.

Participants learn to develop the skills to determine what failure mechanisms might occur, and how to test for them, develop models for them, and eliminate them from the product.

1. **Overview of Reliability and Statistics.** Participants learn the fundamentals of statistics, sample sizes, distributions and their parameters.
2. **Failure Mechanisms.** Participants learn the nature and manifestation of a variety of failure mechanisms that can occur both at the die level and at the package level. These include time-dependent dielectric breakdown, hot carrier degradation, NBTI, PBTI, electromigration, stress-induced voiding, contamination, retention, charge loss, etc.
3. **Test Structures.** Participants learn how test structures can be designed to help test for a particular failure mechanism.
4. **Test Strategies.** Participants learn the basics on how to test test-structures, design screening tests, and how to perform wafer level testing effectively.
5. **Design for Reliability.** Participants learn the developments occurring in DFR at the transistor, gate, block, and chip level.

COURSE OBJECTIVES

1. The seminar will provide participants with an in-depth understanding of the failure mechanisms, test structures, equipment, and testing methods used to achieve today's high reliability components.
2. Participants will be able to gather data, determine how best to plot the data and make inferences from that data.

3. The seminar will identify the major failure mechanisms, explain how they are observed, how they are modeled, and how they are eliminated.
4. The seminar offers a variety of video demonstrations of analysis techniques, so the participants can get an understanding of the types of results they might expect to see with their equipment.
5. Participants will be able to identify basic test structures and how they are used to help quantify reliability on semiconductor devices.
6. Participants will be able to understand and communicate design-for-reliability needs and goals to the designers and customers.
7. Participants will be able to identify appropriate tools to purchase when starting or expanding a laboratory.

INSTRUCTIONAL STRATEGY

By using a combination of instruction by lecture, video, problem solving and question/answer sessions, participants will learn practical approaches to the failure analysis process. From the very first moments of the seminar until the last sentence of the training, the driving instructional factor is **application**. We use instructors who are internationally recognized experts in their fields that have years of experience (both current and relevant) in this field. The handbook offers hundreds of pages of additional reference material the participants can use back at their daily activities.

THE SEMITRACKS ANALYSIS INSTRUCTIONAL VIDEOS™

One unique feature of this workshop is the video segments used to help train the students. Reliability Analysis is a visual discipline. The ability to identify nuances and subtleties in graphical data is critical to locating and understanding the defect. Some tools output video images that must be interpreted by engineers and scientists. No other course of this type uses this medium to help train the participants. These videos allow the analysts to directly compare material they learn in this course with real analysis work they do in their daily activities.

COURSE OUTLINE

Day One (Lecture Time 8 Hours)

1. Introduction to Reliability
   a. Basic Concepts: Here we identify the goals of reliability studies/qualification and relate it to overall chip quality.
   b. Definitions: We define the top-level terms and definitions used in reliability physics.
   c. Historical Information: We discuss the origins of the study of physics of failure and trace it through the study of physical mechanisms, fundamental materials properties, design for reliability to today's activities in reliability where one must trade off performance, reliability and cost.
2. Statistics and Distributions
   a. Basic Statistics: We identify the basic statistics used for reliability calculations and define the commonly used terms.

b. Distributions: We discuss the major distributions used in semiconductor reliability and in which situations to use them.
   i. Normal Distribution
   ii. Lognormal Distribution
   iii. Weibull Distribution
   iv. Exponential Distribution
c. Which Distribution Should I Use?: We identify areas where choosing the correction distribution is important and how to do so.
d. Data Handling: We discuss how to take data in such way as to maximize the odds of success.
e. Acceleration: We show how to make determinations of failure rates based on acceleration parameters and stress conditions.
f. Sample Size: We discuss the formula for calculating sample sizes need to demonstrate intended reliability levels.

Day Two (Lecture Time 8 Hours)

3. Failure Mechanisms
   a. Time Dependent Dielectric Breakdown
      i. Fundamental Parameters: We discuss the fundamental parameters and issues regarding making TDDB measurements.
      ii. Models (area, activation energies): We discuss the most widely used models in the industry and their advantages and disadvantages.
      iii. Soft Breakdown: We show how today's ICs fail more from soft breakdown and the challenges that causes in making reliability predictions.
      iv. Methods to improve TDDB: We discuss methods to improve TDDB ranging from process-related improvements to design techniques.
      v. BEOL TDDB: We discuss the mechanism of BEOL dielectric failure and the models to quantify its impact.
      vi. Exercises: We work some exercises to calculate TDDB reliability.
   b. Hot Carrier Damage
      i. Fundamental Parameters: We discuss the history and fundamental parameters associated with hot carriers.
      ii. Models: We cover the models used to calculate reliability for hot carrier degradation.
      iii. Effects in Modern ICs (stress liners, SiGe channel, HKMG): We discuss the impact of stress liners, High-K metal gate, and silicon-germanium channels on hot carriers.
      iv. AC effects: We describe the differences between DC and AC hot carrier lifetimes and how AC is more important to monitor.
   c. Negative Bias Temperature Instability
      i. Models: We discuss the Reaction-Diffusion model and how it can be used to calculate reliability.
      ii. Recovery effect: We describe the recovery effect that occurs with NBTI and how it can

change the outcome of the reliability analysis.
   iii. Methods to reduce NBTI: We discuss both process and design techniques for reducing NBTI.
   iv. Measurement techniques: We briefly introduce ultrafast or "on the fly" measurement techniques for NBTI.
d. Positive Bias Temperature Instability
   i. Models: We describe the model development occurring for this mechanism.
   ii. Recovery effect: PBTI and NBTI both exhibit a recovery effect. We discuss how they are similar and how they are different.
   iii. Properties associated with HKMG: We discuss the High-K metal gate interface with itself and the silicon and how that affects the behavior of PBTI.
   iv. Methods to reduce PBTI: We describe process and design techniques for reducing PBTI.
   v. Exercises: We work several exercises for both NBTI and PBTI reliability calculations.
e. Retention/Charge Loss Mechanisms: We briefly cover memory-specific failure mechanisms like retention and charge loss.
f. Electromigration
   i. Mechanism: We describe the basic mechanism and the conditions that affect electromigration
      1. Atomic Flux
      2. Stress Gradients
      3. Surface Tension
   ii. Materials: We show the problems that occur both with aluminum and copper metallization. We show how the metal properties, along with the surrounding layers and dielectrics, affect its behavior.
      1. Aluminum and Copper effects
      2. Grain size
      3. Barrier and seed layers
      4. Surrounding dielectric effects
   iii. Exercises: We work some exercises to calculate electromigration lifetime.
g. Stress Induced Voiding: We discuss the mechanism of stress voiding, its origin, basic models for the mechanism, and how to minimize its effect.
h. Compound Semiconductor Mechanisms: We briefly cover compound semiconductor-specific mechanisms like gate diffusion, contact diffusion, and hydrogen-related issues.

Day Three (Lecture Time 8 Hours)

4. Design for Reliability
   a. Transistor Level: We discuss compact models, SPICE and other approaches to assess transistor reliability in the context of a larger design.
   b. Library Level: We discuss approaches to create models that can be used for gate-level reliability simulations.
      i. Digital Gates

   ii. Analog Gates
   iii. SRAM
   c. Macro/Block Level: We discuss approaches to minimize reliability problems at the block level like signal probability analysis and input vector control.
   d. Core/Chip Level: We discuss top-level techniques to improve reliability like adaptive VDD and adaptive body bias.
   e. Exercises: We work an exercise to show how to implement design for reliability techniques effectively.
5. Single Event Upset: We discuss Single Event Upset, its origins, and techniques for minimizing the effects of SEU on circuit operation.
6. Test Structures and Test Equipment
   a. Test Structures: We describe how the various test structures can be used not only to evaluate yield, but also how they can be used to evaluate reliability. We also describe test structures designed specifically for reliability stress tests.
      i. Parametric Test Structures
      ii. Reliability Test Structures
      iii. Self-Stressing Test Structures
   b. Test Equipment: We briefly describe the major pieces of equipment used for reliability testing.
      i. Wafer Level Testing
7. Wafer Level Testing Activities: We discuss the types of tests performed and the issues regarding test.
8. Future Reliability Challenges: We conclude the course by taking a look forward to determine what types of reliability challenges lie ahead in the future.

Chris Henderson and Paul Sakamoto will be attending SEMICON West and would be pleased to schedule a time to meet with you to discuss your training needs. Please call us at 1-505-858-0454 or email us at info@semitracks.com to schedule.

SEMICON West 2014

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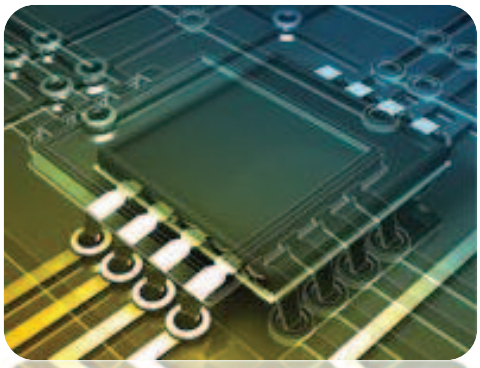
Please feel free to contact us to set up an appointment while you are there!



Upcoming Courses

(Click on each item for details)

Semiconductor Reliability
September 3 – 5, 2014 (Wed – Fri)
San Jose, California

Failure and Yield Analysis
September 8 – 11, 2014 (Mon – Thur)
San Jose, California

Feedback

If you have a suggestion or a comment regarding our courses, online training, discussion forums, or reference materials, or if you wish to suggest a new course or location, please call us at 1-505-858-0454 or Email us (info@semitracks.com).
To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered in the next newsletter, please contact Jeremy Henderson by Email (jeremy.henderson@semitracks.com).
We are always looking for ways to enhance our courses and educational materials.

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We look forward to hearing from you!