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INFOTRACKS

YOUR MONTHLY LOOK INSIDE SEMICONDUCTOR TECHNOLOGY

Semiconductor Cleanroom Technology

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In this month's Feature Article, we will begin our discussion of filtration as it applies to Semiconductor Cleanroom Technology. The ability to effectively filter particles from the atmosphere is the hallmark of a cleanroom. We accomplish this with different types of filtering materials and mechanisms, which we will discuss in more detail below.

Let's begin with a few acronyms. First, EPA stands for Efficient Particulate Air; HEPA stands for High Efficiency Particulate Air; and ULPA stands for Ultra Low Particulate Air. HEPA and ULPA filters are commonly used in semiconductor manufacturing operations. Related to the filter acronyms is the term MPPS, or Most Penetrating Particle Size. Finally, Minimum Efficiency Reporting Value, commonly known as MERV, is a measurement scale designed in 1987 by the American Society of Heating, Refrigerating and Air-Conditioning Engineers (ASHRAE) to report the effectiveness of air filters in more detail than other ratings. It is a term more commonly used with standard commercial and residential air conditioning, but is occasionally mentioned in semiconductor air conditioning applications.

WHAT'S INSIDE?

Want to take control of your learning? **See page 06**

Upcoming Courses:

- Product Qualification Overview
- Advanced CMOS/FinFET Fabrication
- IC Packaging Design and Modeling

See page 10 for more details

The HEPA filter has been in use since the 1960s. HEPA air filter technology was initially developed for the Atomic Energy Commission in the United States as a way to remove radioactive particles from reactor environments. It has since been adapted to cleanrooms in semiconductor, hard disk, and pharmaceutical manufacturing, as well as hospital surgical theaters.

Let's now discuss the HEPA filter in more detail. The HEPA filter is a multi-pleated mat of randomly arranged glass fibers. The removal efficiency of the filter is a function of several factors, including the filter thickness, and the fiber material, diameter and density. HEPA filters use four capture methods to remove particulate matter from the air: straining, impaction, interception, and diffusion. Straining works for the largest particles, or particles with a size much greater than 1 um in diameter. These particles become lodged between the fibers. Impaction works for particles that are somewhat smaller, but still greater than 1 um in diameter. These particles run into and adhere to the fibers due to the fact that their mass causes them to travel in more of a straight line than the air molecules that surround them. Interception works with the next smaller size, from about 0.1-1.0 um in size. These particles are attracted to the fibers by van der Waals forces, and then adhere to the fiber. The smallest particles, below 0.1 um, are removed by diffusion. These particles move randomly and collide with the gas molecules in the air, which is also known as Brownian movement. This random motion causes the particles to impact and adhere to the fibers. Therefore, the thicker the fiber, the more opportunities for the random motion to lead to a collision between the small particles and the fibers. Interestingly, the particles that are the hardest to remove are the ones that are around 0.3 um in size. We will discuss this interesting property in more detail in a next month's Feature Article.

The left side of Figure 1 shows a cut-away view of a HEPA filter. The frame houses a continuous sheet of the filter medium and is held in position by aluminum separators. We also show 3 of the 4 capture methods on the right side of Figure 1. Recall that the largest particles, much greater than 1 um, are removed by straining.

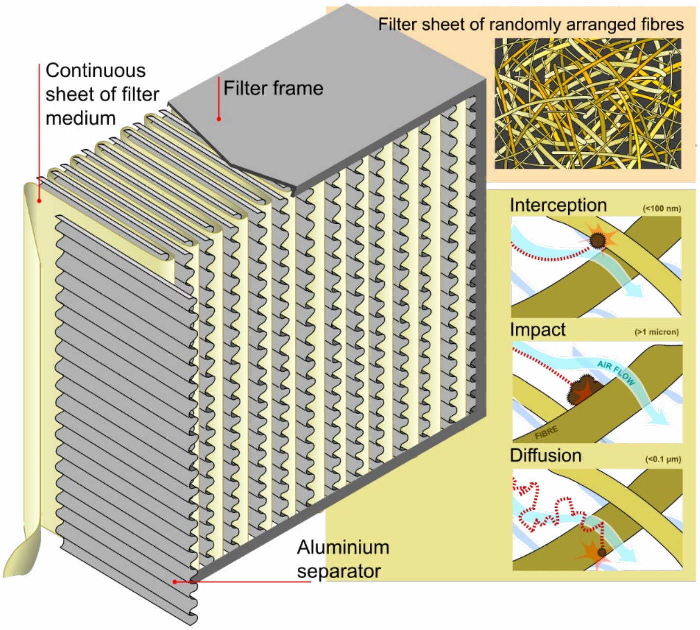


Figure 1- (Left) Cut-away view of HEPA filter, and (Right) 3 of the 4 main filtering mechanisms.

Next, let’s briefly discuss ULPA filters. As a reminder, ULPA is an acronym for "Ultra Low Particulate Air". Some engineers refer to these filters as "Ultra Low Penetration Air” filters, but that is not a common usage of the acronym. An ULPA filter can remove from the air at least 99.999% of dust, pollen, mold, bacteria and any airborne particles with a minimum particle penetration size of 0.12 µm in diameter. An ULPA filter can remove, to a large extent, but not 100%, oil smoke, tobacco smoke, rosin smoke, smog, and insecticide dust. They can also remove carbon black to some extent. In a modern semiconductor fab, some Fan filter units incorporate ULPA filters. The materials used in ULPA filters are the same as those used in HEPA filters, and both HEPA and ULPA filter media have similar designs. Like the HEPA filter, the ULPA filter media is like an enormous web of randomly arranged fibers. When air passes through this dense web, the solid particles get attached to the fibers and are eliminated from the air. Porosity is one of the key considerations of these fiber mats. Lower porosity, while decreasing the speed of filtration, increases the quality of filtered air. This parameter is measured in pores per linear inch. Figure 2, shows an example of an ULPA filter.

Figure 2- ULPA Filter (image courtesy Dekatech).

In next month’s Feature Article, we will continue our discussion of filtration for cleanrooms by discussing filtration mechanisms in more detail.

Technical Tidbit: Continuity Testing

This month's Technical Tidbit covers continuity testing. Test engineers use the continuity test to verify that there is electrical connectivity between the Device Under Test (DUT) and the Automated Test Equipment (ATE).

We show an example of the electrical connection path between the tester and the DUT in Figure 1. The test engineer programs the ATE to test the connection between the pin card electronics in the ATE to the DUT. This path goes through the pogo pin blocks, the Device Interface Board, and the Handler contactor or socket.

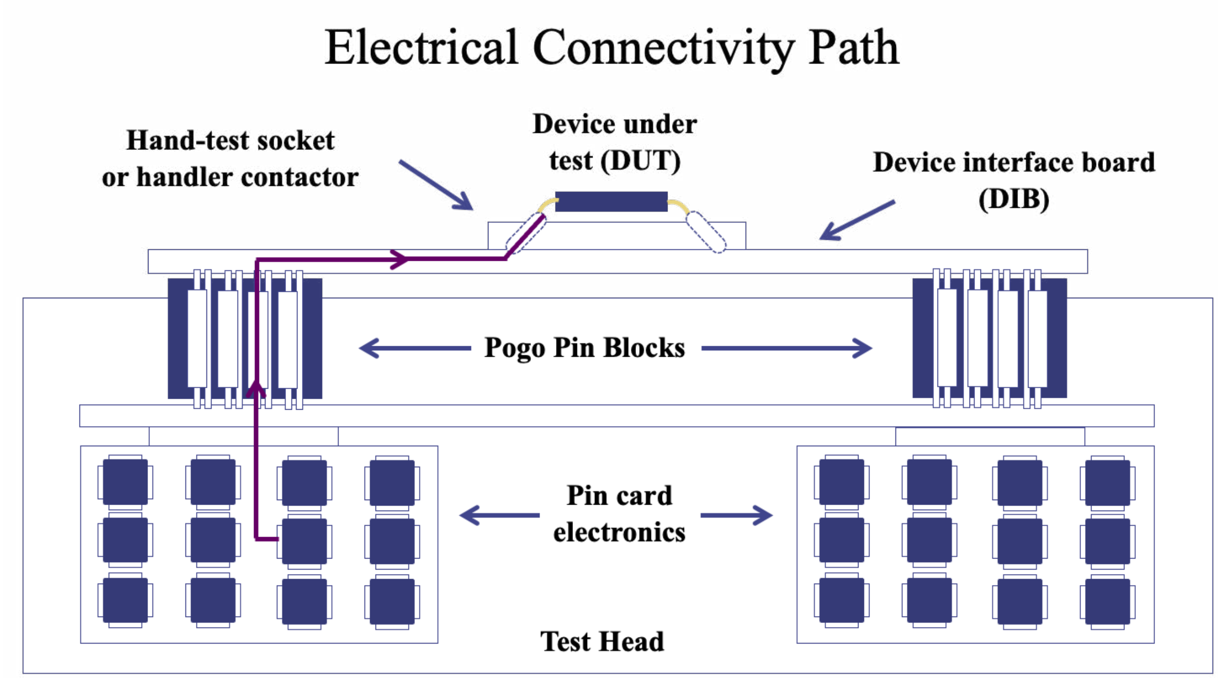


Figure 1- Diagram showing the electrical connectivity path used in continuity testing (after Burns and Roberts)

Test engineers also use continuity testing to check for the bond wire integrity. This ensures that each of the bond wires is connected to the leadframe and the bondpads, and that they are not fused. We use continuity testing to verify there are no shorts to ground or V_{CC}. We also use continuity testing to verify the no-connect pins are indeed not connected. We might use the test to check that the Thermal Pad is shorted to GND. We also use it to verify that multiple GND or V_{CC} pins are connected internally. We might also use the test during a customer return analysis to verify there is no electrical overstress damage. It is worth noting that in CMOS circuits we use the term V_{SS} for GND and V_{DD} for V_{CC}.

Figure 2 shows how continuity testing works. The red arrow indicates forcing a positive current to measure the V_{CC} diode, and the green arrow indicates forcing a negative current to measure the GND diode.

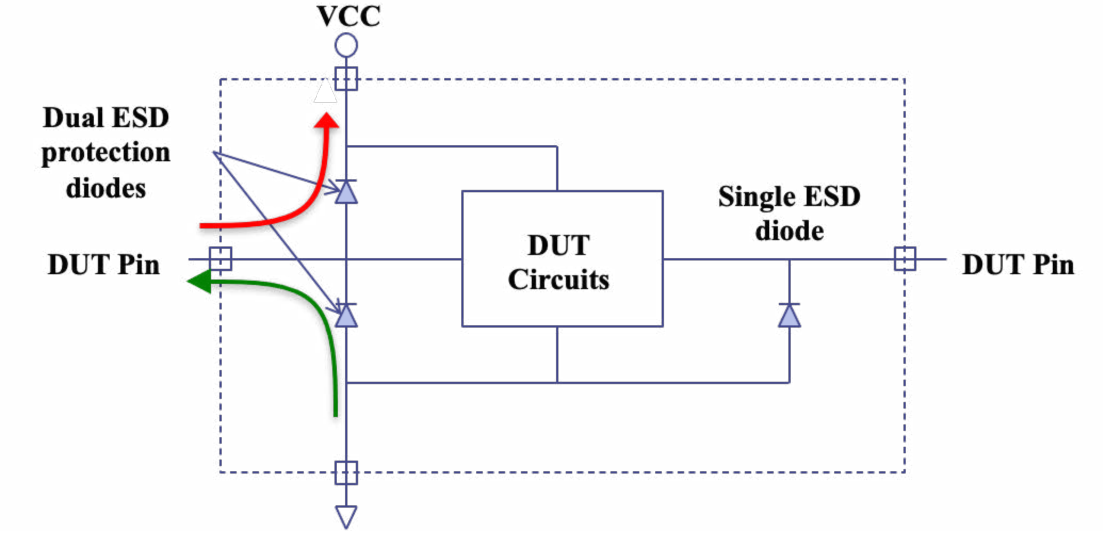
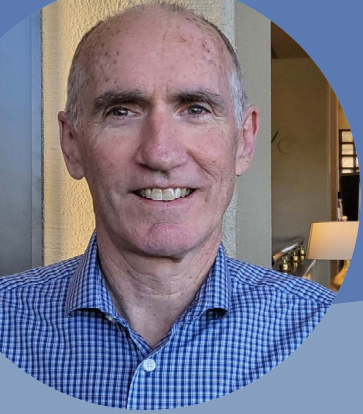


Figure 2- Diagram depicting current paths during continuity testing.

In order to detect the path from the ATE pin electronics to the DUT, we also need to complete the circuit within the DUT. We do this by detecting the presence of the ESD protection circuits on the DUT pin. There are two basic configurations for ESD input protection diodes: a two-diode configuration with one diode between the pin and V_{CC} and another between the pin and GND; and a single-diode configuration with a diode between the pin and GND. When performing continuity testing, we use a Source/Measurement Unit (SMU) to force current. We first force 0 microamps or 0 volts on all of the DUT pins to create a stable starting condition. We then force a current on the pin under test, using positive current to measure the V_{CC} diode and negative current to measure the GND diode (depicted by the red and green arrows respectively in Figure 2, as stated earlier). We typically use 100 µA to 1 mA as a forcing current as this range will settle faster on a tester, leading to somewhat faster testing times. We then wait for the measurement unit to settle and then measure the voltage. We force current and measure voltage, rather than forcing a voltage and measuring the current, because this approach is faster from a test time perspective, since it is faster to make a voltage measurement, than trying to measure a potentially low current level. At low current levels (between 100 µA and 1 mA), the voltage drop across the ESD protection diode is approximately 635 mV. It will vary depending on the size of the diode, the doping levels, and the temperature at which the measurement is performed. Therefore, a voltage near to 635 mV is a normal, passing value. If the voltage is 0 V or close to 0 V, this indicates a short, which is a failure. If the voltage is the compliance voltage (i.e., 10 V on a 10 V range), this indicates an open, which is a failure.



Ask The Experts

Q: When silicon's ability as a semiconductor, or the size of transistors cannot be minimized any more, what is the next material that can be used as a suitable successor for silicon?

A: Right now, there is no good replacement material for silicon. Silicon has a number of properties that make it better than almost anything else out there. For example, it is straightforward to make large single crystals of silicon; it is straightforward to form an oxide on the surface of silicon, but most importantly, silicon is a low-cost material. Furthermore, in the most advanced chips made today, the silicon substrate is basically just a platform for creating the rest of the chip, so, conceivably in the future, it may be such that the silicon is just the substrate, and we build everything in different materials on top of the silicon substrate.

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Course Spotlight: ADVANCED CMOS/FINFET FABRICATION

OVERVIEW

Semiconductor and integrated circuit developments continue to proceed at an incredible pace. For example, today's microprocessor chips have one thousand times the processing power of those a decade ago. These challenges have been accomplished because of the integrated circuit industry's ability to track something known as Moore's Law. Moore's Law states that an integrated circuit's processing power will double every two years. This has been accomplished by making devices smaller and smaller. The question looming in everyone's mind is "How far into the future can this continue?" ***Advanced CMOS/FinFET Fabrication*** is a 1.5-day course that offers detailed instruction on the processing used in a modern integrated circuit, and the processing technologies required to make them. We place special emphasis on current issues related to manufacturing the next generation devices. This course is a must for every manager, engineer and technician working in the semiconductor industry, using semiconductor components or supplying tools to the industry.

By concentrating on the latest developments in CMOS and FinFET technology, participants will learn why FinFETs are fast becoming the technologies of choice at feature sizes below 20nm. Our instructors work hard to explain semiconductor processing without delving heavily into the complex physics and materials science that normally accompany this discipline.

Participants learn basic but powerful aspects about CMOS fabrication and FinFET technology. This skill-building series is divided into four segments:

1. Front End Of Line (FEOL) Overview. Participants study the major developments associated with FEOL processing, including Ion Implantation, Rapid Thermal Annealing (RTA) for implants and silicides, and Pulsed Plasma Doping. They also study alternate substrate technologies like SOI as well as High-k/Metal Gates for improved leakage control.
2. Back End Of Line (BEOL) Overview. Participants study the major developments associated with BEOL processing, including copper metallization and Low-k Dielectrics. They learn about why they're necessary for improved performance.
3. FinFET Manufacturing Overview. Participants learn how semiconductor manufacturers are currently processing FinFET devices and the difficulties associated with three-dimensional structures from a processing and metrology standpoint.
4. FinFET Reliability. They also study the failure mechanisms and techniques used for studying the reliability of these devices.

COURSE OBJECTIVES

1. The seminar will provide participants with an in-depth understanding of Bulk technology, SOI technology and the technical issues.
2. Participants will understand how Hi-K/Metal Gate devices are manufactured.
3. Participants will also understand how FinFET devices are manufactured.
4. The seminar provides a look into the latest challenges with copper metallization and Low-k dielectrics.
5. Participants will understand the difficulties associated with non-planar structures and methods to alleviate the problems.
6. Participants will be able to make decisions about how to evaluate FinFET devices and what changes are likely to emerge in the coming years.
7. Participants will briefly learn about IC reliability and the failure modes associated with these devices.
8. Finally, the participants see a comparison between FinFETs and new alternatives (such as Gate All Around (GAA) structures and nanosheets).

COURSE OUTLINE

1. Advanced CMOS Fabrication – Introduction
2. Front End Of Line (FEOL) Processing
    a. SOI and FD-SOI
    b. Ion Implantation and Rapid Thermal Annealing
    c. Pulsed Plasma Doping
    d. Hi-K/Metal Gates
    e. Processing Issues
        i. Lithography
        ii. Etch
        iii. Metrology
3. Back End Of Line (BEOL) Processing
    a. Introduction and Performance Issues
    b. Copper
        i. Deposition Methods
        ii. Liners
        iii. Capping Materials
        iv. Damascene Processing Steps
    c. Lo-k Dielectrics
        i. Materials
        ii. Processing Methods
    d. Reliability Issues
4. FinFET Manufacturing Overview
    a. Substrates
        i. Bulk
        ii. SOI
    b. FinFET Types
    c. Process Sequence
    d. Processing Issues
        i. Lithography
        ii. Etch
        iii. Metrology
5. FinFET Reliability
    a. Defect density issues
    b. Gate Stack
    c. Transistor Reliability (BTI and Hot Carriers)
    d. Heat dissipation issues
    e. Failure analysis challenges
6. Future Directions for FinFETs
    a. Comparison of FinFETs and other Techniques (GAA, Nanosheets) – Are FinFETs a better choice?
    b. Scaling

Upcoming Courses:

Public Course Schedule:

Product Qualification Overview - September 11, 2023 (Mon.) | Phoenix, Arizona - $695

Advanced CMOS/FinFET Fabrication - September 25-26, 2023 (Mon.-Tues.) | Phoenix, Arizona - $995

IC Packaging Technology - January 23-24, 2024 (Tues.-Wed.) | Phoenix, Arizona - $1,295

Advanced CMOS/FinFET Fabrication - January 29-30, 2024 (Mon.-Tues.) | Phoenix, Arizona - $995

Wafer Fab Processing - February 26-29, 2024 (Mon.-Thurs.) | Munich, Germany - $2,095

Failure and Yield Analysis - March 4-7, 2024 (Mon.-Thurs.) | Munich, Germany - $2,095

Semiconductor Reliability and Product Qualification - March 11-14, 2024 (Mon.-Thurs.) | Munich, Germany - $2,095

Defect-Based Testing - March 20-21, 2024 (Wed.-Thurs.) | Munich, Germany - $1,195

Webinar Schedule:

IC Packaging Design and Modeling - September 18 - 21, 2023 (Mon. – Thurs.) | - $600

Have an idea for a course? If you have a suggestion or a comment regarding our courses, online training, discussion forums, or reference materials, or if you wish to suggest a new course or location, please email us at info@semitracks.com

To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered, please contact Jeremy Henderson at jeremy.henderson@semitracks.com

We are always looking for ways to enhance our courses and educational materials and look forward to hearing from you!