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InfoTracks

Semitracks Monthly Newsletter

Oxidation Part 2

By Christopher Henderson

In our continuing series, we will discuss the subject of oxidation. Last month, we discussed oxidation kinetics. This month, we'll discuss oxidation systems in more detail.

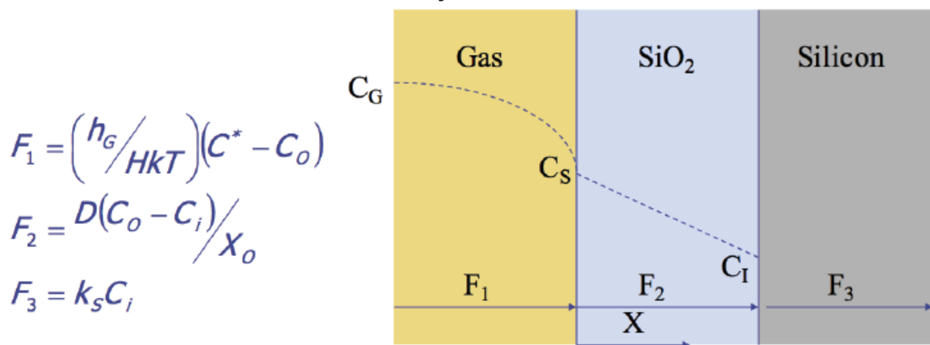

Figure 10. Deal-Grove oxidation model.

There are three steps in the oxidation model. The first step is the gas transfer of oxygen from the ambient environment to the gas/oxide interface. The second step is the diffusion of oxygen across the oxide layer. The third step is the chemical reaction that occurs at the silicon surface. The equations for each step are shown in Figure 10. F1 is the gas transport equation, F2 is the oxide diffusion equation, and F3 is the oxygen/silicon reaction equation. H_G is the mass transfer coefficient in gas, and H is

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Henry's law constant. C* is defined as $H \times p_G$, where p_G is the partial pressure of the oxidizing species in the bulk of the gas. D is the diffusivity of the oxidizing species in SiO_2 and k_s is the chemical surface reaction rate constant for oxidation. In the steady state condition F1 should equal F2 which should also equal F3. When the equations are set equal to one another, one can solve for the concentration at the surface of the oxide and the concentration at the interface between the silicon and the silicon dioxide. When the diffusion constant D is very small, the flux of oxygen through the silicon dioxide is small compared to the reaction rate at the interface. This is known as the diffusion rate controlled case, indicated by the line shown here. When the diffusion constant D is very large, an ample supply of oxygen can reach the interface. This is a reaction rate controlled case.

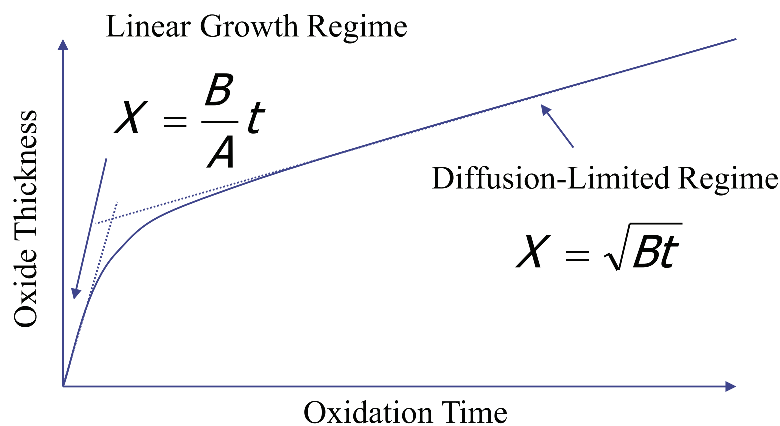


Figure 11. Oxide growth rate.

If one solves for equation F3 (the reaction rate at the silicon/silicon dioxide surface) after applying the appropriate boundary conditions, one can obtain a solution for X, or the thickness of the oxide. This is a somewhat complicated differential equation boundary value problem, so we will not work it here. Basically, the thickness can be described under two different conditions: one where the time scale is quite long, and one where the time scale is short. The short time scale describes the initial growth region or the reaction rate limited case, and the long-time scale describes the diffusion limited case. For short times where t plus τ is much less than $A^2/4B$, $X_O = B/A(t + \tau)$, where B/A is called the linear rate constant. For very long times where t is much greater than $A^2/4B$, $X_O^2 = B \times t$, where B is called the parabolic rate constant. The graph in Figure 11 shows the composite of the two growth regimes, where oxide thickness is plotted against oxidation time.

$$B = C_1 \, exp\left(-\frac{E_1}{kT}\right), \frac{B}{A} = C_2 \, exp\left(-\frac{E_2}{kT}\right)$$

Ambient	B	B/A
Dry O2	$C_1=7.72\times10^2 \mu m^2 hr^{-1}$	$C_2=6.23\times10^6 \mu m\text{-}hr^{-1}$<111> $C_2=3.71\times10^6 \mu m\text{-}hr^{-1}$<100>
	$E_1=1.23eV$	$E_2=2.00eV$
Wet O2	$C_1=2.14\times10^2 \mu m^2 hr^{-1}$	$C_2=8.95\times10^7 \mu m\text{-}hr^{-1}$<111> $C_2=5.33\times10^7 \mu m\text{-}hr^{-1}$<100>
	$E_1=0.71eV$	$E_2=2.05eV$
H2O	$C_1=3.86\times10^2 \mu m^2 hr^{-1}$	$C_2=1.63\times10^8 \mu m\text{-}hr^{-1}$<111> $C_2=9.70\times10^7 \mu m\text{-}hr^{-1}$<100>
	$E_1=0.78eV$	$E_2=2.05eV$

Rate constants describing silicon oxidation kinetics at 1 atm total pressure

Figure 12. Rate constants under oxidation conditions.

In order to solve for B and A, one must first know the values of C1, C2, E1, and E2. These values can be determined experimentally. This table shows values for the four constants under three different oxidation conditions: dry oxygen, wet oxygen, and steam. Wet oxygen is a condition where oxygen is bubbled through water prior to entering the oxidation furnace. These constants are for one atmosphere total pressure. The constant C2 is different depending on the crystal face exposed. In general, the <111> crystal face exposed results in a C2 constant that is about 1.68 times greater than with the <100> face exposed.

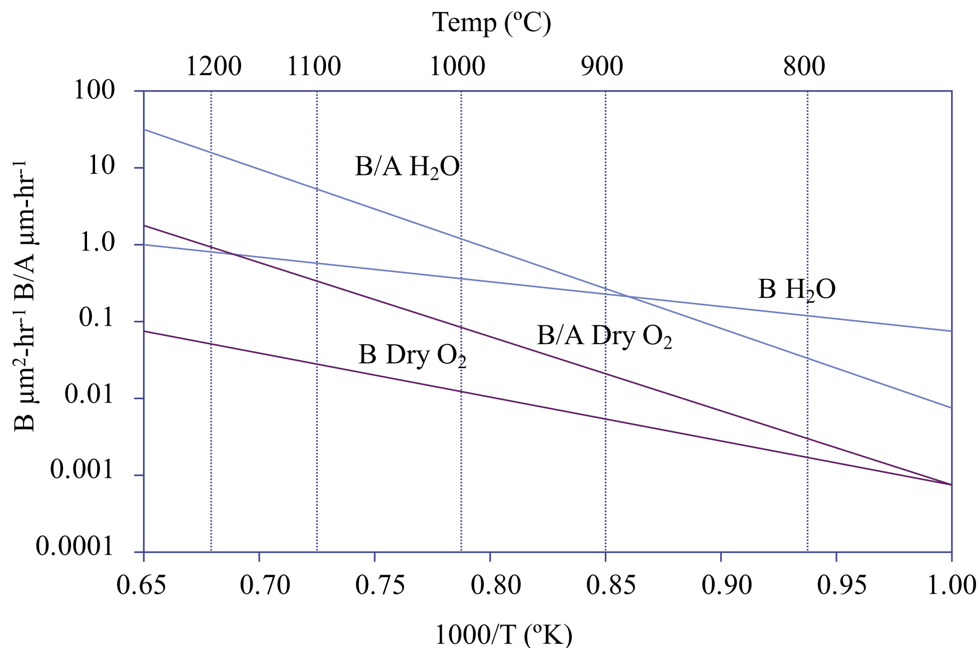


Figure 13. Rate constants as a function of temperature.

Figure 13 shows the rate constants B and B/A as a function of temperature. In general, the rate constants trend higher with increasing temperature. Also, the B/A rate constant has a higher slope than the B constant.

There are three basic factors which affect the oxidation process at the surface: temperature, availability of the oxidizing species, and the surface potential of the wafer. As is the case with many reactions, the rate of oxidation is greater at higher temperatures. The availability of oxygen at the surface is also important. Finally, the surface potential or surface energy can come into play. The crystal orientation, the silicon doping concentration, and any pre-oxidation surface treatments can affect the electro-chemical potential of the surface, increasing or decreasing the rate of reaction.

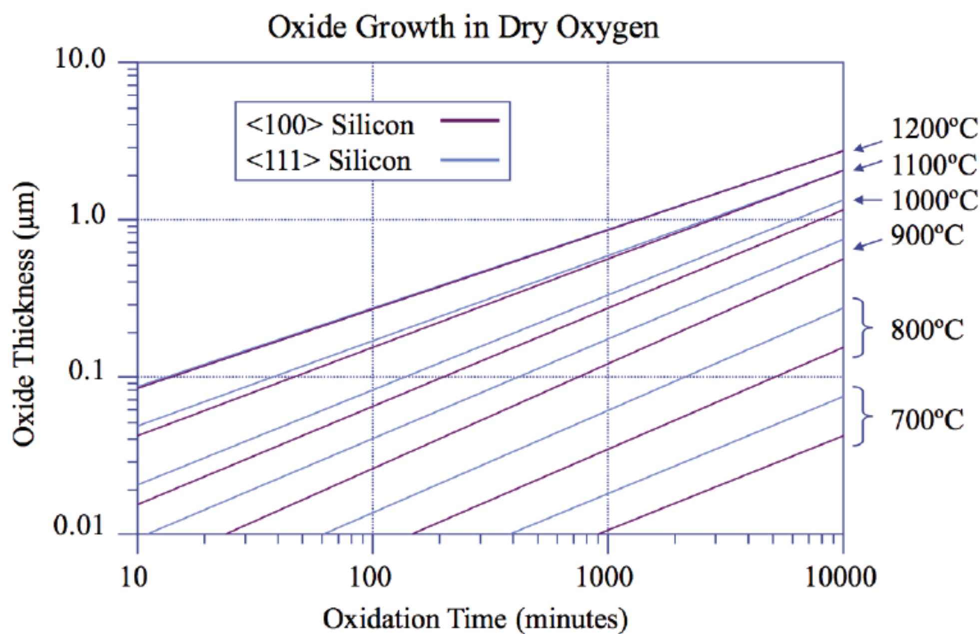


Figure 14. Temperature and crystal orientation effects: oxide growth in dry oxygen.

This graph shows the oxide growth in dry oxygen. The graph shows the oxide thickness as a function of oxidation time for several different growth temperatures. Notice that the oxide growth is approximately a straight line on a log-log plot. Also notice that the growth rates on <111> silicon are slightly faster than on <100> silicon. This is because the electro-chemical potential is slightly greater for the <111> face.

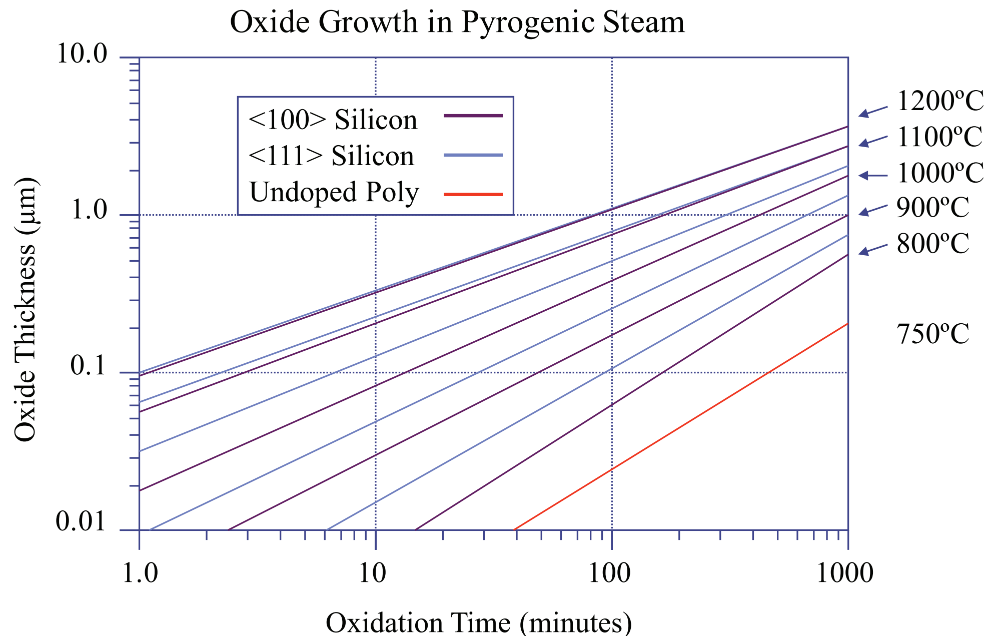


Figure 15. Temperature and crystal orientation effects: oxide growth in pyrogenic steam.

This graph shows the oxide growth in pyrogenic steam. The graph shows the oxide thickness as a function of oxidation time for several different growth temperatures. Notice that the oxide growth is approximately a straight line on a log-log plot. The growth rates are about a factor of ten faster than shown on the previous slide in dry oxygen. Also notice that the growth rates on <111> silicon are slightly faster than on <100> silicon. This is because the electro-chemical potential is slightly greater for the <111> face. We also show a growth line for undoped polysilicon at 750°C.

There are three major factors that affect the availability of the oxidizing species. They include diffusivity, solubility and pressure. In terms of diffusivity, oxygen diffuses much faster through silicon dioxide than water molecules. The water molecule with its angled shape occupies more volume than the oxygen molecule. This makes it more difficult for the water molecule to move through the silicon dioxide structure. On the other hand, water is approximately 600 times more soluble in silicon dioxide than is oxygen. Silicon dioxide readily traps and holds water, while oxygen tends to diffuse away quickly. Pressure is the third factor affecting oxidation. Increasing pressure from the outside environment increases the concentration of the species in the reaction zone.

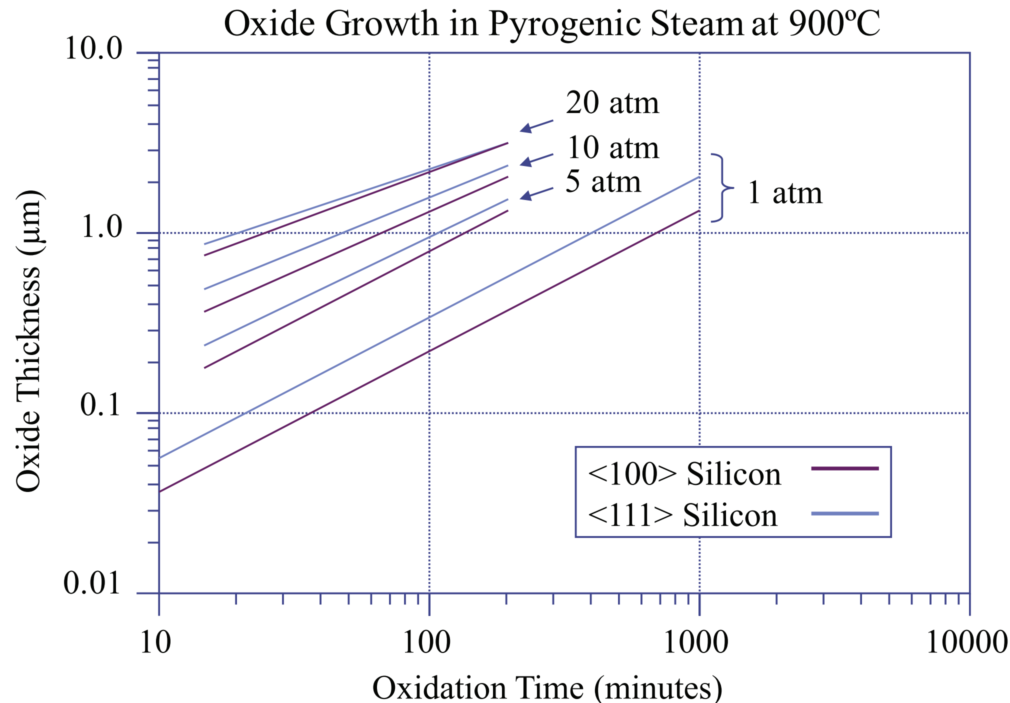


Figure 16. Pressure effects.

This graph shows the effects of pressure on oxide growth in pyrogenic steam. The graph shows the oxide thickness as a function of oxidation time for several different pressures. Notice that the oxide growth rate increases as the ambient pressure is increased.

There are several factors that change the surface potential of the silicon surface. These are crystal orientation, silicon doping concentration, and surface treatment. The <111> plane oxidizes the fastest while the <100> plane oxidizes the slowest. The bonds coming out of the <111> plane more easily accept oxygen. Higher surface doping concentrations give higher oxidation rates. The silicon to silicon bonds are compressed and/or stretched by substitutional impurities. These bonds are more easily broken to accept oxygen than silicon to silicon bonds in an area where the lattice is free from impurities. Finally, surface treatments such as a hydrochloric acid treatment can increase the growth rate. The acid oxidizes the surface, allowing oxygen to bond more easily.

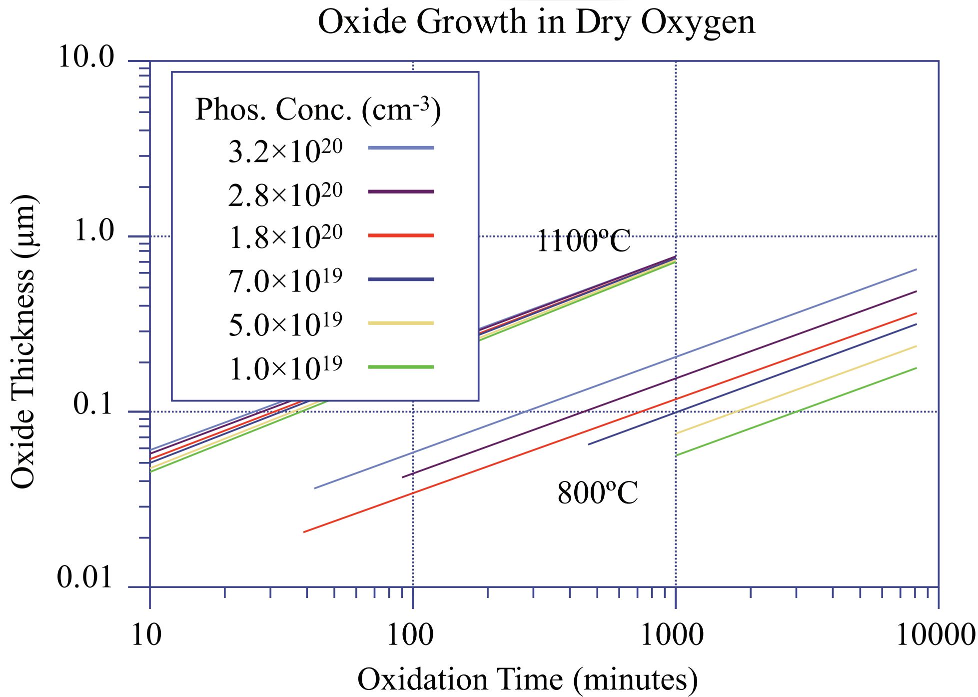


Figure 17. Doping effects on oxidation.

This graph shows the doping effects on oxidation. Notice that as the concentration of phosphorus increases, the growth rate of the oxide increases. The effect is more pronounced at lower temperatures. At higher temperatures, one can see that the oxidation lines are closely packed together.

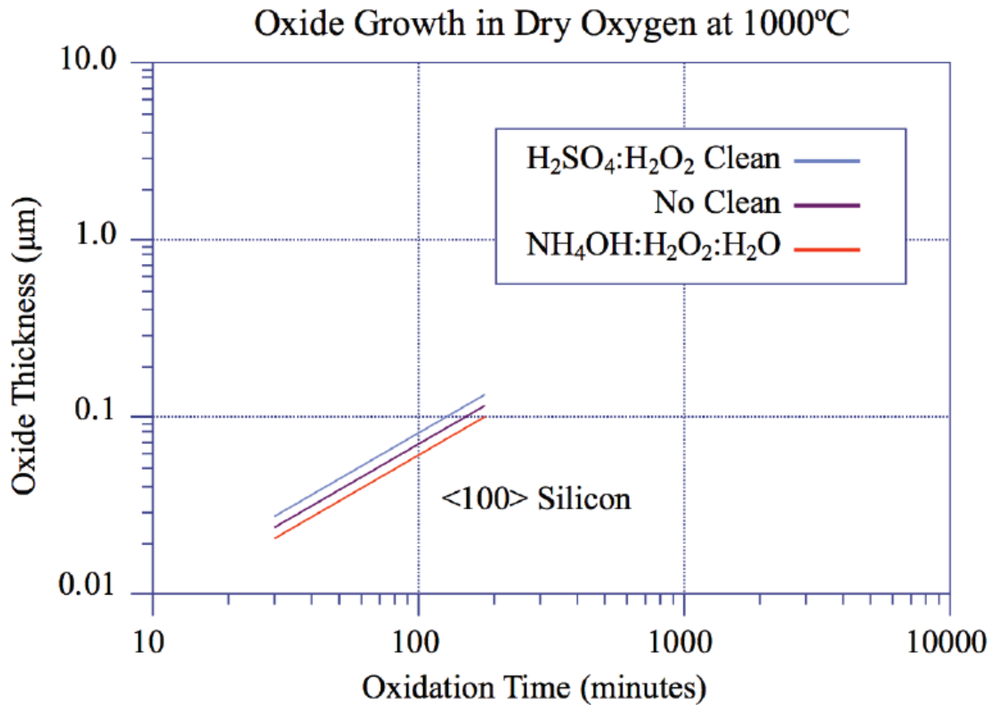


Figure 18. Pre-treatment effects on oxidation.

This graph shows the effects of two different pre-treatments, and no pre-treatment of the silicon surface. The sulfuric acid–hydrogen peroxide clean oxidizes the surface, allowing faster oxide growth, while the ammonium hydroxide–hydrogen peroxide–water clean makes the surface more alkaline, reducing the growth rate.

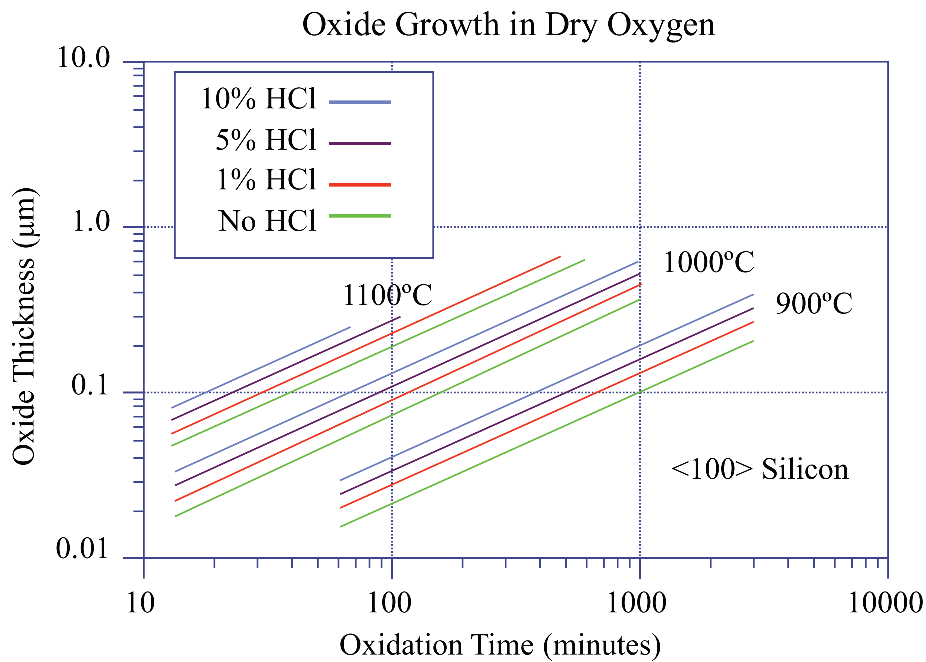


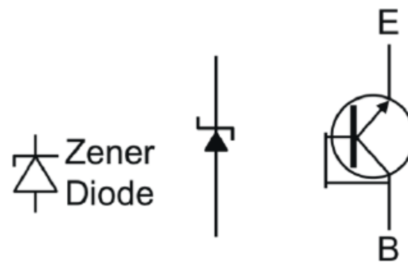
Figure 19. HCI effects on oxidation.

This graph shows the effects of oxide growth when the silicon surface is exposed to hydrochloric acid. Researchers have studied the effects of chlorine gas on silicon dioxide growth for a number of years, since chlorine can reduce fixed and mobile charge in the silicon dioxide, increase the lifetime of the minority carriers, and reduce the density of oxidation-induced stacking faults in the silicon below. Chlorine can also cause the oxide reaction rate to increase, but the reasons for this are not well understood. Researchers have also observed the buildup of chlorine at the silicon/silicon dioxide interface.

Technical Tidbit

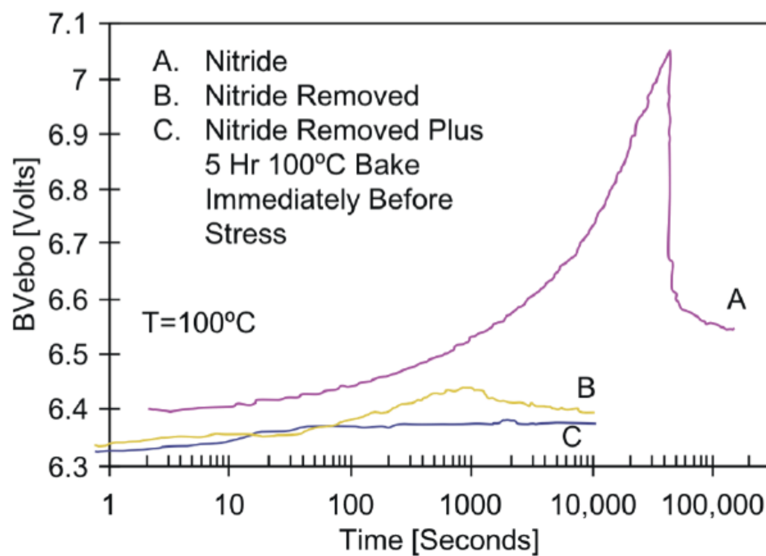
Emitter-Base Junction Breakdown (Vz) Drift

In bipolar analog circuit designs, diode connected transistors with reverse biased emitter-base junctions are sometimes used as Zener diodes with 6-7 V Zener breakdown voltages (Vz). In the past, these were commonly used to make reference voltage supplies. Through observation, engineers discovered that putting the surface diode into breakdown caused a small shift in the breakdown voltage. But when the device used a nitride passivation overcoat, the shift in Vz was more significant. Furthermore, counter to normal behavior, baking a device with this problem actually made the problem worse, further increasing Vz when power was reapplied. Interestingly, when engineers created a window in the nitride over these diodes, Vz improved and stabilized, by letting trapped Hydrogen escape. The basic concept is that avalanche breakdown of the emitter-base junction breaks the silicon-hydrogen bonds, and activates H+ that moves into the silicon, compensating the p-type boron doping and making it less p-type. The surface doping on the lightly doped side determines the breakdown voltage, so this causes Vz to increase.



The following graph shows the behavior seen with this problem. For more information, the reader should refer to this technical paper:

James Dunkley, *et al* (Silicon Systems—now TI), "Hot Electron Induced Hydrogen Compensation of Boron Doped Silicon Resulting from Emitter Base Avalanche," IEDM 1992, 785 – 788.



Ask the Experts

Q: I am not sure if I have a moisture or a mobile ion problem. How do I design a stress test to distinguish between mobile ions and moisture?

A: The main problem with this issue is that both moisture ingression and mobile ions are thermally activated. What is worse is that their thermal activation can be almost the same. Moisture ingression problems typically have an activation energy of ~0.75eV, while the mobile ion sodium also has an activation energy of ~0.75eV (see examples in JEP122). So it is going to be almost impossible to design a procedure to remove the moisture without modifying the sodium ions. A better option would be to create a procedure for detecting sodium. In that case you could do UHAST to redistribute the mobile ions, while leaving the moisture in place (if it is already there). This approach also has problems. If there is no moisture, then UHAST can cause moisture to penetrate into the device and complicate the detection of sodium. However, I think you could factor this out if you use control samples (that don't contain ion contamination).

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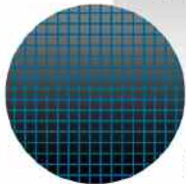

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Spotlight: CMOS, BiCMOS, and Bipolar Process Integration

OVERVIEW

Semiconductor and integrated circuit developments continue to proceed at an incredible pace. For example, today's mixed-signal chips perform a wide range of applications unheard of a few years ago, including wireless applications, high speed communications, and signal processing. These challenges have been accomplished because of the integrated circuit industry's ability to track something known as Moore's Law. A corollary to Moore's Law is that frequencies on mixed-signal devices continue to rise. This has been accomplished by making devices smaller and smaller. The question looming in everyone's mind is "How far into the future can this continue?" ***CMOS, BiCMOS, and Bipolar Process Integration*** is a 3-day course that offers detailed instruction on the physics behind the operation of a modern mixed-signal integrated circuit, and the processing technologies required to make them. We place special emphasis on current issues related to designing and manufacturing the next generation devices. This course is a must for every manager, engineer and technician working in the semiconductor industry, using semiconductor components or supplying tools to the industry.

By focusing on the fundamentals of transistor operation and performance, participants will learn why advances in the industry are occurring along certain lines and not others. Our instructors work hard to explain how semiconductor devices work without delving too heavily into the complex physics and mathematical expressions that normally accompany this discipline.

Participants learn basic but powerful aspects about the semiconductor industry. This skill-building series is divided into three segments:

1. **Basic Device Operation.** Participants learn the fundamentals of transistor operation. They learn why BiCMOS devices dominate the mixed-signal industry today.
2. **Fabrication Technologies.** Participants learn the fundamental manufacturing technologies that are used to make modern integrated circuits. They learn the typical CMOS, Bipolar and BiCMOS process flows used in integrated circuit fabrication.
3. **Current Issues in Process Integration.** Participants learn how device operation is increasingly constrained by three parameters. They also learn about the impact of using new materials in the fabrication process and how those materials may create problems for the manufacturers in the future.
4. **An Overview of Issues Related to Process Integration.** Participants learn about the image of new materials, yield, reliability and scaling on technology and process integration. They receive an overview of the major reliability mechanisms that affect silicon ICs today.

COURSE OBJECTIVES

1. The seminar will provide participants with an in-depth understanding of the semiconductor industry and its technical issues.
2. Participants will understand the basic concepts behind transistor operation and performance.
3. The seminar will identify the key issues related to the continued growth of the semiconductor industry.

4. The seminar offers a wide variety of sample problems that participants work to help them gain knowledge of the fundamentals of device operation and manufacturing.
5. Participants will be able to identify basic and advanced technology features on semiconductor devices. This includes features like silicon-germanium, emitter islands, copper, and low-k dielectrics.
6. Participants will understand how reliability, power consumption and device performance are interrelated.
7. Participants will be able to make decisions about how to construct and evaluate new CMOS, BiCMOS, and bipolar technologies.

INSTRUCTIONAL STRATEGY

By using a combination of instruction by lecture, classroom exercises, and question/answer sessions, participants will learn practical information on semiconductor devices and the operation of this industry. From the very first moments of the seminar until the last sentence of the training, the driving instructional factor is **application**. We use instructors who are internationally recognized experts in their fields that have years of experience (both current and relevant) in this field. The handbook offers hundreds of pages of additional reference material the participants can use back at their daily activities.

COURSE OUTLINE

Day 1

1. Introduction
2. Basic Semiconductor Concepts
   a. Diffusion/Drift
   b. PN Junction Diodes
   c. Bipolar Junction Transistor
   d. MOS Transistor
   e. Additional Concepts
      i. Avalanche Breakdown
      ii. Zener Breakdown
      iii. Tunneling
      iv. Schottky Barriers
3. General Scaling Issues
   a. Constant Field Scaling/Constant Voltage Scaling
   b. Process Integration Issues
      i. Transistors (Ion vs Ioff, Mobility Enhancement, short channel effects, etc.)
      ii. Interconnect (RC delay, power dissipation, etc.)
   c. Limitations to Scaling

Day 2

4. Conventional CMOS
    a. Well/Substrate Engineering
    b. Device Isolation
    c. Gate Stack
    d. Contacts/Silicide
    e. Scaling Issues
    f. Basic CMOS Flow Presentation
5. Conventional BiCMOS
    a. Bipolar Transistor Fundamentals
    b. BiCMOS Process Overview
    c. Scaling and Limitations
    d. Basic BiCMOS Flow Presentation
6. Bipolar Enhancement Techniques
    a. SiGe
    b. SiGe:C
7. Power Technologies
    a. LDMOS
    b. DECMOS
    c. BCD
8. Additional Analog Circuit Elements
    a. Resistors
    b. Capacitors
    c. JFETs

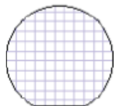
Day 3

9. Interconnects
    a. Aluminum Interconnects, Issues
    b. Copper Interconnects, Issues
    c. Low-k Dielectrics
10. CMOS/Bipolar/BiCMOS Reliability Considerations
    a. Electrostatic Discharge
    b. Electromigration and Stress Migration
    c. Soft Errors, Plasma Damage
    d. Dielectric Reliability
    e. Bias Temperature Instabilities
    f. Hot Carrier Reliability
    g. Burn-In

11. Yield Considerations
    a. Yield Detractors
    b. Models
    c. Monitors
12. Conclusion/Wrap Up

You may want to stress some aspects more than others or conduct a simple one-day overview course. Many of our clients seek ongoing just-in-time training that builds in-depth, advanced levels of reliability expertise. We'll work with you to determine the best course of action and create a statement of work that emulates the very best practices of semiconductor reliability analysis.

Our instructors are active in the field and they practice the disciplines daily. Please give us a call (505) 858-0454 or drop us an e-mail (info@semitracks.com).



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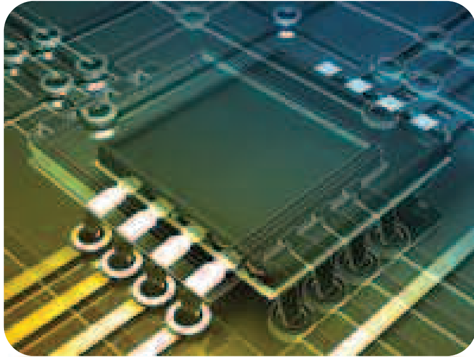

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If you have a suggestion or a comment regarding our courses, online training, discussion forums, or reference materials, or if you wish to suggest a new course or location, please call us at 1-505-858-0454 or Email us (info@semitracks.com).

To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered in the next newsletter, please contact Jeremy Henderson by Email (jeremy.henderson@semitracks.com).

We are always looking for ways to enhance our courses and educational materials.

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To post, read, or answer a question, visit our forums.
We look forward to hearing from you!

Upcoming Courses

(Click on each item for details)

CMOS, BiCMOS and Bipolar Process Integration

September 10 – 12, 2018 (Mon – Wed)
San Jose, California, USA

Wafer Fab Processing

September 17 – 20, 2018 (Mon – Thur)
San Jose, California, USA

Failure and Yield Analysis

October 29 – November 1, 2018 (Mon – Thur)
Singapore