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Lead Free Solders—General Issues

By Christopher Henderson

In this section we will discuss some of the technical challenges associated with the use of lead-free solders. Lead-free solders are now in widespread use throughout the industry as a result of recent regulations on hazardous materials.

First, we will cover the objectives for this section. Next, we'll discuss the transition to lead free solders. We'll then discuss lead free materials properties, the challenges associated with using these materials, and their reliability. Finally, we'll summarize our findings.

The objective of this section is to provide an overview of the challenges associated with the use lead-free solders in today's electronics. We will also report on the reliability of these materials. Specifically, we will cover silver-tin-copper solders, sometimes called SAC solders, since they are the most widely used lead free solders today. Last, we will identify some gaps in the performance of these materials and areas for further study.

The biggest motivation for the lead-free solder transition is the advent of government regulations. Because lead is identified as a hazardous substance, government agencies are trying to reduce the amount of lead use by imposing restrictions. This directly impacts the electronics industry, since traditional solders use lead as a constituent of the solder alloy. The European Union has taken the lead to remove lead, and the rest of the world has followed suit. There are some exemptions, but the majority of electronic systems are now required to be free from lead solders. The Removal of Hazardous Substances,

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commonly called RoHS, greatly restricts the use of lead in electronic products that were introduced after July 1, 2006.

First, let's consider what we do know about lead free solders. Because of considerable research in the early 2000s and earlier, we understand the melting and freezing characteristics as well as the microstructure of a number of lead free solders. We also understand the mechanical properties of these solders. These properties have an impact on the solder joint's reliability. Some lead free solders have improved fatigue performance compared with standard lead tin solders. Those same solders also have reduced dynamics performance. The biggest problem with solder joints is fatigue. And fatigue is an issue with lead free solders as well. This fatigue can be reduced by managing the overall thermal dissipation environment through the right design choices and appropriate packaging and heat sink materials. It can also be mitigated through appropriate board design and test methods.

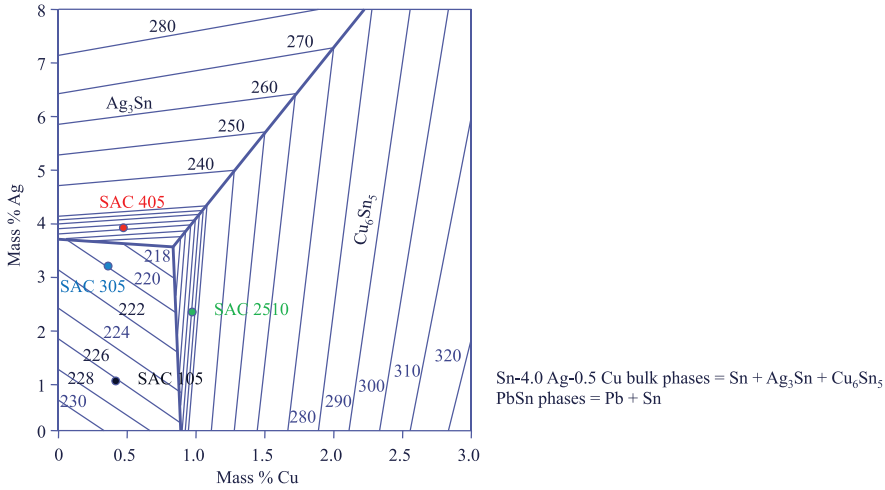


Figure 1. Ternary phase diagram and several common solder alloys for the Tin-Silver-Copper (SnAgCu) family.

Over the past several years, the silver-tin-copper solder system has become the preferred solder alloy for lead free applications. The mechanical properties, reflow temperatures and processing options provide reasonable performance. This two-dimensional ternary alloy chart in Figure 1 shows the phases and melting temperatures associated with the system. Some common SAC solder alloys are shown on the chart. Lead free SAC solders normally have between 1 and 8 percent silver. They also exhibit variations in microstructure, so their properties vary somewhat as well. One obvious variation is the melting temperature. SAC 305 has a melting temperature of 220°C, while SAC 405 is approximately 223, SAC 305 and SAC 2510 are both 226.

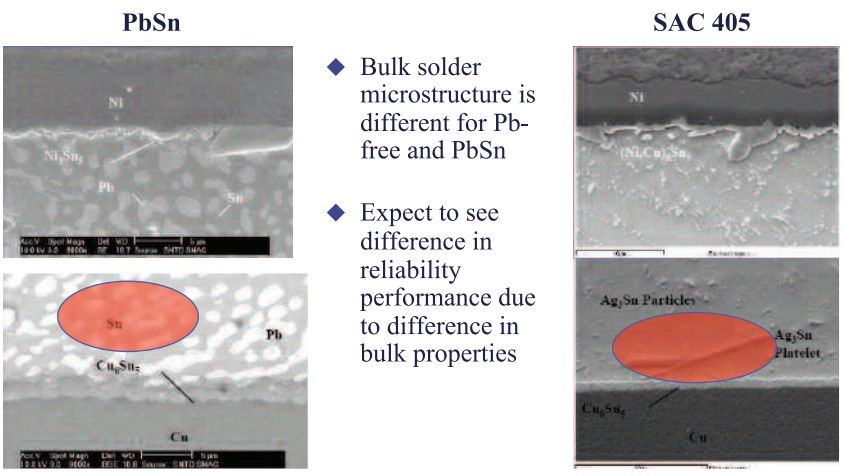


Figure 2. Microstructure for Lead-Tin (left) and a lead-free (SAC 405) (right) solders.

In Figure 2, if we look at the lead-tin alloy (left) and the silver-copper-tin alloy (right) at the microscale, we notice that the structure is different. Notice that the lead-tin alloy is such that the lead forms bubbles or large smooth-shaped regions within the tin matrix. In the SAC 405 solder on the right, the silver-tin phase tends to form particles, or in some instances platelets in the tin matrix. The differences in microstructure lead to different properties that affect the reliability of the solders.

Property	PbSn	SnAgCu	Comments
Melting Point	183°C	217 - 219°C	Sn-4.0 Ag-0.5 Cu
Young's Modulus	35 Gpa	53 Gpa	Sn-4.0 Ag-0.5 Cu
Tensile Strength (20°C at 0.004s^{-1})	40 N/mm^2	48 N/mm^2	Sn-3.8 Ag-0.7 Cu
Joint Shear Strength (20°C at 0.1mm/min)	23 N/mm^2	27 N/mm^2	Sn-3.8 Ag-0.7 Cu
Creep Strength (100°C at 0.1mm/min)	1.0 N/mm^2	5.0 N/mm^2	Sn-3.8 Ag-0.7 Cu

Figure 3. Material properties—PbSn vs. SnAgCu.

If we look at the materials properties of the two solders in Figure 3, we see some differences as well. Notice that the melting point of the tin-silver-copper solder is more than 30 degrees higher than the lead-tin solder. The Young's modulus is higher, as well as the tensile strength, shear strength and creep strength. This means that the SAC 405 solder is stiffer and stronger than the lead-tin solder. This gives better fatigue performance, but reduced dynamics performance. Although good fatigue performance is useful, thermal cycling associated with electronics usage requires better dynamics performance. Temperature swings cause packaging and board materials to expand and contract, so the solder needs good dynamics performance to handle this behavior.

Based on the materials properties and microstructure, there are five major challenges associated with the tin-silver-copper lead-free solder system. The first one is the higher reflow temperature compared to lead-tin solders. This can lead to component and printed circuit board damage. The second one is surface finish. Surface finish properties strongly affect corrosion and ultimately the solder joint reliability. The third is mechanical integrity. Lead-free solders are much stiffer than lead-tin solders, and this limits the amount of flexing that a printed circuit board can withstand. The fourth is reliability. Solder fatigue and temperature dwell times can impact reliability since leaded and lead-free solders respond differently. The fifth is the formation of tin whiskers. Most manufacturers use 100 percent tin plating on the leads to provide a wettable surface for the lead-free solder. Pure tin exhibits high levels of stress when plated on a lead, and this can lead to tin whiskers as the tin attempts to relieve the stress through extrusion. The industry is actively studying this failure mechanism through the Joint Electron Device Engineering Council, and the resulting test standard they have compiled is called JESD 201.

Pb Free Failure Concerns	Stress Test	Comments
Solder fatigue	Temp Cycle	Electrical open/solder crack
Overstressing	Shock Test	Electrical open/solder crack
Overstressing	Vib Test	Electrical open/solder crack
PCB trace, via corrosion	Temp/Humid 85/85°C	Electrical open due to via, trace corrosion
IMC growth, diffusion & solder creep	Bake Test	Electrical open IMC growth, diffusion & shorts due to solder creep

Figure 4. Pb free board level reliability concerns.

The challenges mentioned in the previous paragraph translate into board level reliability concerns (Figure 4). Because of their properties, lead-free solders are subject to a variety of problems that can occur during temperature cycling and shock, vibration testing, bake test, and HAST testing. Lead-free solders are stiff and can cause a fracture at the board solder interface. Lead-free solders are also prone to corrosion and intermetallic growth. This means that open circuit problems are the biggest concern. The application will determine the stress environment, so the lead-free solder joint reliability can be established by understanding the environment, knowing the failure mechanisms associated with that environment, performing accelerated testing to characterize those mechanisms, and extrapolating back to use conditions.

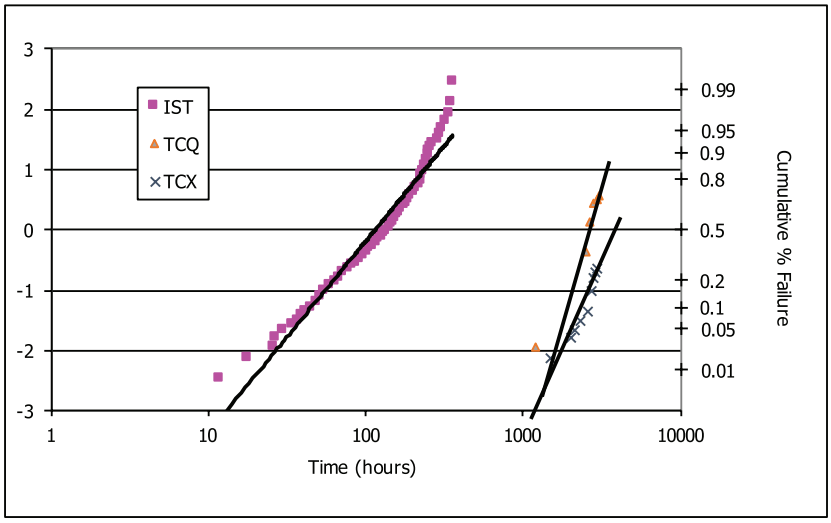


Figure 5. Immersion silver PCB via temperature cycling reliability.

The plot in Figure 5 shows an example of cycles to failure for solder joints processed with an immersion silver technology. Interconnect stress testing and temperature cycling can provide a quick method for determining the reliability. The quality of the plated through holes on the printed circuit board is important, and this test can provide data quickly to access any problems. One can also correlate the temperature cycling stress to factors such as moisture barriers.

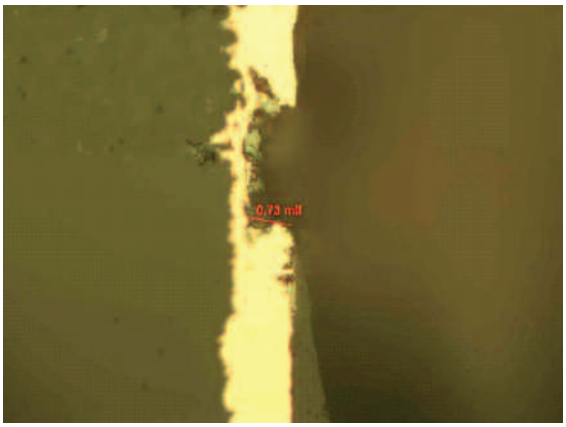
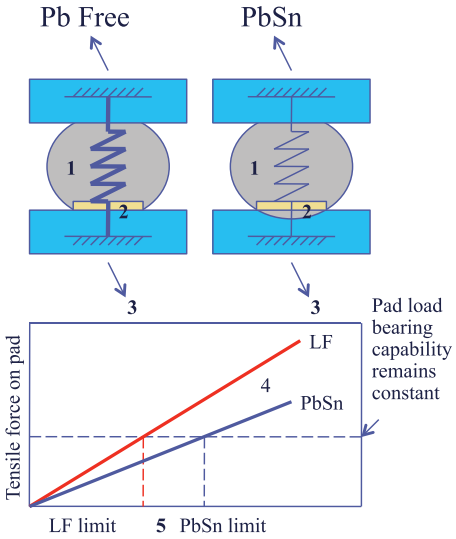


Figure 6. Optical image showing PCB via corrosion.

The image in Figure 6 shows an example of via thinning due to corrosion. This type of failure is caused by heat and humidity, and is accelerated by HAST testing. Notice that the corroded area is severely thinned, increasing the chance of an open circuit at this location.



1. Lead free is stiffer than PbSn
2. Pad adhesion strength is equivalent for Pb free and PbSn
3. Board bending pulls apart the opposite surfaces of the solder ball
4. Stiffer Pb-free ball generates higher forces on the pad. The softer PbSn ball deforms to accommodate bending, resulting in lower forces acting on the pad
5. Pb-free ball reaches the critical level of force required to pull the pad out at lower strain. This is a consequence of the ball material property, not the pad property

Figure 7. Concept behind transient bend stress—PbSn vs. Pb free solder joints.

Another technique for evaluating lead-free solder joints is the transient bend test (Figure 7). This test simulates the flexing a print circuit board might experience. For example, a cell phone might flex somewhat when one puts the phone in the pocket and then sits down. The bend in a printed circuit board will cause the solder balls near the corners of a package to experience a tensile force, which can result in open connections. In the transient bend test, tensile force is applied to the pad. As we noted earlier, lead-free solders are stiffer than leaded solders. However, the pad load capability remains the same, so the lead-free solder joint will fail sooner under the same tensile force. When a tensile force is applied, the PCB bending pulls on the opposite surfaces of the solder ball. The strain limit is reached more quickly in the lead-free solder ball and interface. The softer leaded solders are pliable, and result in lower forces for a given amount of strain.

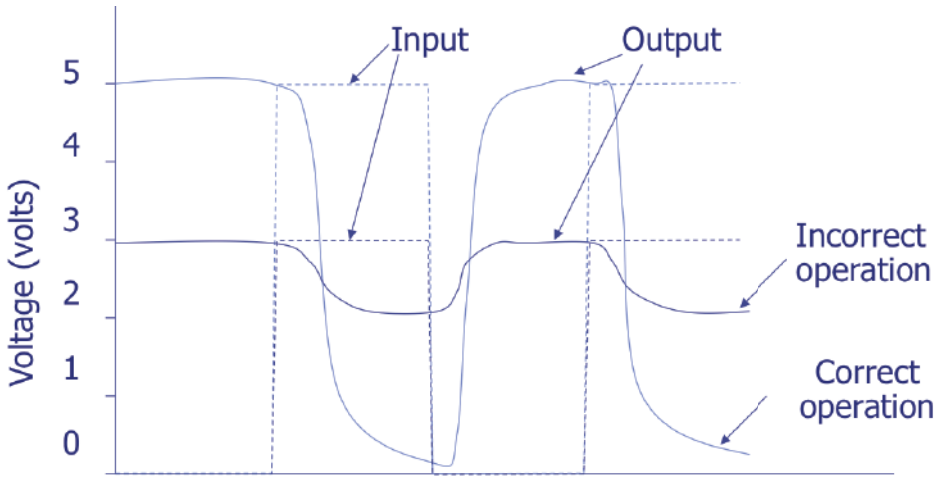
Technical Tidbit

Very Low Voltage (MinVDD) Testing

Testing to remove defects from ICs is an important, as well as challenging task. Sometimes we require novel methods to detect defects, as standard functional testing is inadequate. One such technique that can be effective is Very Low Voltage Testing.

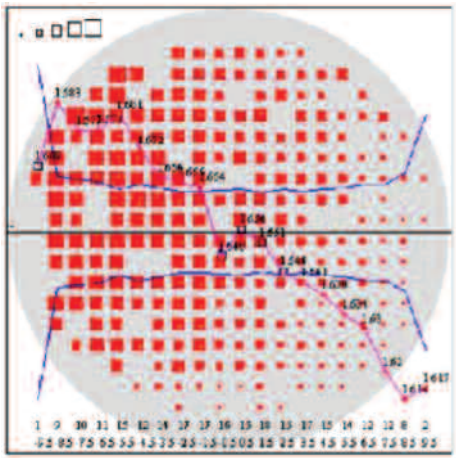
Very low voltage testing (VLV), or MinVDD testing as it is sometimes called, was developed by Ed McCluskey and Hong Hao at Stanford University. The idea behind VLV testing is that a chip that is degraded may not function correctly at lower voltage levels. While an IC with a subtle defect might work at its nominal operating voltage of 3.3 volts, it may not work correctly at 1.5 volts. An IC free of defects would work correctly at both voltages. This technique is potentially useful for catching problems related to defects on chips. It may not be as useful for problems related to process variations or design/manufacturing interactions, but this has not been explored in detail.

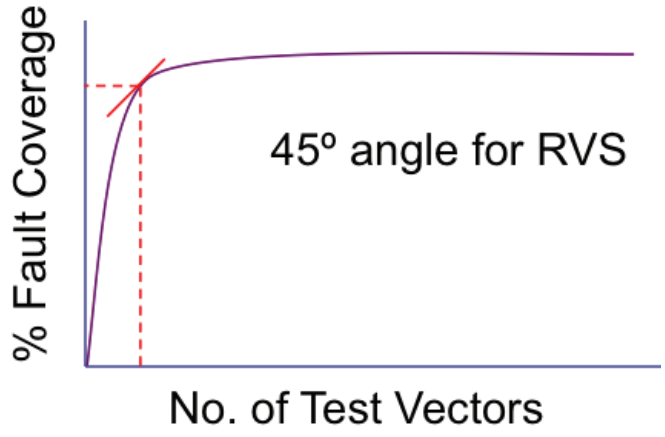
This graph helps illustrate the concept behind VLV testing. Let's assume there is a gate-to-source resistance in the upper n-channel transistor in a two input NAND gate. When the device is operated at 5 volts, as shown here, the output switches correctly with the input. When the device is operated at 3 volts, as shown here, the output does not switch correctly. Instead, the voltage remains at a level that would constitute a logical high value to the next input stage. If we assume that the gate-to-source resistance is attributable to an oxide defect, one can envision a situation where the oxide defect grows worse with time, lowering the gate-to-source resistance until it becomes a logical failure at the regular operating voltage.



NAND gate exhibiting a gate-source resistance in the upper n-channel transistor

McCluskey and Hao did an experiment to try and prove this hypothesis. They tested 148 ICs at 6 volts and 2 volts. All of the ICs passed functional and parametric testing; however, one failed at 2 volts. The majority of these ICs also failed IDDQ testing. The 148 ICs were then burned in at 125°C for one week. After this test, the one IC that failed at 2 volts also failed at 5 volts. McCluskey and his graduate students performed similar experiment several years later on 9 ICs that failed VLV testing. The 9 ICs were burned in at 125°C for one week and tested again. Two of the 9 failed just 6 hours into the burn-in. Based on the data, the test appears to find problems. The question is whether or not it is more effective than burn-in, and can it replace an expensive test like burn-in. If it did, it would be much more cost effective. A VLV test does not require chambers, and can be performed in a manner of seconds. While the test could certainly supplement burn-in, it is probably not a replacement for it.





A production implementation of MinVDD might look something like this. Because we don't have sufficient time during test to run full vector sets across the wafers to understand MinVDD at every die, what we do is we use Reduced Vector Sets (RVS) to collect and map MinVDD. MinVDD will vary across the wafer, so we want to collect the data and create a MinVDD map. We can then run a full vector set with a guard band on MinVDD and look for outliers using statistical post processing.

Ask the Experts

Q: What is OA?

A: Are you referring to OpenAccess (OA)? If so, this is an interoperability standard that designers and the EDA industry use to port data (layouts, netlists, etc.) between tools. Many of the EDA tool providers allow design information to be read or written using the OpenAccess standard. OpenAccess can also be addressed through scripting languages, which is the method most design engineers use when working with the standard. For more information on this subject, we would recommend you visit the Si2 website (www.si2.org). They are the group tasked with maintaining and promoting the standard.

Spotlight: IC Packaging (two courses)

IC Packaging Technology

OVERVIEW

Overview: Integrated Circuit packaging has always been integral to IC performance and functionality. An IC package serves many purposes: (1) pitch conversion between the fine features of the IC die and the system level interconnection, (2) chemical, environmental and mechanical protection, (3) heat transfer, (4) power, ground and signal distribution between the die and system, (5) handling robustness, and (6) die identification among many others. Numerous critical technologies have been developed to serve these functions, technologies that continue to advance with each new requirement for cost reduction, space savings, higher speed electrical performance, finer pitch, die surface fragility, new reliability requirements, and new applications. Packaging engineers must fully understand these technologies to design and fabricate future high-performance packages with high yields at exceptional low-costs to give their company a critical competitive advantage.

This two-day class will detail the vital technologies required to construct IC packages in a reliable, cost effective, and quick time to market fashion. When completed, the participant will understand the wide array of technologies available, how technologies interact, what choices must be made for a high-performance product vs. a consumer device, and how such choices impact the manufacturability, functionality, and reliability of the finished product. An emphasis will be given to manufacturing, processes and materials selection tailoring and development. Each fundamental package family will be discussed, including flip chip area array technologies, Wafer Level Packaging (WLP), Fan-Out Wafer Level Packaging (FO-WLP), and the latest Through Silicon Via (TSV) developments. Additionally, future directions for each package technology will be highlighted, along with challenges that must be surmounted to succeed.

WHAT WILL I LEARN BY TAKING THIS CLASS?

1. **Molded Package Technologies.** Participants learn the fundamentals of molding critical to leaded, leadless, and area array packaging, enabling them to eliminate problems such as flash, incomplete fill, and wire sweep.
2. **Flip Chip Technologies.** Participants learn the fundamentals of plating, bumping, reflow, underfill, and substrate technologies that are required for both high performance and portable products.
3. **Wafer Level Packages.** Participants learn the newest technologies that enable the increasingly popular Wafer Chip Scale Level Packages (WCSPs) and Fan-Out Wafer Level Packages (FO-WLPs).
4. **Through Silicon Via Packages and Future Directions.** Participants will know the latest advances in the recently productized TSV technology, as well as future directions that will lead to the products of tomorrow.

COURSE OBJECTIVES

1. The course will supply participants with an in-depth understanding of package technologies current and future.
2. Potential defects associated with each package technology will be highlighted to enable the student to identify and eliminate such issues in product from both internal assembly and OSAT houses.
3. Cu and solder plating technologies will be described with special emphasis on package applications in TSVs and Cu pillars for FO-WLPs. Emphasis will be placed on eliminating issues such as reliability, non-uniformity, void free thermal aging performance, and contamination free interfaces.
4. New package processes employed in Through Silicon Via production will be described, along with current cost reduction thrusts, to enable the student to understand the advantages and limits of the technologies.
5. Temporary bonding and wafer thinning processes will be highlighted, as well as the cost reduction approaches currently being pursued to enable wider adoption of TSV packages.
6. The trade-offs between silicon, glass, and organic interposers will be highlighted, along with the processes used for each.
7. Participants will gain an understanding of the surface mount technologies that enable today's fine pitch products.
8. The class will provide detailed references for participants to study and further deepen their understanding.

COURSE OUTLINE

1. The Package Development Process as a Package Technology:
   a. Materials and Process Co-Design
2. Molded Package Technologies:
   a. Die Attach
      i. Plasma Cleans
   b. Wire Bonding
      i. Au vs. Cu vs. Ag
      ii. Die Design for Wire Bonding
   c. Lead Frames
   d. Transfer and Liquid Molding
      i. Flash
      ii. Incomplete Fill
      iii. Wire Sweep
      iv. Green Materials
   e. Pre- vs. Post-Mold Plating
   f. Trim Form
   g. Saw Singulation
   h. High Temperature and High Voltage Materials

3. Flip Chip and Ball Grid Array Technologies:
   a. Wafer Bumping Processing
      i. Cu and Solder Plating
      ii. Cu Pillar Processing
   b. Die Design for Wafer Bumping
   c. Flip Chip Joining
   d. Underfills
   e. Substrate Technologies
      i. Surface Finish Trade-Offs
      ii. Core, Build-up, and Coreless
   f. Thermal Interface Materials (TIMs) and Lids
   g. Fine Pitch Warpage Reduction
   h. Stacked Die and Stacked Packages
   i. Material Selection for Board Level Temperature Cycling and Drop Reliability
4. Wafer Chip Scale Packages:
   a. Redistribution Layer Processing
   b. Packing and Handling
   c. Underfill vs. No-Underfill
5. Fan-Out Wafer Level Packages:
   a. Chip First vs. Chip Last Technologies
   b. Redistribution Layer Processing
   c. Through Mold Vias
6. Through Silicon Via Technologies:
   a. Current Examples
   b. Fundamental TSV Process Steps
      i. TSV Etching
      ii. Cu Deep Via Plating
      iii. Temporary Carrier Attach
      iv. Wafer Thinning
   c. Die Stacking and Reflow
   d. Underfills
   e. Interposer Technologies: Silicon, Glass, Organic
7. Surface Mount Technologies:
   a. PCB Types
   b. Solder Pastes
   c. Solder Stencils
   d. Solder Reflow

IC Packaging Design and Modeling

OVERVIEW

IC packaging complexity levels are rising year-by-year in lock step with process advances and electrical performance enhancements. Single die packages with leads have given way to multi-chip area array packages, stacked die packages, and stacked packages. Pin-counts have increased from a few handfuls to thousands. Space constraints for consumer products have required shrinking some packages to barely larger than the chip volume, and high-performance applications have required ever increasing levels of power dissipation and higher frequency operation. Pin count increases alone driven by wide I/O have driven substrate technologies to include upwards of 20 or 30 interconnect layers. Higher integration levels in automotive applications have motivated higher reliability requirements. At the same time, time-to-market and cost reduction requirements have forced an ever-accelerating product development pace where missing a product launch can spell a company's doom. Trial and error iteration won't work in today's industry.

The only way to meet the interrelated demands of complexity, performance, time-to-market, and reliability is through appropriate package design processes and modeling. This two-day class will cover fundamental issues in package design, including the need for appropriate risk analysis, up-front design rules, early look-ahead, and modeling coupled with verification. Participants will learn the fundamentals of thermal and electrical analysis for performance characterization. Compact models that enable transferring phenomenological behavior between die, package, and system level models will be described. Mechanical analysis examples applied to a wide range of reliability issues will be emphasized with a focus on solving issues in advance. Participants will learn the critical factors that must be implemented to ensure the success of their package designs and products.

WHAT WILL I LEARN BY TAKING THIS CLASS?

Participants will learn critical skills required to design a fully functioning IC package that meets competing requirements. This skill-building series is divided into four segments:

1. **Packaging Design Overview.** Participants learn the fundamentals of packaging design. They learn why modeling has become critical to today's semiconductor packaging and how important co-design from the chip level through the system level is to product performance.
2. **Mechanical Simulations.** Participants learn the fundamentals of displacement, strain, stress, and energy and how to interpret the stresses that can be calculated. They learn how to apply fracture mechanics to a problem.
3. **Thermal Simulations.** Participants learn heat transfer modeling. They also learn about steady-state and transient thermal modeling. Reasons for and the topology of industry standard and compact thermal models will be described.
4. **Modeling Semiconductor Packages.** Participants learn about the software used for modeling a variety of aspects of semiconductor packaging. They see many examples of current modeling tools used by package design experts.

COURSE OBJECTIVES

1. Application spaces for each package family will be covered, including the primary constraints and care-abouts for the product spaces.
2. A thorough listing of interrelated factors will be detailed to enable participants to understand what factors throughout the entire package design chain must be considered when making modifications to one or more package constituents.
3. Mechanical modeling will be highlighted as a tool to be used to develop a parametric understanding stress impacts. For example, if an underfill modulus is changed, what happens to the stresses on the circuits under the bumps, on the die interface, in the underfill etc.
4. Participants will know the types of stress analyses that should be performed for each package question, as well as the inputs and verification that is required to ensure the model is producing real answers, not just numbers.
5. Thermal and electrical modeling techniques needed to verify a package's performance well before tooling is committed will be described
6. Participants will learn from real examples how best to utilize package design tools and will learn their strengths and weaknesses.
7. Participants will see examples of package design rules that, when incorporated in design manuals, enable robust reliable package design. Participants will learn how to develop package design rules for their own products.
8. Knowledge gained from the class will improve time-to-market for participants by helping them avoid costly qualification failures.

COURSE OUTLINE

1. Assembly & Packaging Processes:
   a. Material Selection
   b. Typical Assembly Process Flows
   c. Package Types & Evolution
   d. Simulation Tools & Applications
   e. Risk Evaluation & Risk Mitigation
2. Design for Manufacturability (DfM):
   a. Solid Mechanics
   b. Assembly-Induced Stress
   c. Package Warpage & Coplanarity
   d. Die Bonding, Wire Bonding, & Microbump Bonding
   e. Mold Flow Modeling and Correlations

3. Design for Reliability (DfR):
   a. Chip-to-Package Interaction (CPI)
   b. Interfacial Delamination & Adhesion
   c. Solder Joint Reliability (SJR)
4. Design for Performance:
   a. Heat Transfer
   b. Package Thermal Resistance
   c. Steady State & Transient Thermal Behavior
   d. Power Distribution and Noise
   e. Compact Models
   f. Drop Testing & Simulation
5. Advanced Packaging Examples:
   a. Multichip Packages
   b. Stacked Packages
   c. Wafer Level Packaging
   d. 3D Packaging
   e. Through Silicon Via (TSV) Interconnects

International Symposium for Testing and Failure Analysis

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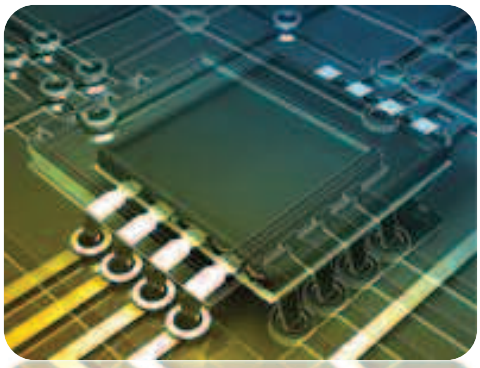
Semitracks is planning to demonstrate our Online Training Software for Failure Analysis at ISTFA.
For more information,
please contact us at info@semitracks.com



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Upcoming Courses

(Click on each item for details)

Failure and Yield Analysis
September 11 – 14, 2017 (Mon – Thur)
San Jose, California, USA

Semiconductor Reliability / Product Qualification
September 18 – 21, 2017 (Mon – Thur)
Portland, Oregon, USA

IC Packaging Design and Modeling
September 25 – 26, 2017 (Mon – Tue)
Dallas, Texas, USA

IC Packaging Technology
September 27 – 28, 2017 (Wed – Thur)
Dallas, Texas, USA

Failure and Yield Analysis
April 9 – 12, 2018 (Mon – Thur)
Munich, Germany

Wafer Fab Processing
April 9 – 12, 2018 (Mon – Thur)
Munich, Germany

Semiconductor Reliability / Product Qualification
April 16 – 19, 2018 (Mon – Thur)
Munich, Germany