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InfoTracks

Semitracks Monthly Newsletter

Time Domain Reflectometry Part II

By Christopher Henderson

Last issue, we began our discussion on time domain reflectometry, or TDR. To recap a little, in order to calculate the distance to the defect, the engineer captures the signal and establishes a time difference. He or she must relate that time difference back into a distance to establish where the open or change in resistance might be. The distance to the defect in millimeters can be calculated by

$$D = \frac{c \cdot \Delta t}{2 \times 10^{9} \cdot \varepsilon}$$

where c is the speed of light in meters per second, Δt is the estimated time difference calculated from the waveforms, and ε is the dielectric constant of the material. Different materials have different dielectric constants, so one needs to take this variable into account. Last month we provided a table of example materials and their dielectric constants. As an example calculation, a Δt of 50 psec gives a distance to the open of 3.71mm in a fiberglass substrate.

The key challenge with this technology is interpretation and integration with the design files. Waveforms can be quite difficult to interpret, necessitating comparisons between good devices and failing devices. The locations shown in this diagram are the locations where waveforms are measured in the next illustration. They are la-

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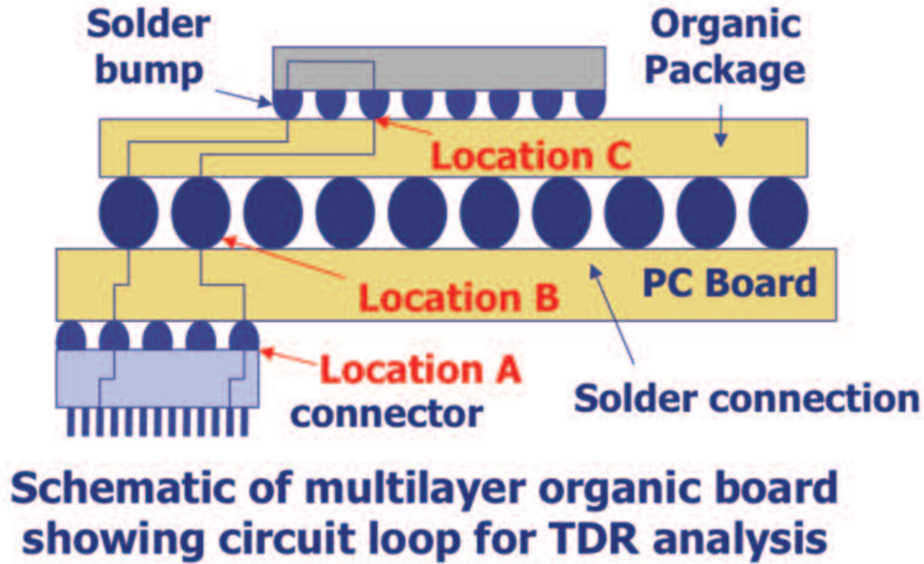
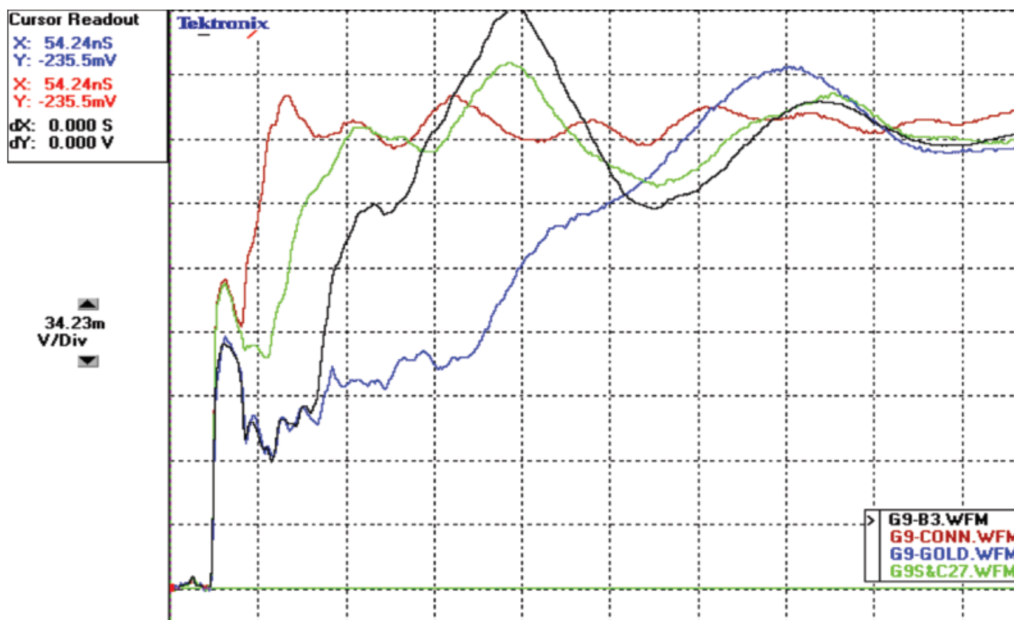
beled Location A, B, and C. The times associated with those locations should be based on the distances through the vias and traces.

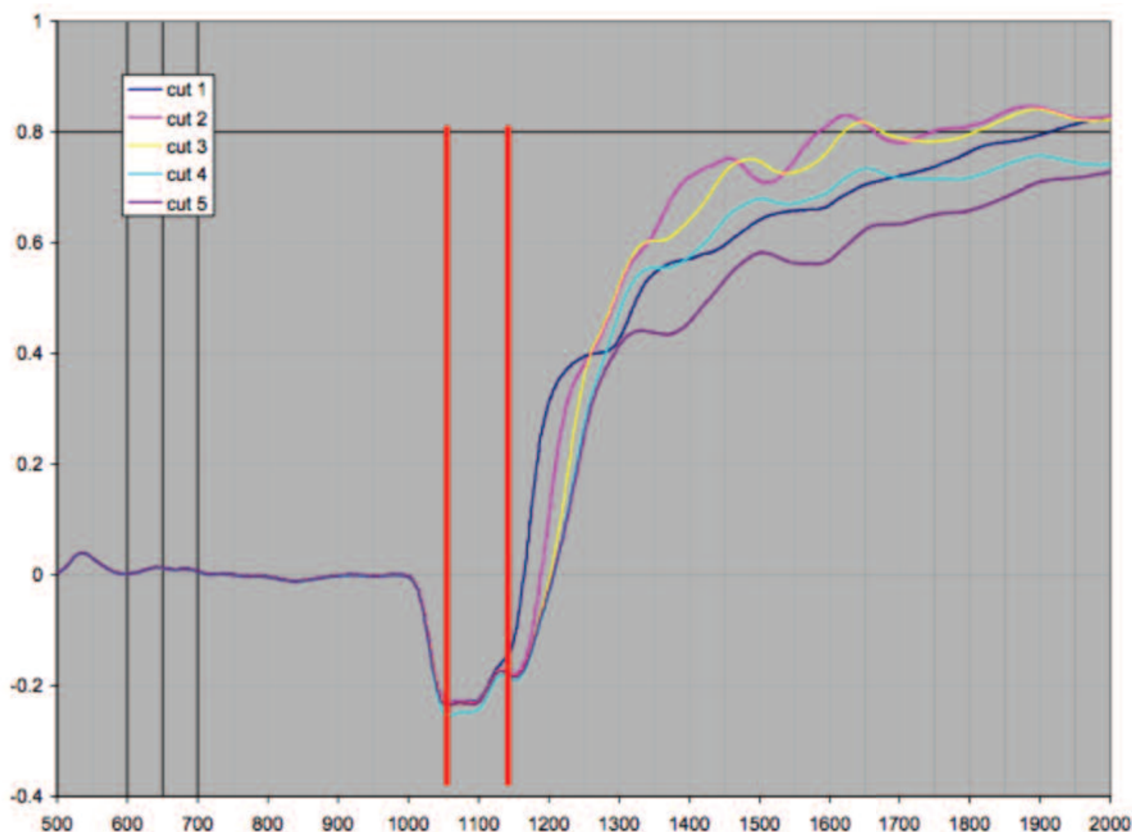


Schematic of multilayer organic board showing circuit loop for TDR analysis

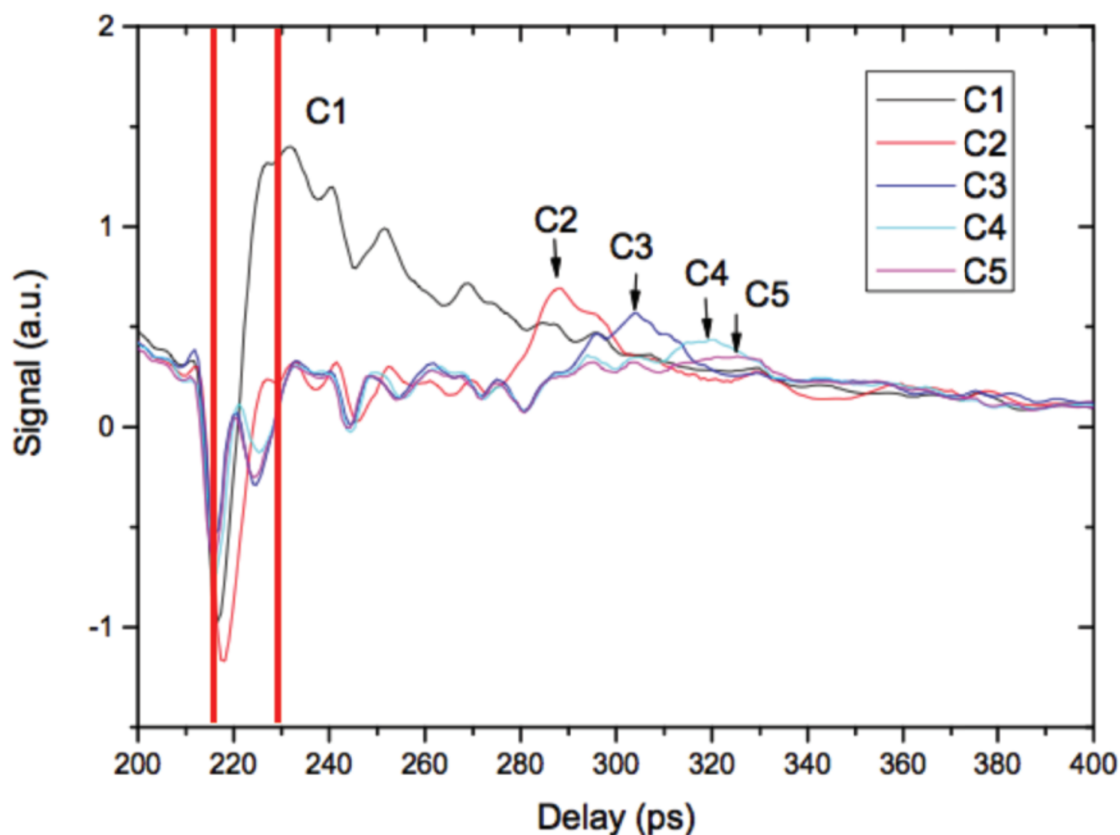
The challenge with TDR is interpreting the waveforms. There can be numerous reflections at material bends and interfaces, which add complexity to the waveforms. In this graph, the red waveform is from the unterminated cable of the time domain reflectometer. The green waveform is from the cable connected to the printed circuit board, the black is from a unit with electrical opens and the blue is from a good unit. The waveform rises more slowly in the good unit indicating that more of the signal is transmitted further into the package before being reflected. The sharp rise in the black waveform indicates a strong reflection, or change in material interface closer to the package edge. Notice that although there is a significant difference between the good unit and the unit with the electrical opens, the point where one should indicate the rise is not clear.



Another issue with interpreting TDR waveforms is that it can be difficult to identify small differences. In these waveforms, we are looking at differences. It is clear that the reflection waveforms from Cut 1 and Cut 2 are separable but the rising edges from the reflections of Cut 3 to Cut 5 are superimposed onto one another, which do not provide useful information about the locations of failures. This can make interpretation a challenge when the distance to the open is small.



One method for better resolving the data in a TDR waveform is to use electro-optical TDR. Electro-optical TDR uses electro-optics and a photoconductive switch to generate the pulse. With conventional TDR the highest frequencies run at approximately 50GHz. This yields about a 250-micron resolution. With electro-optical TDR, the bandwidth can be as high as 2THz, which yields approximately 10 microns resolution. Here we show the same data from the cuts on the previous slide, but this time we use electro-optical TDR to create the waveforms. In this case, the waveforms can more easily be resolved.



To summarize, TDR is becoming more common in the analysis of packaging problems. The ability to gather data non-destructively that can aid in isolating the failure in a complex package is important. Interpretation can be a challenge though. Package complexity leads to reflected signals at vias, bends, and materials interfaces. Because of the frequencies of the signals, the spatial resolution for TDR is somewhat limited as well. With standard TDR, the spatial resolution is around 250 microns. Electro-optical TDR is a newer form of TDR that does improve on the original technique. The higher frequencies allow for spatial resolution down to 10 microns, and improved ability to interpret the data. Expect to see more use of electro-optical TDR in the future.

Ask the Experts

Q: I am trying to determine the percentage of chromium in a SiCr fusible link resistor using Energy Dispersive X-Ray Spectroscopy, but I am seeing a very low percentage (1-2%). How much chromium should be in the SiCr resistor?

A: A: The typical number is between 15 and 35%. The reason you are seeing such a low percentage is probably due to the fact that the SiCr resistor is very thin, and the interaction volume of the SEM is penetrating well beyond the material, causing you to see more of the silicon in the SiO2 and substrate. The resistor film is usually around 10nm thick, which means the vast major of the beam penetrates beyond the resistor.

Technical Tidbit

Al-Si metallization systems

Some companies use different percentages of silicon in their aluminum-silicon (Al-Si) metallization systems. This phase diagram helps to illustrate why one might choose different percentages.

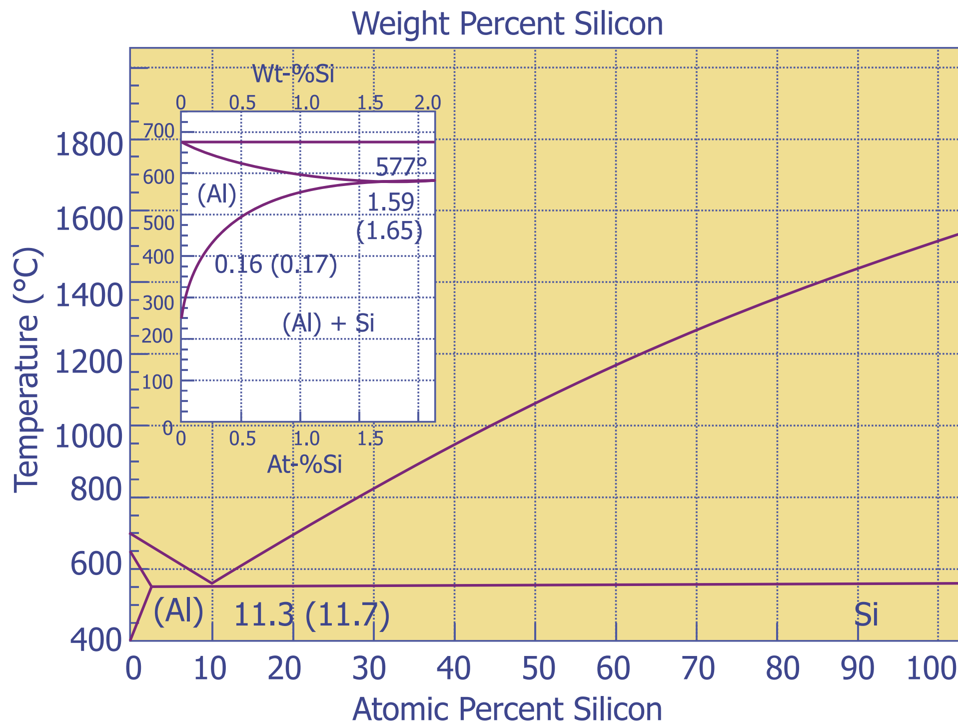


Figure 1. Al-Si Phase Diagram.

If we look at the phase diagram, we see 100% Al on the left and 100% Si on the right. The melting temperature for Al is 660°C, the melting temperature for Si is 1414°C, and the eutectic temperature (at 11.3% Si) is 577°C. We are interested in how much Si we can incorporate into the Al in solid solution – the region at the lower left. We have expanded that region in the white inset graph. Notice that at Al-0.5%Si, the solid solution temperature can be as low as 500°C whereas with Al-1%Si, the solid solution temperature can only be as low as 550°C. This means that if we want Al-1%Si, we'll need to do the deposition at 550°C or higher, whereas with Al-0.5%Si, we can do the deposition as low as 500°C. A lower deposition temperature can be beneficial from a thermal budget standpoint, creating less damage. On the other hand, a higher percentage of Si in the Al will better prevent Si nodules. This is the basic tradeoff process engineers face with Al-Si metal systems.

Spotlight: Failure and Yield Analysis

OVERVIEW

Failure and Yield Analysis is an increasingly difficult and complex process. Today, engineers are required to locate defects on complex integrated circuits. In many ways, this is akin to locating a needle in a haystack, where the needles get smaller and the haystack gets bigger every year. Engineers are required to understand a variety of disciplines in order to effectively perform failure analysis. This requires knowledge of subjects like: design, testing, technology, processing, materials science, chemistry, and even optics! Failed devices and low yields can lead to customer returns and idle manufacturing lines that can cost a company millions of dollars a day. Your industry needs competent analysts to help solve these problems. ***Advanced Failure and Yield Analysis*** is a four-day course that offers detailed instruction on a variety of effective tools, as well as the overall process flow for locating and characterizing the defect responsible for the failure. This course is designed for every manager, engineer, and technician working in the semiconductor field, using semiconductor components or supplying tools to the industry.

By focusing on a ***Do It Right the First Time*** approach to the analysis, participants will learn the appropriate methodology to successfully locate defects, characterize them, and determine the root cause of failure.

Participants learn to develop the skills to determine what tools and techniques should be applied, and when they should be applied. This skill-building series is divided into three segments:

1. **The Process of Failure and Yield Analysis.**Participants learn to recognize correct philosophical principles that lead to a successful analysis. This includes concepts like destructive vs. non-destructive techniques, fast techniques vs. brute force techniques, and correct verification.
2. **The Tools and Techniques.** Participants learn the strengths and weaknesses of a variety of tools used for analysis, including electrical testing techniques, package analysis tools, light emission, electron beam tools, optical beam tools, decapping and sample preparation, and surface science tools.
3. **Case Histories.** Participants identify how to use their knowledge through the case histories. They learn to identify key pieces of information that allow them to determine the possible cause of failure and how to proceed.

COURSE OBJECTIVES

1. The seminar will provide participants with an in-depth understanding of the tools, techniques and processes used in failure and yield analysis.
2. Participants will be able to determine how to proceed with a submitted request for analysis, ensuring that the analysis is done with the greatest probability of success.
3. The seminar will identify the advantages and disadvantages of a wide variety of tools and techniques that are used for failure and yield analysis.
4. The seminar offers a wide variety of video demonstrations of analysis techniques, so the analyst can get an understanding of the types of results they might expect to see with their equipment.
5. Participants will be able to identify basic technology features on semiconductor devices.
6. Participants will be able to identify a variety of different failure mechanisms and how they manifest themselves.
7. Participants will be able to identify appropriate tools to purchase when starting or expanding a laboratory.

INSTRUCTIONAL STRATEGY

By using a combination of instruction by lecture, video, and question/answer sessions, participants will learn practical approaches to the failure analysis process. From the very first moments of the seminar until the last sentence of the training, the driving instructional factor is **application.** We use instructors who are internationally recognized experts in their fields that have years of experience (both current and relevant) in this field. The handbook offers hundreds of pages of additional reference material the participants can use back at their daily activities.

THE SEMITRACKS ANALYSIS INSTRUCTIONAL VIDEOS™

One unique feature of this workshop is the video segments used to help train the students. Failure and Yield Analysis is a visual discipline. The ability to identify nuances and subtleties in images is critical to locating and understanding the defect. Many tools output video images that must be interpreted by analysts. No other course of this type uses this medium to help train the participants. These videos allow the analysts to directly compare material they learn in this course with real analysis work they do in their daily activities.

COURSE OUTLINE

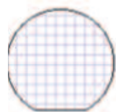
1. Introduction
2. Failure Analysis Principles/Procedures
    a. Philosophy of Failure Analysis
    b. Flowcharts
3. Gathering Information
4. Package Level Testing
    a. Optical Microscopy
    b. Acoustic Microscopy
    c. X-Ray Radiography
    d. Hermetic Seal Testing
    e. Residual Gas Analysis
5. Electrical Testing
    a. Basics of Circuit Operation
    b. Curve Tracer/Parameter Analyzer Operation
    c. Quiescent Power Supply Current
    d. Parametric Tests (Input Leakage, Output voltage levels, Output current levels, etc.)
    e. Timing Tests (Propagation Delay, Rise/Fall Times, etc.)
    f. Automatic Test Equipment
    g. Basics of Digital Circuit Troubleshooting
    h. Basics of Analog Circuit Troubleshooting

6. Decapsulation/Backside Sample Preparation
    a. Mechanical Delidding Techniques
    b. Chemical Delidding Techniques
    c. Backside Sample Preparation Techniques
7. Die Inspection
    a. Optical Microscopy
    b. Scanning Electron Microscopy
8. Photon Emission Microscopy
    a. Mechanisms for Photon Emission
    b. Instrumentation
    c. Frontside
    d. Backside
    e. Interpretation
9. Electron Beam Tools
    a. Voltage Contrast
        i. Passive Voltage Contrast
        ii. Static Voltage Contrast
        iii. Capacitive Coupled Voltage Contrast
        iv. Introduction to Electron Beam Probing
    b. Electron Beam Induced Current
    c. Resistive Contrast Imaging
    d. Charge-Induced Voltage Alteration
10. Optical Beam Tools
    a. Optical Beam Induced Current
    b. Light-Induced Voltage Alteration
    c. Thermally-Induced Voltage Alteration
    d. Seebeck Effect Imaging
    e. Electro-optical Probing
11. Thermal Detection Techniques
    a. Infrared Thermal Imaging
    b. Liquid Crystal Hot Spot Detection
    c. Fluorescent Microthermal Imaging
12. Chemical Unlayering
    a. Wet Chemical Etching
    b. Reactive Ion Etching
    c. Parallel Polishing

13. Analytical Techniques
    a. TEM
    b. SIMS
    c. Auger
    d. ESCA/XPS
14. Focused Ion Beam Technology
    a. Physics of Operation
    b. Instrumentation
    c. Examples
    d. Gas-Assisted Etching
    e. Insulator Deposition
    f. Electrical Circuit Effects
15. Case Histories

You may want to stress some aspects more than others or conduct a simple one-day overview course. Many of our clients seek ongoing just-in-time training that builds in-depth, advanced levels of reliability expertise. We'll work with you to determine the best course of action and create a statement of work that emulates the very best practices of semiconductor reliability analysis.

Our instructors are active in the field and they practice the disciplines daily. Please give us a call (505) 858-0454 or drop us an e-mail (info@semitracks.com).



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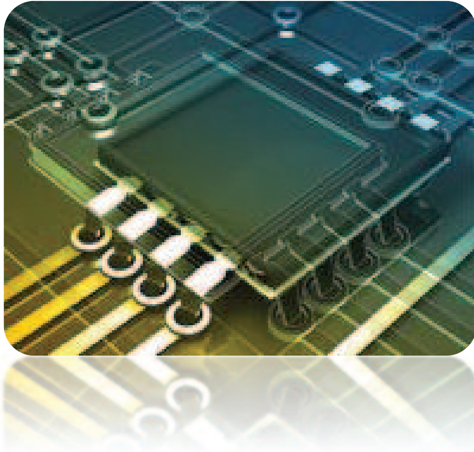

Upcoming Courses

(Click on each item for details)

Semiconductor Reliability
September 3 – 5, 2014 (Wed – Fri)
San Jose, California, USA

Failure and Yield Analysis
September 8 – 11, 2014 (Mon – Thur)
San Jose, California, USA

Product Qualification
January 26 – 27, 2015 (Mon – Tue)
San Jose, California, USA

Wafer Fab Processing
January 26 – 29, 2015 (Mon – Thur)
San Jose, California, USA

EOS, ESD and How to Differentiate
January 28 – 29, 2015 (Wed – Thur)
San Jose, California, USA

Feedback

If you have a suggestion or a comment regarding our courses, online training, discussion forums, or reference materials, or if you wish to suggest a new course or location, please call us at 1-505-858-0454 or Email us (info@semitracks.com).

To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered in the next newsletter, please contact Jeremy Henderson by Email (jeremy.henderson@semitracks.com).

We are always looking for ways to enhance our courses and educational materials.

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http://www.semitracks.com

To post, read, or answer a question, visit our forums.
We look forward to hearing from you!