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YOUR MONTHLY LOOK INSIDE SEMICONDUCTOR TECHNOLOGY

Semiconductor Cleanroom Technology

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In this month's Feature Article, we will continue our discussion of Cleanroom Technology. This article discusses cleanroom access. Semiconductor cleanrooms must remain free of contamination and particles, how control over how to enter and exit the cleanroom is critical.

To begin, let's address a fundamental question – why do we limit access to the cleanroom? Generally, it is all about contamination control. There are two main reasons. First, fewer entry and exit points mean fewer opportunities for particles to enter the cleanroom. Second, fewer people in the cleanroom means fewer opportunities for particles to enter the cleanroom.

A vestibule is typically the main access point to the actual cleanroom. In order to seal the room for cleanliness, and also allow access to personnel, vestibules are constructed with two or more doors and only one door is allowed to be opened at a time. A simple two-door airlock will have electric locks on each door which are normally unlocked. Opening either door will cause the other door to lock, preventing air and airborne particulates from entering or exiting the airlock. The door hardware must cause the doors to close immediately after an entry or exit.

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- Advanced CMOS/FinFET Fabrication

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These airlocks use door status switches to sense when a door has been opened, and a door interlock controller then activates the locking mechanism of the unopened door. In some situations, local building codes may require special lock override controls to enable personnel to escape the area in an emergency. Since only one door can be accessed at a time by design, the system must be tied into the fire alarm system to unlock the doors in case of fire. An emergency override switch should be located within the room and at each doorway into the room. These devices can operate the door lock directly as well as signal the door interlock controller. Some facilities use an emergency pull station or a latching push-pull switch with a key reset to override the system and unlock the necessary doors. These devices frequently incorporate a built-in sounder to alert area personnel that the doors are unlocked for uninhibited ingress or egress. Sometimes there are multiple entrances to a cleanroom creating complex traffic patterns. These can easily be accommodated using a PLC-based controller. These can involve dozens of doors and some doors may be used to pass between two sterile rooms. This situation requires that all doors in each of the two rooms be secured whenever the "shared" door between them is open. The shared door may be normally unlocked for faster traffic flow if the other doors in the two rooms are normally locked.

Airlocks help maintain air pressurization differentials and directional air flow between adjacent areas when personnel or equipment pass between them. Airlocks provide critical separation barriers in pharmaceutical and biopharmaceutical plants. In addition to separating areas of different environmental air cleanliness classifications, they also divide containment and non-containment areas, and may also operate as equipment "pass-thru" and gowning/de-gowning areas. Figure 1 shows an example of an airlock system for a semiconductor cleanroom. There are four types of airlocks, each suited to a particular type of application: the "cascading pressure airlock", the "pressure bubble airlock", the "pressure sink airlock" and the "potent compound airlock". The "cascading pressure airlock" is the airlock type preferred by the US Government when containment is not an issue. It is used to separate clean areas from more general work areas. In this configuration, pressurized air "cascades" from the cleanest to the less clean adjacent areas. In this application, the same quantity of air is supplied to and returned from the airlock. In contrast, the "pressure bubble airlock" and the "pressure sink airlock" are used to separate contained clean areas from non-contained (either clean or non-clean) areas. In the "pressure bubble airlock", conditioned air from a clean, non-contained source is used to pressurize the airlock. The supply air then dissipates into adjacent areas through the airlock doors, walls and other openings, preventing cross-contamination between adjacent rooms, and contamination from adjacent areas from entering the airlock. In the "pressure sink airlock", negative pressure is maintained relative to all adjacent areas, and all the air supplied to and infiltrated into the room is exhausted, also preventing cross-contamination between adjacent areas. Of these two methods, the pressure bubble airlock is the most commonly used because all particles or dirt are kept out of the airlock at all times, while in the pressure sink airlock, particles and dirt from all adjacent rooms opening into the airlock are continuously passing into the airlock through door, wall or ceiling cracks. The "potent compound airlock" is a combination of the pressure bubble and pressure sink airlocks. This two-compartment airlock arrangement allows personnel to protect themselves before coming into contact with any dangerous materials,while at the same time, the semiconductor product, also known as the potent compound, is protected from contamination from adjacent, connected areas. All conditioned, clean air supplied to the gown room is dissipated into the adjacent rooms while all the conditioned, clean air supplied to the airlock room (as well as all infiltration air into that room) is exhausted.

Figure 1- Example of an airlock system for a semiconductor cleanroom (image courtesy Terra Universal)

One process that helps to further prevent particles from entering the cleanroom is the air shower. Streams of compressed air blow across the body suit as personnel enter the fab, helping to dislodge any particles that might be adhered to the body suit. Figure 2 shows an example of the air shower.

Figure 2- Example of an air shower (image courtesy Angstrom Technology)

To determine the pressure differential required between adjacent rooms of different cleanliness level, both US and European Community (EC) manufacturing practices must be examined. However, because the US Aseptic Processing Guide requires a static pressure differential of 0.05 inches in a water gauge pressure measurement system, for both "controlled" and "critical" areas, and the EC Guide gives a range of 10 to 15 pascals, or 0.04 to 0.06 inches of water, a differential of 0.05 inches will satisfy both manufacturing practices. It is also necessary to determine where to apply the pressure differential, because this will vary depending on the airlock type. For example, in cascading pressure airlocks, the differential should be between the cleanroom and the corridor, whereas in both pressure bubble and pressure sink airlocks, it should be between the airlock and the corridor, and between the airlock and the contained area. Containment must also be considered for these two airlocks, and the containment area should always be negative to any adjacent non-contained areas. This will ensure that in the event that both airlock doors are mistakenly opened simultaneously, any airflow will be from the non-contained area (the corridor) to the contained area. Although the contained area is at a cleaner classification level than the corridor, it is also at a lower pressure. In a pressure sink airlock, there is a lower pressure inside the airlock and a higher pressure on both sides of the airlock. This is typically used where contaminated air must remain in one location, but it is not commonly used in the semiconductor industry. In a potent compound airlock, both pressure bubble and pressure sink airlock principles apply. This two-compartment airlock arrangement allows personnel to gown themselves before coming into contact with any dangerous materials, while the product, or potent compound, is protected from contamination from adjacent connected areas. If the three doors of a potent-compound airlock are inadvertently left open, the airflow will still be from the non-contained area (the corridor) to the contained area, preventing the release of hazardous gasses.

In next month's Feature Article, we will continue our discussion of cleanroom access. More specifically, we will cover personnel access and gowning procedures.

Technical Tidbit:Complimentary Field Effect Transistors (CFETs)

In this month's Technical Tidbit, we will discuss Complementary Field Effect Transistors (CFETs). CFETs represent a potential solution to allow designers to continue to create more complex integrated circuits.

In order to increase the density of transistors on an integrated circuit, the semiconductor industry initially scaled the lateral size of the transistors to smaller and smaller dimensions. By the 32nm technology node, the industry had pretty much used every single processing method known to achieve lateral scaling while maintaining reasonable power consumption and reliability. With the introduction of the FinFET at the 22nm technology node, engineers began using the vertical dimension to continue scaling transistors. The FinFET worked well down to the 7nm technology node, but then it began to suffer from insufficient performance to continue scaling. In response, engineers introduced the Gate All Around (GAA) or nanosheet transistor at the 5nm technology node. However, this change is only helpful for a limited amount of additional scaling. The biggest problem is that the p- and n-channel transistors still sit side-by-side. This creates a number of difficulties when optimizing the design and technology elements. Today's processes are so complex and interconnected with the design, that the design and technology need to be optimized together, a process known as Design Technology Co-Optimization, or DTCO. When the p- and n-channel transistors sit side-by-side, there must be sufficient spacing to prevent cross-talk, leakage, and reliability problems. Therefore, at the 2nm technology node, additional changes will be needed. The main change being contemplated is stacking the p- and n-channel on top of one another, creating an architecture known as a Complementary Field Effect Transistor (CFET) architecture. Figure 1 shows a 3D model of a notional CFET architecture (on the left), and a Transmission Electron Microscope (TEM) cross section image of an early-stage development process of a CFET architecture (on the right).

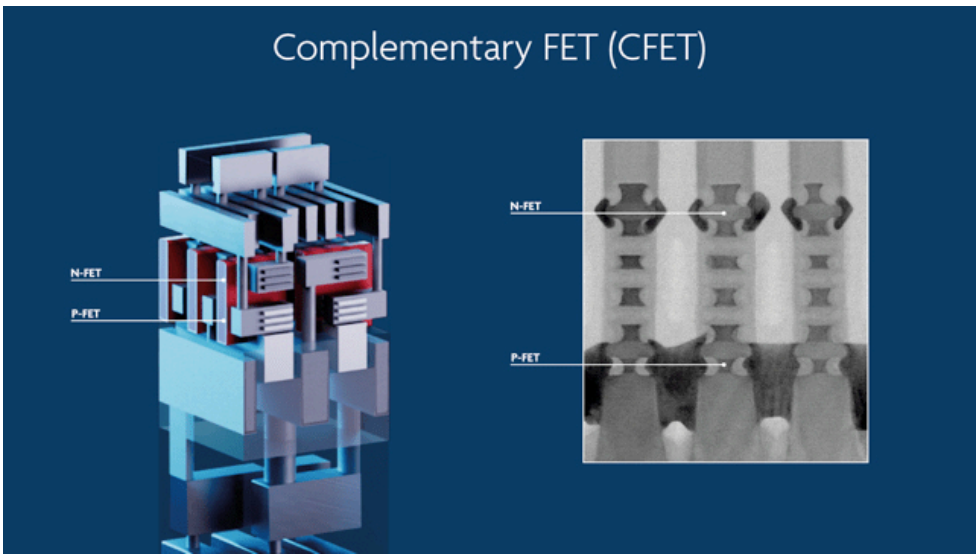

Figure 1- 3D Model (left) and TEM cross-section (right) of a CFET architecture (images courtesy imec)

In the CFET architecture, the n-channel FETs sit above the p-channel FETs. This means that engineers no longer need to worry about the lateral separation between the two transistors, since they now overlap one another vertically. The p-channel FETs are likely to stay on the bottom, where one can use the silicon substrate to provide stress for the p-channel transistor to improve the mobility of the carriers in the transistor. Signal routing is also simplified with this process, since the channels of the two types of transistors sit in a single vertical structure.

There are two potential options for fabricating CFETs. The first option is to do the processing of the two transistor types on a single wafer. This has the advantage of reducing the number of steps in the overall chip fabrication process, but it may not lead to a well-optimized process for high performance designs. Furthermore, the complexity of the individual processing steps will be extremely challenging. Sacrificial structures and Atomic Layer Deposition will be needed for a large number of processing steps. The second option is to do the processing of the two transistor types on separate wafers. This may reduce the complexity of some of the individual processing steps. It may also allow engineers to better optimize the p- and n-channel transistors for higher performance. Unfortunately, the number of processing steps overall is much higher with this approach. As researchers continue to investigate these challenges, we should see a clearer path forward for CFETs within the next 1-2 years.

Ask The Experts

Q: What does the acronym CESL stand for?

A: Thanks for your question. In semiconductor process technology, CESL stands for Contact Etch Stop Layer.

Course Spotlight: WAFER FAB PROCESSING

OVERVIEW

Semiconductor and integrated circuit developments continue to proceed at an incredible pace. The industry as a whole has gotten to this point of incredible complexity through the process of countless breakthroughs and developments in wafer fab processing. Today's wafer fab contains some of the most complex and intricate procedures ever developed by mankind.

Wafer Fab Processing is a 4-day course that offers an in-depth look into the semiconductor manufacturing process, and the individual processing technologies required to make them. We place special emphasis on the basics surrounding each technique, and we delve into the current issues related to manufacturing the next generation devices. This course is a must for every manager, engineer and technician working in the semiconductor industry, using semiconductor components or supplying tools to the industry.

By focusing on the basics of each processing step and the issues surrounding them, participants will learn why certain techniques are preferred over others. Our instructors work hard to explain how semiconductor processing works without delving heavily into the complex physics and mathematical expressions that normally accompany this discipline.

Participants will learn basic, but powerful, aspects about the semiconductor industry. This skill-building series is divided into three segments:

1. **Basic Processing Steps.** Each processing step addresses a specific need in IC creation. Participants will learn the fundamentals of each processing step and why they are used in the industry today.

2. **The Evolution of Each Processing Step.** It is important to understand how wafer fab processing came to the point where it is today. Participants will learn how each technique has evolved for use in previous and current generation ICs.

3. **Current Issues in Wafer Fab Processing.** Participants will learn how many processing steps are increasingly constrained by physics and materials science. They will also learn about the impact of using new materials in the fabrication process, and how those materials may create problems for the manufacturers in the future.

COURSE OBJECTIVES

1. The course will provide participants with an in-depth understanding of the semiconductor industry and its technical issues.

2. Participants will understand the basic concepts behind the fundamental wafer fab processing steps.

3. The course will identify the key issues related to each of the processing techniques, and their impact on the continued scaling of the semiconductor industry.

4. The course offers a wide variety of sample problems that participants will work to help them gain knowledge of the fundamentals of wafer fab processing.

5. Participants will be able to identify the basic features and principles associated with each major processing step. These include processes like chemical vapor deposition, ion implantation, lithography, and etching.

6. Participants will understand how processing, reliability, power consumption and device performance are interrelated.

7. Participants will be able to make decisions about how to construct and evaluate processing steps for CMOS, BiCMOS, and bipolar technologies.

See next page for course outline

COURSE OUTLINE

DAY 1

1. Basics and Fundamentals: Semiconductor Devices and ICs
   a. Acronyms
   b. Common Terminology
   c. Brief History
   d. Semiconductor Materials
   e. Electrical Conductivity
   f. Semiconductor Devices
   g. Classification of ICs and IC Processes
   h. Integrated Circuit Types

2. Crystallinity, Crystal Defects, Crystal Growth
   a. Crystallinity
   b. Crystal Defects
   c. Crystal Growth
   d. Controlling Crystal Defects

3. Basic CMOS Process Flow
   a. Transistors and Isolation
   b. Contacts/Vias Formation
   c. Interconnects
   d. Parametric Testing

4. Ion Implantation 1 (The Science)
   a. Doping Basics
   b. Ion Implantation Basics
   c. Dopant Profiles
   d. Crystal Damage and Annealing

5. Ion Implantation 2 (Equipment, Process Issues)
   a. Equipment
   b. Process Challenges
   c. Process Monitoring and Characterization
   d. New Techniques

7. Contamination Monitoring and Control
   a. Contamination Forms and Effects
   b. Contamination Sources and Control
   c. Contamination Characterization and Measurement

DAY 2

6. Thermal Processing
   a. Overview of Thermal Processing
   b. Process Applications of SiO_2
   c. Thermal Oxidation
   d. Thermal Oxidation Reaction Kinetics
   e. Oxide Quality
   f. Atomistic Models of Thermal Diffusion
   g. Thermal Diffusion Kinetics
   h. Thermal Annealing
   i. Thermal Processing Hardware
   j. Process Control

8. Wafer Cleaning
   a. Wafer Cleaning Strategies
   b. Chemical Cleaning
   c. Mechanical Cleaning

9. Vacuum, Thin Film, and Plasma Basics
   a. Vacuum Basics
   b. Thin Film Basics
   c. Plasma Basics

10. Chemical Vapor Deposition 1 (Basics, LPCVD, Epitaxy)
   a. CVD Basics
   b. LPCVD Films
   c. LPCVD Equipment
   d. Epi Basics
   e. Epi Process Applications
   f. Epi Deposition Process
   g. Epi Deposition Equipment

DAY 3

11. Physical Vapor Deposition
   a. PVD Basics
   b. Sputter Deposition Process
   c. Sputter Deposition Equipment
   d. Al-Based Films
   e. Step Coverage and Contact/Via Hole Filling
   f. Metal Film Evaluation

12. Lithography 1 (Photoresist Processing)
   a. Basic Lithography Process
   b. Photoresist Materials
   c. Photoresist Process Flow
   d. Photoresist Processing Systems

13. Lithography 2 (Image Formation)
   a. Basic Optics
   b. Imaging
   c. Equipment Overview
   d. Actinic Illumination
   e. Exposure Tools

14. Lithography 3 (Registration, Photomasks, RETs)
    a. Registration
    b. Photomasks
    c. Resolution Enhancement Techniques
    d. The Evolution of Optical Lithography

15. Etch 1 (Basics, Wet Etch, Dry Etch)
    a. Etch Basics
    b. Etch Terminology
    c. Wet Etch Overview
    d. Wet Etch Chemistries
    e. Types of Dry Etch Processes
    f. Physics and Chemistry of Plasma Etching

DAY 4

16. Etch 2 (Dry Etch Applications and Equipment)
    a. Dry Etch Applications
    b. SiO_2
    c. Polysilicon
    d. Al and Al Alloys
    e. Photoresist Strip
    f. Silicon Nitride
    g. Dry Etch Equipment
    h. Batch Etchers
    i. Single Wafer Etchers
    j. Endpoint Detection
    k. Wafer Chucks

17. Chemical Vapor Deposition 2 (PECVD)
    a. CVD Basics
    b. PECVD Equipment
    c. CVD Films
    d. Step Coverage

18. Chemical Mechanical Polishing
    a. Planarization Basics
    b. CMP Basics
    c. CMP Processes
    d. Process Challenges
    e. Equipment
    f. Process Control

19. Copper Interconnect, Low-k Dielectrics
    a. Limitations of "Conventional" Interconnect
    b. Copper Interconnect
    c. Cu Electroplating
    d. Damascene Structures
    e. Low-k IMDs
    f. Cleaning Cu and low-k IMDs

20. Leading Edge Technologies and Techniques
    a. Process Evolution
    b. Atomic Layer Deposition (ALD)
    c. High-k Gate and Capacitor Dielectrics
    d. Ni Silicide Contacts
    e. Metal Gates
    f. Silicon on Insulator (SOI) Technology
    g. Strained Silicon
    h. Hard Mask Trim Etch
    i. New Doping Techniques
    j. New Annealing Techniques
    k. Other New Techniques
    l. Summary of Industry Trends

Upcoming Courses:

Public Course Schedule:

IC Packaging Technology - January 23-24, 2024 (Tues.-Wed.) | Phoenix, Arizona - $1,295

Advanced CMOS/FinFET Fabrication - January 29-30, 2024 (Mon.-Tues.) | Phoenix, Arizona - $995

Fundamentals of High-Volume Production Test - January 29-30, 2024 (Mon.-Tues.) | Phoenix, Arizona - $1,295

Wafer Fab Processing - February 26-29, 2024 (Mon.-Thurs.) | Munich, Germany - $2,095 until Feb. 5, then $2,195

Failure and Yield Analysis - March 4-7, 2024 (Mon.-Thurs.) | Munich, Germany - $2,095 until Feb. 12, then $2,195

Semiconductor Reliability and Product Qualification - March 11-14, 2024 (Mon.-Thurs.) | Munich, Germany - $2,095 Until Feb. 19, then $2,195

Defect-Based Testing - March 20-21, 2024 (Wed.-Thurs.) | Munich, Germany - $1,195 until Feb. 26, then $1,295

Have an idea for a course? If you have a suggestion or a comment regarding our courses, online training, discussion forums, or reference materials, or if you wish to suggest a new course or location, please email us at info@semitracks.com

To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered, please contact Jeremy Henderson at jeremy.henderson@semitracks.com

We are always looking for ways to enhance our courses and educational materials and look forward to hearing from you!