SEMITRACKS, INC.

ISSUE 162
JANUARY
2023

INFOTRACKS

YOUR MONTHLY LOOK INSIDE SEMICONDUCTOR TECHNOLOGY

Semiconductor Cleanroom Technology

By Christopher Henderson

In last month's Feature Article, we continued our series on Cleanroom Technology by discussing some aspects of Cleanroom Construction. In this Feature Article, we will continue our discussion on Cleanroom Technology by discussing the Heating, Ventilation and Air Conditioning aspect of Cleanroom Construction.

(continued on page 2)

WHAT'S INSIDE?

Want to take control of your learning? See Page 8

UPCOMING COURSES:

EOS, ESD & How to Differentiate

Wafer Fab Processing

And more! See page 12 for more details

Heating, Ventilation and Air Conditioning, also known as HVAC (pronounced "H-vac") for cleanrooms requires special design. Figure 1 shows a cross-section diagram of a basic HVAC system for a cleanroom.

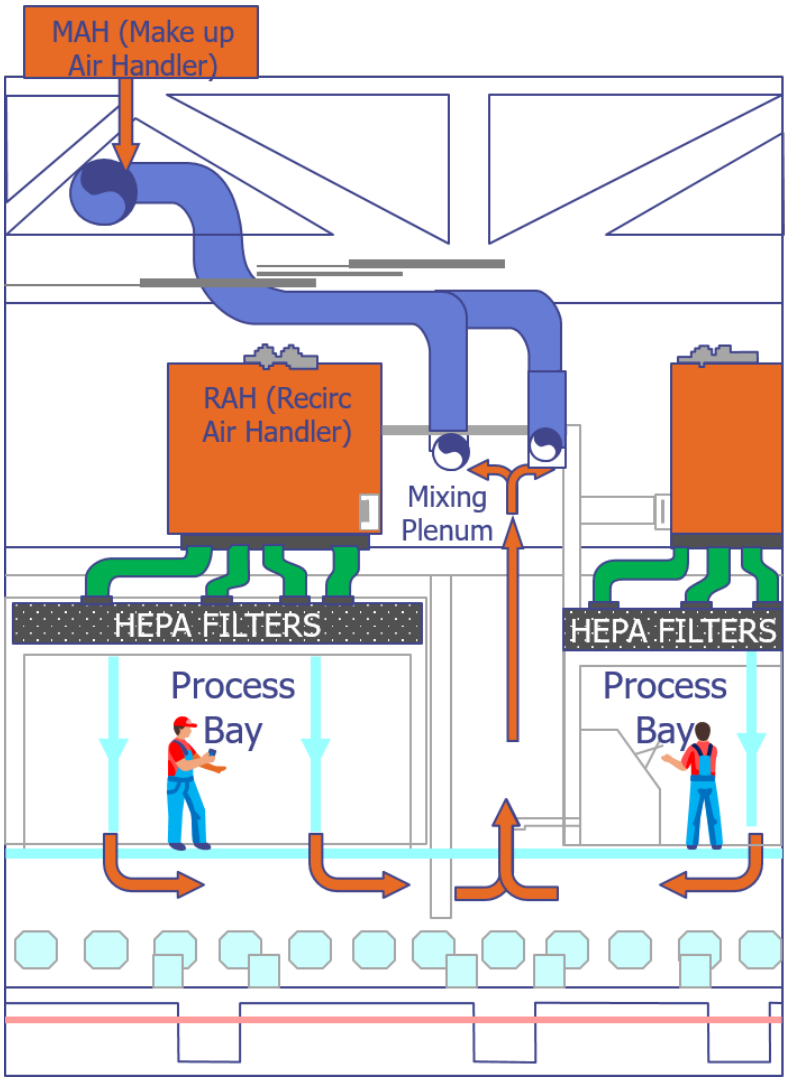

Figure 1- Cross-section diagram of a basic HVAC configuration for a cleanroom

In order to keep a cleanroom free from particles, the air exchange rate needs to be many times greater than a traditional HVAC system. Typically, the air in a cleanroom needs to be completely replaced every six seconds or so, so this requires large blowers. At the same, however, the volume of air

through the HVAC system should not generate turbulent airflow, so the airflow receptacles must be quite large. Typically, a large percentage of the ceiling and floor form the receptacles and return air vents. In addition, the HVAC system should not generate significant levels of vibration. This means that the air handlers must be mounted in such a way as to not cause vibrations, and moving parts must be well-maintained to ensure vibrations do not appear later during use. Power should be well-conditioned and designed and implemented in such a manner to minimize transients or spikes. Therefore, adequate surge protection is critical. Furthermore, power to a wafer fab cleanroom needs to be continuous, because sensitive tools can lose calibration or be damaged by a power failure. Therefore, backup power in case of main power failure is a must. This requires a combination of batteries for immediate response, and diesel generators for a more prolonged response.

State-of-the-art high-volume cleanrooms are highly complex building projects, so considerable planning and preparation are necessary. Heating, Ventilation and Air Conditioning plays a key role, as the environment must be ultra-clean and ultra-stable when it comes to temperature and humidity. Other environmental aspects like vibration and electromagnetic interference must also be highly controlled.
In next month's Feature Article, we will continue our discussion on Cleanroom Construction by covering the aspect of equipment placement.

Figure 2 is an example of a ballroom arrangement in a cleanroom. This arrangement has the advantage of the most flexibility for equipment placement. It also works best when the manufacturer plans to use an automated material handling system. However, the equipment will also exhaust into the same cleanroom space, so greater care may be required to prevent hazardous chemical leaks from harming personnel and contaminating the cleanroom environment.

Figure 2- Picture showing a ballroom-style cleanroom nearing completion of construction

Figure 3 is an example of a bay-chase arrangement in a cleanroom. The bay portion of the cleanroom is on the left, and the chase portion of the cleanroom is on the right. This arrangement has the advantage of allowing the utilities to be plumbed in to the tool through a chase environment, making servicing tools easier and preventing harm to personnel easier to implement. However, the bay-chase arrangement does not provide as much flexibility for equipment placement.

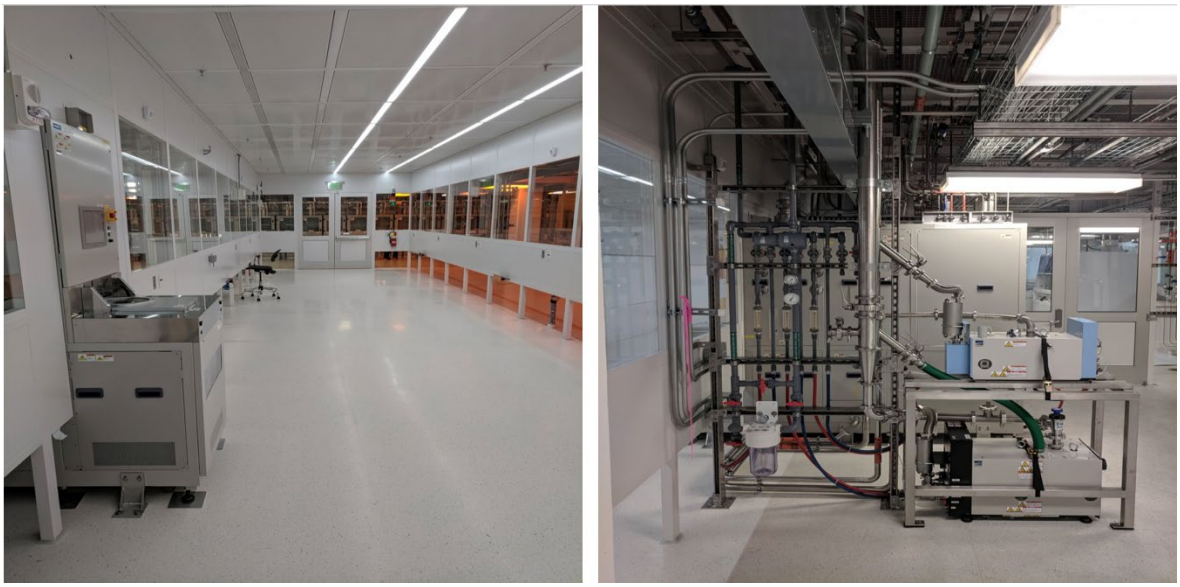

Figure 3- Cleanroom bay (left) and cleanroom chase (right) in a bay-chase configuration

Another important aspect of fab construction is equipment placement. In general, in a state-of-the-art fab, engineers try to place process tools in order to limit movement. Additional movement consumes time, so limiting movement is important. One can accomplish this by grouping module level tools together. For example, the gate stack module might consist of cleaning tools for the silicon surface, thermal oxidation furnaces for the gate oxide growth, and low pressure chemical vapor deposition for the polysilicon gate. These tools might be grouped in a local area or bay to reduce movement. Another factor in equipment placement is lighting. For example, lithography requires specialized light to prevent the premature exposure of photoresist. Furthermore, vibration isolation is more important for some processes. Process steps like lithography and ion implantation require nanometer-level placement, so vibration must be tightly controlled. Finally, Chemical Mechanical Polishing, or CMP, must often be dealt with independently. Since it is a dirty process, the process tools for CMP are often placed away from other tools, since the process can run the risk of contaminating other tools.

Fabs have historically been laid out so that all of the copies of the same type of tool appear together. There are several advantages to this type of functional layout. First, process tools have historically been quite unreliable, so it is desirable for all copies of a tool to be grouped together so that the copies can back each other up. Second, there will be some tools that perform multiple steps. For example, 17 steppers may be used to perform 22 masking operations. The steppers are grouped together because it is impossible to have a one-to-one assignment of steppers to masking steps. Third, one operator may be able to run multiple tools (for example, furnaces) as long as these tools are close enough together that the operator can access any of the tools easily. Fourth, similar tools may share a common set of facility needs. Despite these advantages, there is a growing cost of functional layouts as well. Because functional layouts do not reflect the sequence in which the tools are used in the process recipe, lots may have to traverse long, complicated, overlapping paths through the fab as they move from process step to process step. This problem becomes more serious as the number of steps increases and as lot transportation is automated. Factory modeling may be needed to evaluate different layout alternatives, such as a hybrid between functional layouts and a layout reflecting the process sequence. Figure 4 shows an example of a basic factory model to help understand the layout alternatives.

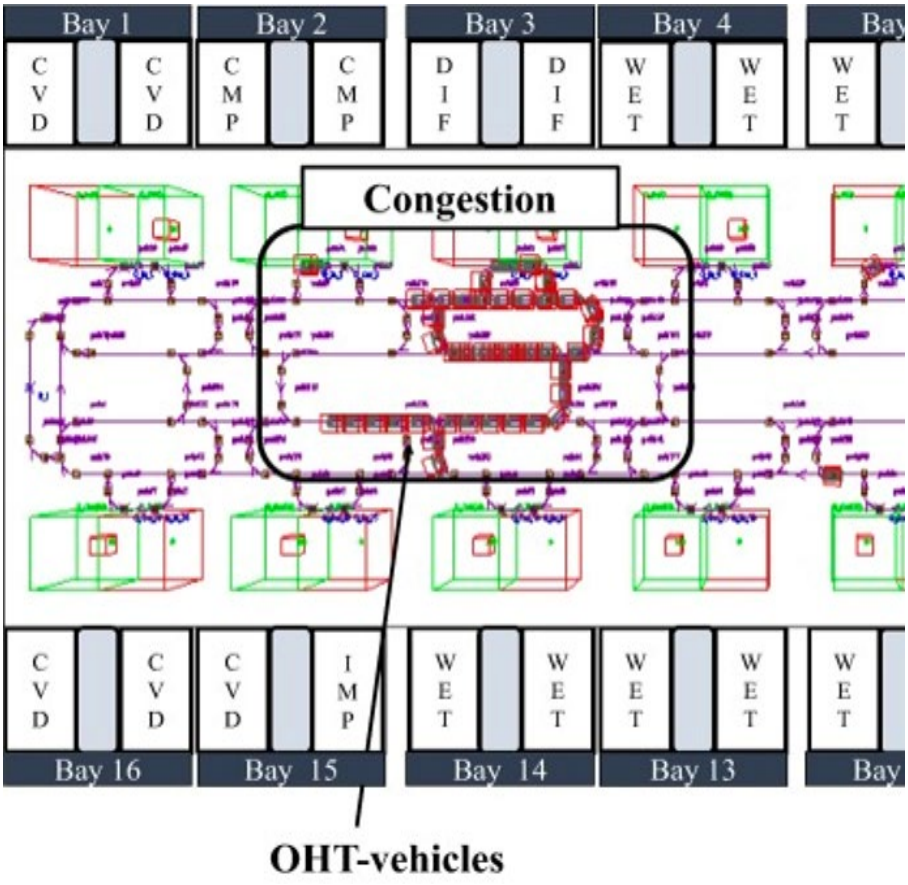

Figure 4- Basic factory model of a cleanroom showing congestion, which might be targeted as an opportunity for improving the workflow

Another important component of a modern fab is the Automated Material Handling System, or AMHS. We show a diagram of such a system in Figure 5. There are different types of AMHS implementations. These implementations can include one or more of the following systems: Automated Guidance Vehicles (AGVs), Rail Guided Vehicles (RGVs), Overhead Hoist Vehicle (OHV) and Overhead Transport (OHT) systems. AGV and RGV systems are more common in older 200mm fabs, while OHV and OHT systems are more common in 300mm fabs. In this image we show an example of an AMHS that contains both OHV and OHT systems. In conjunction with these systems in 300mm fabs, wafers are processed and transported in an enclosed container called a Front Opening Unified Pod (FOUP). A FOUP is transported from one set of equipment to another using an Overhead Hoist Transfer vehicle (OHT) system. The OHT travel rail can extend up to 10 kilometers with up to several hundred cars in large fabs, according to Daifuku, a major integrator of AMHS. To get everything working in unison, fabs use various factory automation technologies. Vendors also use WIP flow techniques, such as real-time dispatching and scheduling, to coordinate the fab flow.

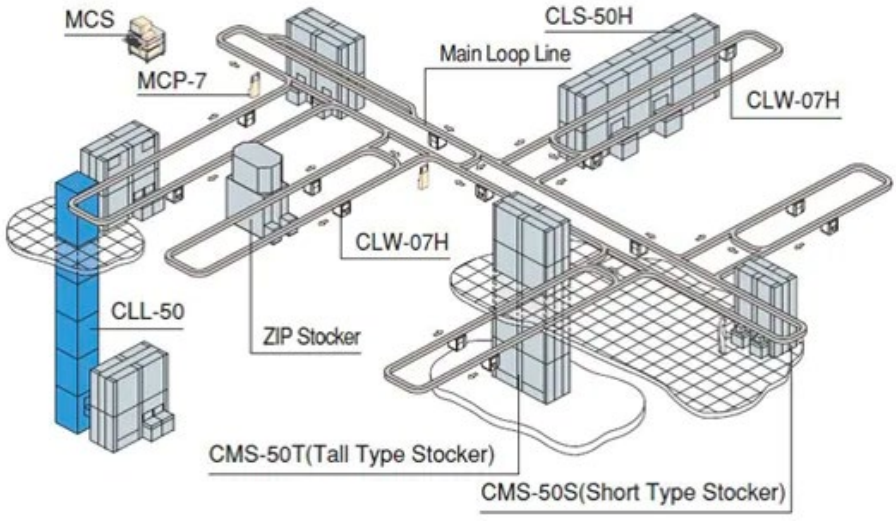

Figure 5- Diagram showing a schematic of an Automated Material Handling System, or AMHS

In conclusion, we finished our two-part section on cleanroom construction. State-of-the-art high-volume cleanrooms are highly complex building projects, so considerable planning and preparation are necessary. Heating Ventilation and Air Conditioning plays a key role, as the environment must be ultra-clean and ultra-stable when it comes to temperature and humidity. Other environmental aspects like vibration and electromagnetic interference must also be highly controlled. Equipment placement and fab process goals also play a key role in the construction of the fab. Because these construction projects are so complex, they are often classified as some of the most expensive construction projects when construction is underway. Just the shell of the building and cleanroom can run well in excess of $1Billion. In next month's feature article, we will begin a discussion on power usage in a semiconductor fabrication facility.

In next month's Feature Article, we will continue our discussion on Cleanroom Construction by covering the aspect of equipment placement.

Technical Tidbit: RowHammer Attacks

This month's Technical Tidbit covers a strange term that has been in the news in trade magazines recently, known as RowHammer. People attempting to "break into" certain types of chips will sometimes use what is known as a "RowHammer" attack to do this.

RowHammer is the phenomenon in which repeatedly accessing a row in a Dynamic Random Access Memory, or DRAM, chip causes bits in physically adjacent rows in the memory to change states from a logical "1" to a logical "0", or vice versa. We show the concept graphically in Figure 1.

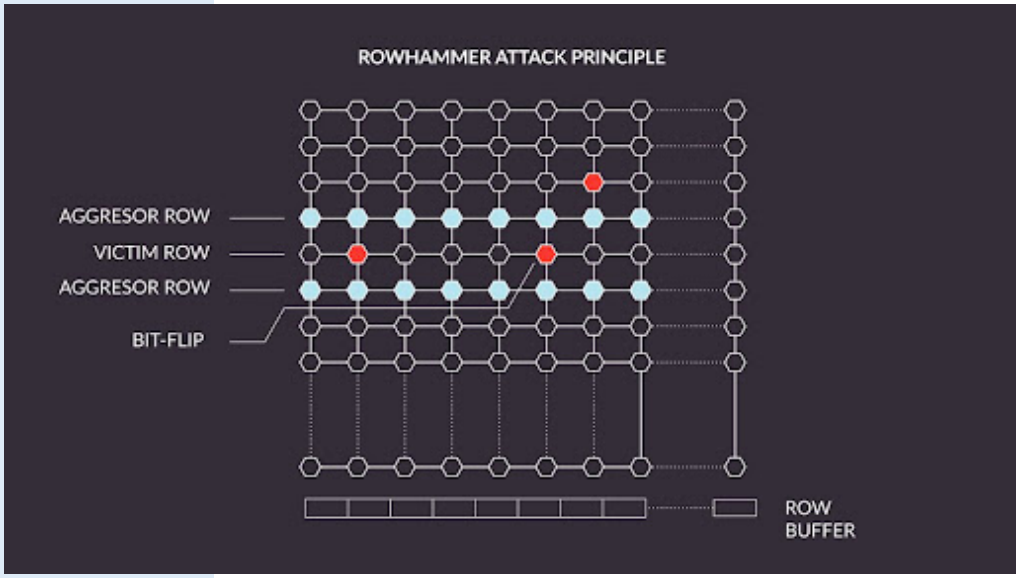

Figure 1- Diagram showing the fundamental concept behind a RowHammer attack

People with nefarious intent can use this behavior to cause a system to crash. This behavior was first demonstrated in 2014 by Yoongu Kim and a team of researchers working at Carnegie Mellon University. This results in data corruption, and leads to a serious and widespread system security vulnerability, as many other researchers have demonstrated since the original paper in 2014. Researchers have also demonstrated that the RowHammer phenomenon is getting much worse as DRAM technology scaling continues. In other words, newer DRAM chips are fundamentally more vulnerable to RowHammer at the device and circuit levels. Deeper analysis of RowHammer shows that there are several aspects to the problem as the vulnerability is sensitive to many variables, including environmental conditions, like temperature and voltage; process variation; stored data patterns; as well as memory access patterns and memory control policies. As such, engineers have had a difficult time developing fully-secure and very efficient (i.e., low-overhead in performance, energy, area) protection mechanisms against RowHammer. Furthermore, attempts made by DRAM manufacturers have been shown to lack security guarantees. Engineers continue to look for techniques to either solve, or at least mitigate, the problem. There are likely two aspects to the problem that need further study. One aspect is to better understand the problem at a fundamental physical level so that we can determine all of the factors that affect RowHammer sensitivity. Another aspect is that we need system-level solutions where the system and memory cooperate to identify and mitigate the data corruption problems that occur due to RowHammer attacks.

Ask The Experts

Q: How long does it take to implant a dose onto a wafer? Milliseconds, seconds, longer?

A: The typical dose time for a wafer is on the order of seconds. Obviously, the amount of the dose is a significant factor in the time. Larger doses for heavily-doped regions require longer implant times, whereas smaller doses for lightly-doped regions require less time.

Course Spotlight: Wafer Fab Processing

This is one of our public courses we are planning to hold in 2023. Stay tuned on our website for course announcements!

COURSE OBJECTIVES

With focused guidance from your instructor, you will gain insight into the following:

1. an in-depth understanding of the semiconductor industry and its technical issues.
2. an understanding of basic fundamental wafer fab processing steps.
3. key issues of each of the processing techniques and their impact on the continued scaling of the semiconductor industry.
4. sample problems to gain hands-on knowledge of the fundamentals of wafer fab processing
5. Identifying basic features and principles associated with each major processing step, including chemical vapor deposition, ion implantation, lithography, and etching.
6. understanding how processing, reliability, power consumption and device performance are interrelated
7. making decisions about how to construct and evaluate processing steps for CMOS, BiCMOS, and bipolar technologies.

INSTRUCTIONAL STRATEGY

By using a combination of instruction by lecture, classroom exercises, and question/answer sessions, you will learn practical information on semiconductor processing and the operation of this industry. From the very first moments of the seminar until the last sentence of the training, the driving focus is **application**. Our instructors are internationally recognized experts in their fields, who have years of current, relevant expertise in this field. The course notes offer dozens of pages of additional reference material you can use on the job.

OVERVIEW

Semiconductor and integrated circuit developments continue to proceed at an incredible pace. The industry as a whole has gotten to this point of incredible complexity through the process of countless breakthroughs and developments in wafer fab processing. Today's wafer fab contains some of the most complex and intricate procedures ever developed by mankind. ***Wafer Fab Processing*** is a 4-day course that offers an in-depth look into the semiconductor manufacturing process, and the individual processing technologies required to make them. We place special emphasis on the basics surrounding each technique, and we delve into the current issues related to manufacturing the next generation devices. This course is a must for every manager, engineer and technician working in the semiconductor industry, using semiconductor components or supplying tools to the industry.

By focusing on the basics of each processing step and the issues surrounding them, participants will learn why certain techniques are preferred over others. Our instructors work hard to explain how semiconductor processing works without delving heavily into the complex physics and mathematical expressions that normally accompany this discipline.

Participants learn basic but powerful aspects about the semiconductor industry. This skill-building series is divided into three segments:

1. Basic Processing Steps: each processing step addresses a specific need in IC creation. Participants learn the fundamentals of each processing step and why they are used in the industry today.

2. The Evolution of Each Processing Step: it is important to understand how wafer fab processing came to the point where it is today. Participants learn how each technique has evolved for use in previous and current generation ICs.

3. Current Issues in Wafer Fab Processing: p articipants learn how many processing steps are increasingly constrained by physics and materials science. They also learn about the impact of using new materials in the fabrication process and how those materials may create problems for the manufacturers in the future.

COURSE OUTLINE

Day 1

1. Introduction
2. Silicon Basics
    a. Crystallinity
    b. Crystal Defects
    c. Crystal Growth
3. Basic CMOS Process Flow
4. Ion Implantation

Day 2

5. Thermal Processing
    a. Thermal Processing
        a. Diffusion
        b. Oxidation
        c. Rapid Thermal Processing
6. Cleanliness
    a. Contamination Monitoring
    b. Wafer Cleaning
7. Vacuum-Related Fundamentals
    a. Vacuum Basics
    b. Thin Film Basics
    c. Plasma Basics

Day 3

8. Chemical Vapor Deposition
    a. CVD Basics
    b. Low Pressure CVD
    c. Epitaxy
    d. Plasma-Enhanced CVD
9. Physical Vapor Deposition
    a. Evaporation
    b. Sputtering
10. Lithography
    a. Photoresist
    b. Processing
    c. Image Formation
    d. Photomasks

Day 4

9. Etch
    a. Etch Basics
    b. Wet Etch
    c. Dry Etch
    d. Dry Etch Applications and Equipment
10. Chemical Mechanical Planarization
11. Advanced Topics
    a. Multi-Level Interconnect Processing
    b. Atomic Layer Deposition
    c. Shallow Trench Isolation
    d. Silicon on Insulator

Upcoming Courses

EOS, ESD and How to Differentiate
March 6-7, 2023 (Mon.-Tues.) | Munich, Germany

Semiconductor Reliability and Product Qualification
March 13-16, 2023 (Mon.-Thurs.) | Munich, Germany

Wafer Fab Processing
March 13-16, 2023 (Mon.-Thurs.) | Munich, Germany

Failure and Yield Analysis
March 20-23, 2023 (Mon.-Thurs.) | Munich, Germany

Failure and Yield Analysis
May 1-4, 2023 (Mon.-Thurs.) | Oro Valley, Arizona

Semiconductor Reliability and Product Qualification
May 8-11, 2023 (Mon.-Thurs.) | Oro Valley, Arizona

Have an idea for a course? If you have a suggestion or a comment regarding our courses, online training, discussion forums, or reference materials, or if you wish to suggest a new course or location, please email us at info@semitracks.com

To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered, please contact Jeremy Henderson at jeremy.henderson@semitracks.com

We are always looking for ways to enhance our courses and educational materials and look forward to hearing from you!