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InfoTracks

Semitracks Monthly Newsletter

Thermal Detection Techniques

By Christopher Henderson

This month, we will conclude our series of Feature Articles by discussing Fluorescent Microthermal Imaging, or FMI. FMI uses a compound's temperature-dependent fluorescence to provide thermal mapping. It provides direct quantitative conversion of surface temperature into visible photons. FMI is traditionally performed using a rare earth chelate called Europium Thenotrifluoroacetonate or EuTTA. EuTTA produces a bright orange fluorescence that has a known function with respect to temperature. EuTTA is also conveniently excited by ultraviolet light, making it straightforward to use for FMI.

In order to understand how FMI works, let's review the basics of fluorescent compounds. Researchers worked with a number of fluorescent compounds in the 1950s and 1960s while studying laser behavior. Some of the compounds they studied included materials with rare earth chelates like lanthanum, samarium, europium, gadolinium, terbium, dysprosium, thulium, ytterbium, and lutetium. Europium is of particular interest, since there are several beta-diketone chelates available. One of these is Europium Thenotrifluoroacetonate or EuTTA. EuTTA did not succeed as a lasing compound because its fluorescence falls off rapidly as it heats. However, this makes it ideal as a heat sensing compound for failure analysis. Like we show in Figure 1, ultraviolet energy is pumped into

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the TTA ligand and absorbed. Within the molecule, energy is transferred to the europium atom, causing it to fluoresce in the visible range.

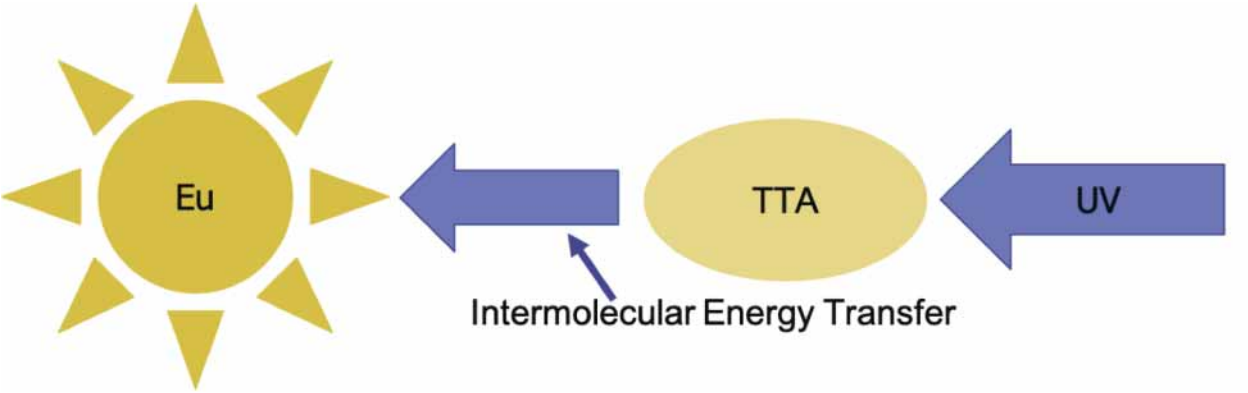


Figure 1. Basic concept behind energy transfer in FMI.

One of the strengths of FMI is its combination of spatial resolution and temperature sensitivity. FMI has been demonstrated to have a spatial resolution of better than 1μm and a temperature resolution of .01K. The theoretical limits for the technique are around 0.35μm spatial resolution, limited by the Rayleigh criteria, and 1mK, limited by the photon shot noise and the sensitivity of the camera system.

Figure 2 shows an example of the image produced by FMI. The basic procedure is to take a cold image, or an image of the device with no power applied, and divide it by a hot image, or an image with power applied. Although some further image manipulation is needed, this produces an image with just thermal data, showing where power is being dissipated on the device.

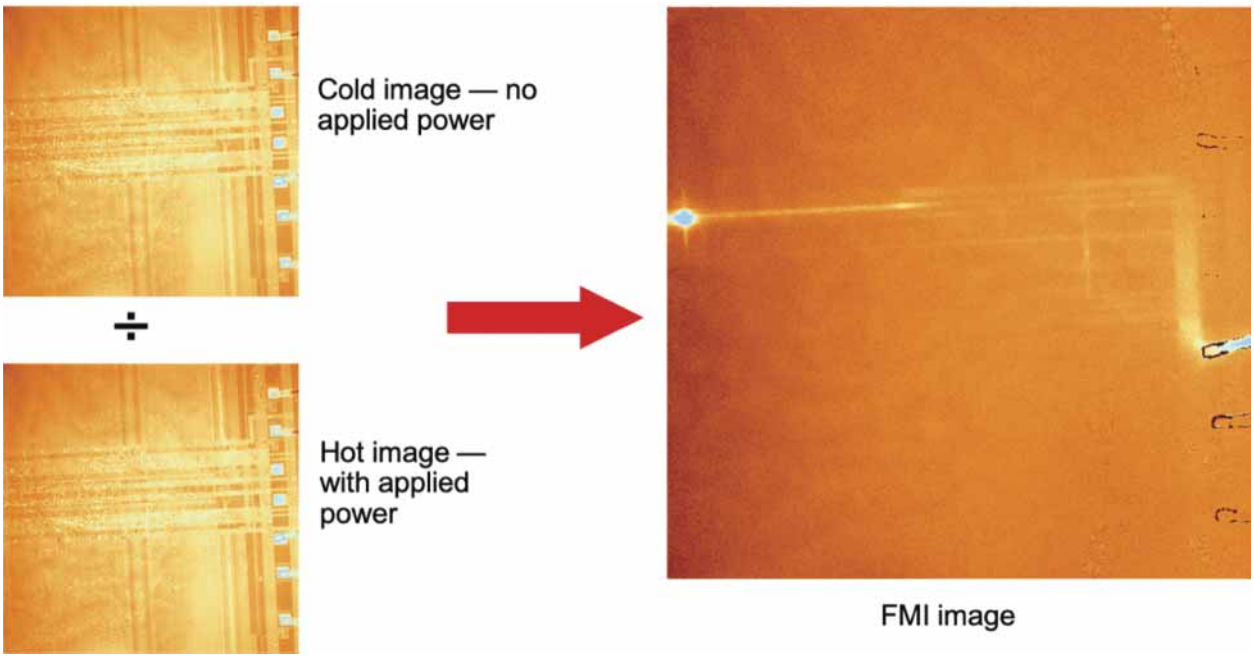


Figure 2. Example of an image produced by FMI.

Let's now look at some examples using FMI to isolate failures. The first example involves a single SRAM that failed electrical testing after burn-in. An IDDQ versus VDD curve showing the shorted condition is shown in Figure 3. Notice that the curve has a linear region above 1V, indicating a resistive short is present.

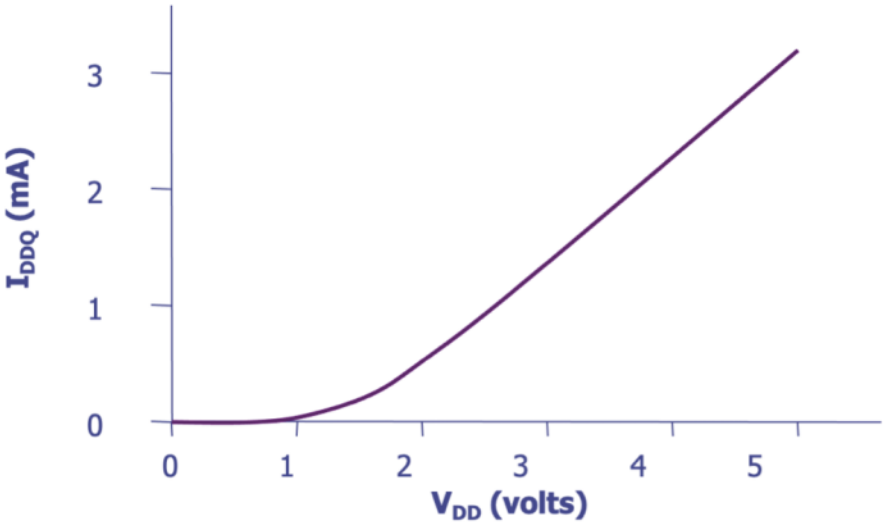


Figure 3. Current-Voltage curve of defect suitable for FMI analysis..

This SRAM failure was in a portion of the memory. No light emission was detected on this sample. The circuit exhibited an elevated background current of around 3.0mA at 5.0V. Normally, the background current should be on the order of 1µA or less for correctly working SRAMs of this size in this technology. Figure 4 is an FMI image overlaid with a reflected light image of the area of the SRAM where the heat is being generated. Notice the bright area indicated by the arrow.

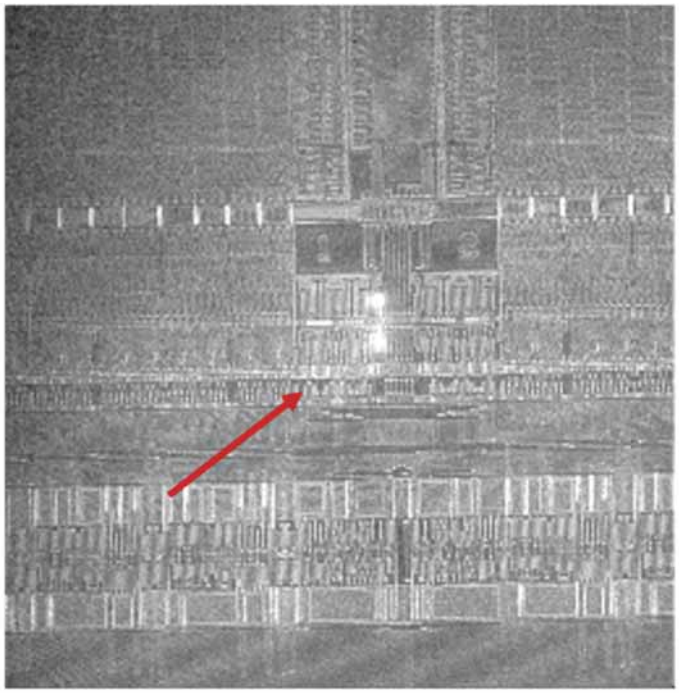


Figure 4. FMI image overlaid on a reflected light image of an SRAM that is failing.

In Figure 5, the left image shows an SEM image of the hot spot area. Notice the particle that is visible, indicated by the arrow. The image on the right of Figure 5 shows an FIB cross section of that particle. Notice that it appears to be bridging two metal lines.

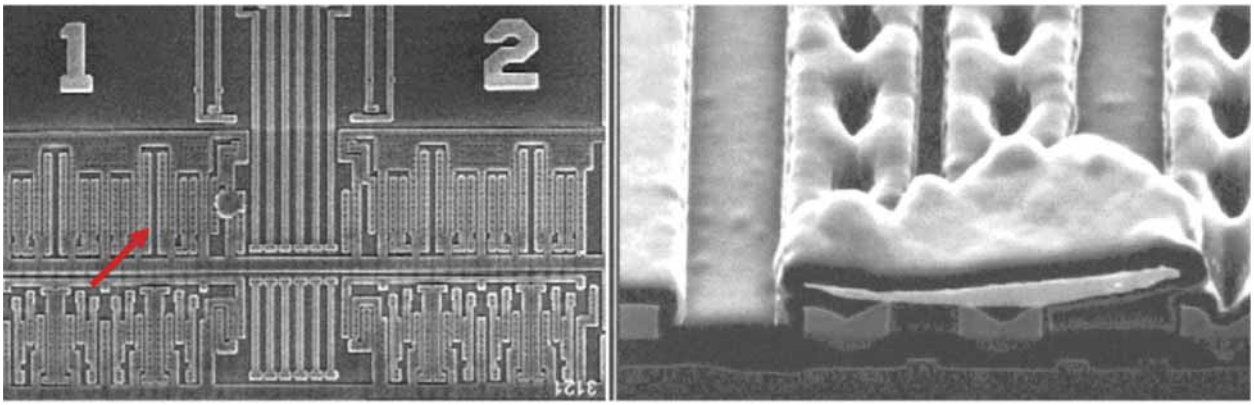


Figure 5. SEM image (left) and FIB image (right) of the defect responsible for the power dissipation imaged with FMI in Figure 4.

Figure 6 shows an energy dispersive x-ray spectrum of the materials in the particle. In addition to the normal elements seen on an integrated circuit, such as silicon, nitrogen, oxygen and titanium, we also have iron, nickel and chromium present. The presence of iron, nickel and chromium is a good indication that the particle is stainless steel.

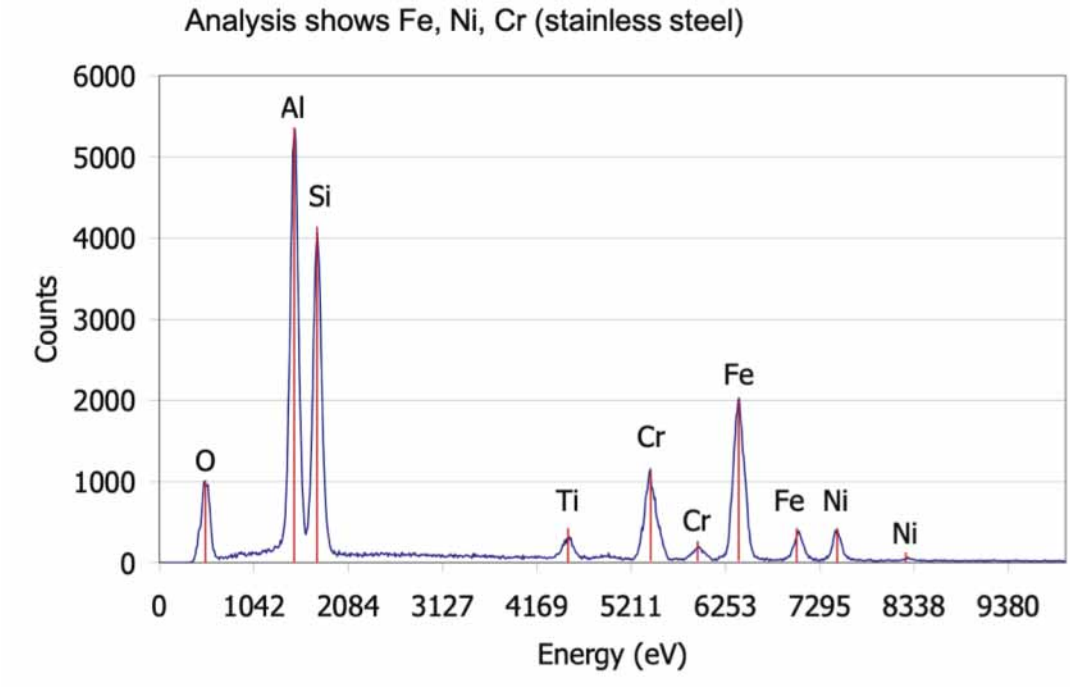


Figure 6. Energy Dispersive X-Ray Spectrum of particle seen in Figure 5.

Figure 7 is probably the most visually interesting of the FMI examples in this article. This 256k SRAM failed electrical testing due to high current after wafer processing. The image on the left of Figure 7 shows the FMI data, while the image on the right shows just the background, or cold image. Notice that the defect, located on the far left in the left-hand image, shows up brightly, as does the bond wire on the right side of the left-hand image. The bond wire is at an elevated temperature, because the heat generated by the high current in it cannot be easily dissipated to the air surrounding it. On the other hand, the heat on the metal lines within the chip can be more easily dissipated into the silicon. A network of metal interconnect is visible in the left image. Even though the current follows a single path, the heat can spread down all of the branches easily, since aluminum has a high thermal conductivity.

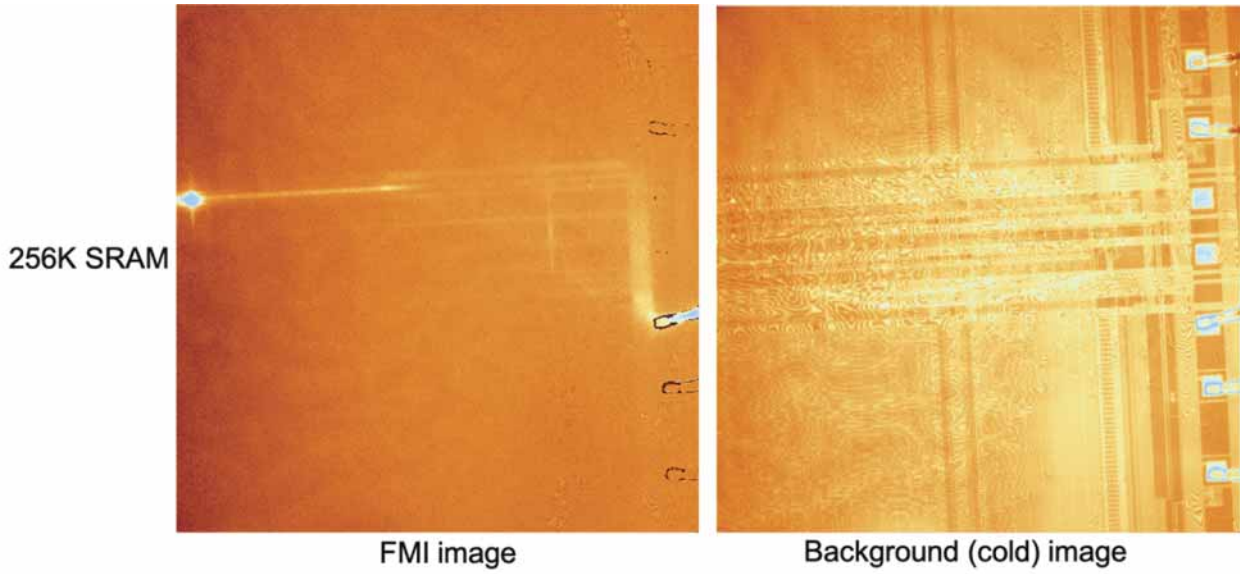


Figure 7. Images of 256K SRAM with shorts, creating excess power dissipation.

Figure 8 shows that the high current seen at electrical testing was the result of a photolithographic defect at metal-1.

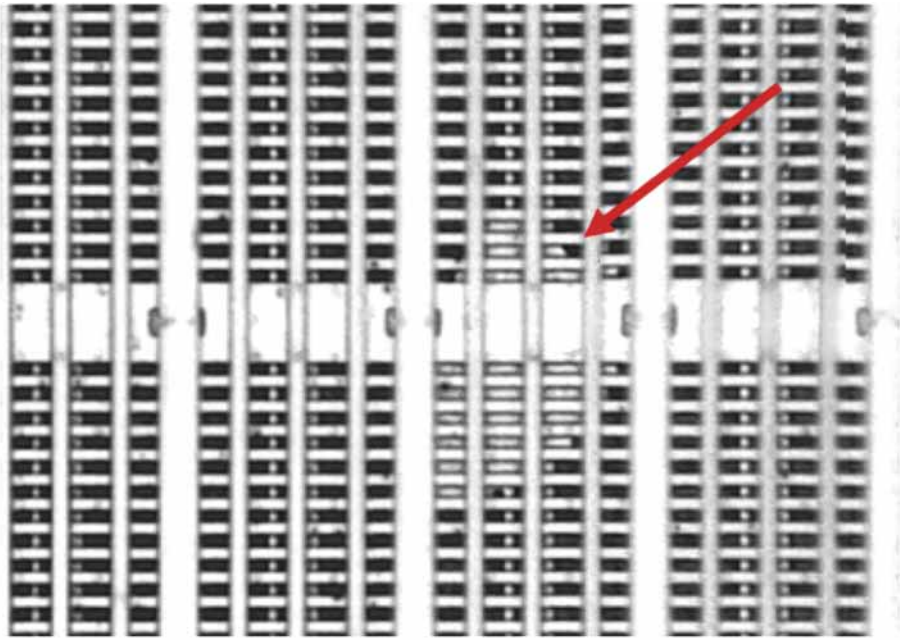


Figure 8. Defect responsible for thermal dissipation due to high current seen with FMI in Figure 7.

In conclusion, Figure 9 shows a comparison of the three thermal imaging techniques we have discussed in the Feature Articles. The structure being used is an electromigration test structure with 100mA of current applied. While 100mA seems like a lot, the power density is quite low, and this level of current results in only a 4°C rise in the temperature of the structure. An Infrared Thermal image is shown on the left of Figure 9, a Liquid Crystal image is shown in the center, and an FMI image is shown on the right. Notice the poor spatial resolution in the left image of Figure 9, the mottled appearance and digital information in the center image, and the higher spatial and thermal resolution in the FMI image on the right.

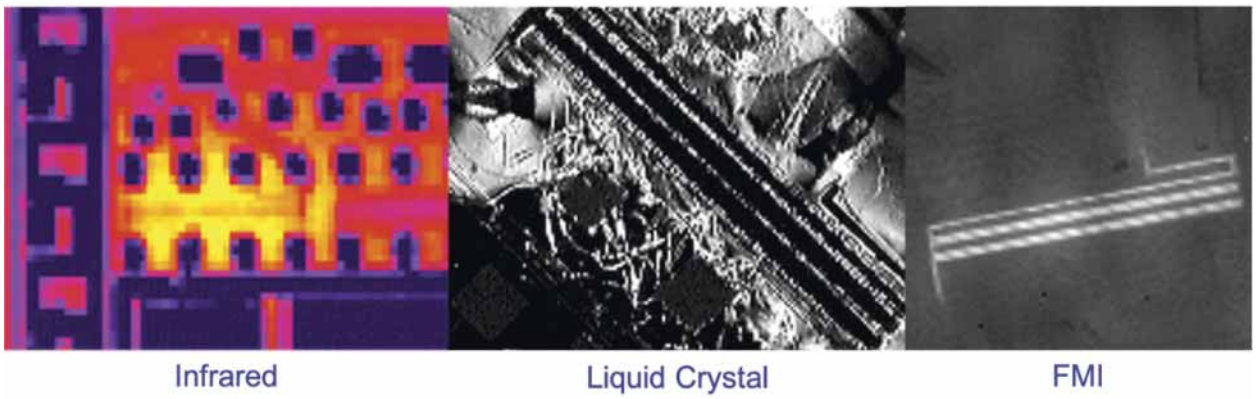


Figure 9. Comparison of Infrared Thermography, Liquid Crystal Thermography,

and Fluorescent Microthermal Imaging.

In summary, there are three popular techniques for thermal defect detection: Infrared Thermography, Liquid Crystal Thermography, and Fluorescent Microthermal Imaging. All three of these techniques have been in use for over 40 years in the FA community. The three techniques exhibit different characteristics. Infrared Thermography and Fluorescent Microthermal Imaging give static maps of surface temperatures, while liquid Crystal Thermography can provide a real-time image of thermal activity. FMI and Liquid Crystals rely on a compound to convert heat to optical information, while Infrared Thermography is total non-contact.

Technical Tidbit

Datasheet Limits

This month's Technical Tidbit introduces the concept of setting datasheet limits. As a semiconductor industry professional, it is important to understand that the process of characterizing the components for a customer's application, or for generic applications (known as Silicon Validation) is done only on a sample of devices, not the entire population, so that means we need to have a wide set of limits to account for the entire population, and the fact that the manufacturing process will vary over time. We require a tight distribution at validation, like we show on the left in Figure 1 to account for more significant variation. On the right in Figure 1, the taller, wider distribution represents the distribution for an entire population we would see at final test, and the shorter distribution represents the sample of devices we would see at validation.

Figure 1. Hypothetical parameter distribution at validation (left) and at final test (right).

A chip manufacturer will typically create two sets of test limits: one external, and one internal. The external limits will be based on the product specification, and the internal limits will be based on data acquired during the silicon validation process. The internal limits will typically be tighter than the external limits. More specifically, the internal limits will be set according to the distribution type, the process capability index (Cpk) requirements used in the manufacturing process, and the customer Defect Parts Per Million (DPPM) requirements. One can then use outlier methodologies to improve the DPPM levels and reliability by eliminating devices that fall outside the distribution, but lie within the external limits, denoted by the Product Data Sheet upper and lower limits (PDS(U) and PDS(L)). To illustrate what we mean by outliers, see Figure 2. One method to use that can provide tighter control is Dynamic Part Average Testing.

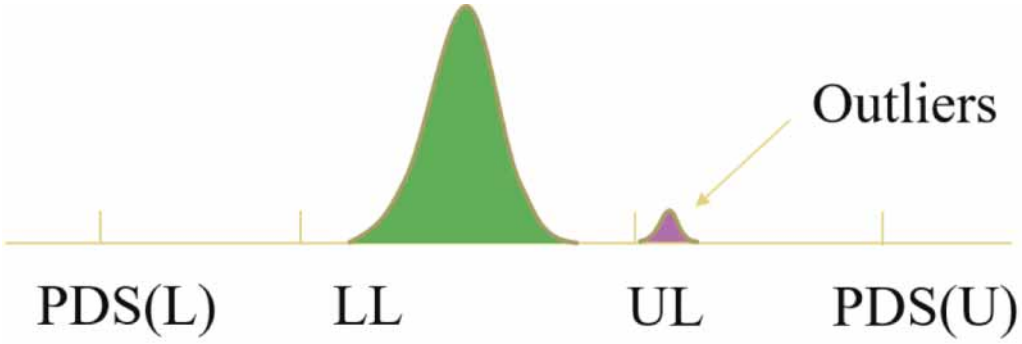


Figure 2. Graph explaining the concept of outlier components for a hypothetical parameter.

Let's now discuss the basic procedure for setting datasheet limits. First, we start with bogeys, or estimated target values. We would then characterize 30 units across a temperature range. 30 is a good number because it will provide confidence at a certain level that you have a normal distribution. Now that we have a histogram of values, you can calculate the limits at each temperature. We can then define a worst case minimum and maximum value for each parameter. We can then determine if we require guardbands, since it may be necessary to limit the amount of test time to just one particular test temperature, which is typically room temperature. Next, we would run a larger sample size to help characterize the yield of the product. This would typically be done using samples from multiple wafer lots, multiple testers, multiple tester sites, and so forth. It is also very useful and important to get feedback from engineers involved with the actual application of the product, like product engineers, application engineers, and system engineers. We will need to perform this testing on a statistically significant sample size. Once the data is collected, we need to discuss it with the product team to see if these results will be sufficient for the customer. We can also determine at this time if we need to modify the device specifications, or add additional test temperatures (known as test insertions) into the testing flow.

When the chip designers are working on setting up test limits, they need to account for a number of variability factors. These include:

- Distribution associated with fab manufacturing
- Distribution associated with assembly/packaging
- Shifts due to stress
- Distribution within the tester
- Shifts between testers
- Shifts between handler interface boards/device interface boards
- Variations in components
- Shifts between sites

We show an example of site-to-site variation in Figure 3.

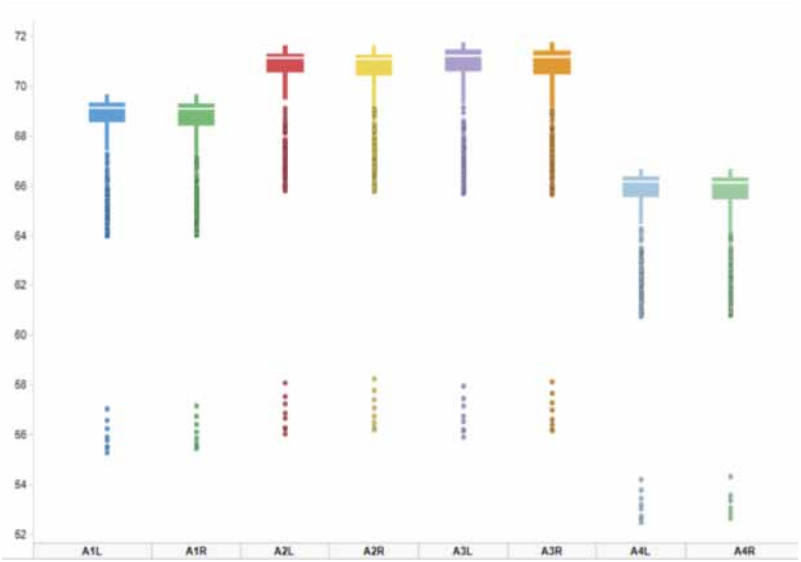


Figure 3. Example of test site variation for a hypothetical parameter.

Testing generates its own set of variability issues. Each tester is not exactly alike. Even if the manufacturer uses testers that are all the same make and model, they will not be exactly alike. This leads to problems. For example, the test engineer might see a variation in input low level leakage (e.g. IIL = 26.285uA on tester A, 26.274uA on tester B). These types of errors can be characterized using linear regression. These differences can result in devices passing on one tester (tester A) and failing on another tester (tester B). These types of errors can be characterized using Pivot tables. These problems can be quite difficult to fix, requiring in-depth troubleshooting with known "golden" devices.

Another important consideration is correlation between lab bench results and Automated Test Equipment (ATE) results. Once in production, the parts will be tested on ATE, but the parts need to work in real-world applications. This is where bench testing comes into play. A bench setup can be made to more closely match the system configuration. The results between ATE and bench testing need to correlate. In production test, we normally just get a single value for a parameter, whereas with bench testing, we typically look at waveform results for anomalies. If there are differences, they need to be resolved before finalizing the datasheet limits. Examples of issues might include glitches, spikes, ramp times, or other phenomenon that may only be seen in waveform data.

Ask the Experts

Q: Do High-K dielectric materials have worse aging degradation such as HCI/BTI/TDDB than traditional silicon dioxide considering that High-K dielectric materials have more traps?

A: The answer is yes. High-K dielectric materials do have worse aging degradation, so they need to be used in conditions where the electric fields and voltages are lower than we use with traditional silicon dioxide materials.

Spotlight: Semiconductor Reliability and Product Qualification

OVERVIEW

Package reliability and product qualification continues to evolve with the electronics industry. New electronics applications require new approaches to reliability and qualification. In the past, reliability meant discovering, characterizing and modeling failure mechanisms and determining their impact on the reliability of the circuit. Today, reliability can involve tradeoffs between performance and reliability, assessing the impact of new materials, dealing with limited margins, etc. in particular, the proliferation of new package types. This requires information on subjects like: statistics, testing, technology, processing, materials science, chemistry, and customer expectations. While customers expect high reliability levels, incorrect testing, calculations, and qualification procedures can severely impact reliability. Your company needs competent engineers and scientists to help solve these problems. ***Semiconductor Reliability and Qualification*** is a four-day course that offers detailed instruction on a variety of subjects pertaining to semiconductor reliability and qualification. This course is designed for every manager, engineer, and technician concerned with reliability in the semiconductor field, qualifying semiconductor components, or supplying tools to the industry.

What Will I Learn By Taking This Class?

Participants learn to develop the skills to determine what failure mechanisms might occur, and how to test for them, develop models for them, and eliminate them from the product.

1. **Overview of Reliability and Statistics.** Participants learn the fundamentals of statistics, sample sizes, distributions and their parameters.
2. **Failure Mechanisms.** Participants learn the nature and manifestation of a variety of failure mechanisms that can occur both at the die and at the package level. These include: time-dependent dielectric breakdown, hot carrier degradation, electromigration, stress-induced voiding, moisture, corrosion, contamination, thermomechanical effects, interfacial fatigue, etc.
3. **Qualification Principles.** Participants learn how test structures can be designed to help test for a particular failure mechanism.
4. **Test Strategies.** Participants learn about the JEDEC test standards, how to design screening tests, and how to perform burn-in testing effectively.

COURSE OBJECTIVES

1. The seminar will provide participants with an in-depth understanding of the failure mechanisms, test structures, equipment, and testing methods used to achieve today's high reliability components.
2. Participants will be able to gather data, determine how best to plot the data and make inferences from that data.
3. The seminar will identify the major failure mechanisms, explain how they are observed, how they are modeled, and how they are eliminated.
4. The seminar offers a variety of video demonstrations of analysis techniques, so the participants can get an understanding of the types of results they might expect to see with their equipment.

5. Participants will be able to identify the steps and create a basic qualification process for semiconductor devices.
6. Participants will be able to knowledgeably implement screens that are appropriate to assure the reliability of a component.
7. Participants will be able to identify appropriate tools to purchase when starting or expanding a laboratory.

COURSE OUTLINE

Day 1 (Lecture Time 8 Hours)

1. Introduction to Reliability
    1. Basic Concepts
    2. Definitions
    3. Historical Information
2. Statistics and Distributions
    1. Basic Statistics
    2. Distributions (Normal, Lognormal, Exponent, Weibull)
    3. Which Distribution Should I Use?
    4. Acceleration
    5. Number of Failures

Day 2 (Lecture Time 8 Hours)

1. Overview of Die-Level Failure Mechanisms
    1. Time Dependent Dielectric Breakdown
    2. Hot Carrier Damage
    3. Negative Bias Temperature Instability
    4. Electromigration
    5. Stress Induced Voiding
2. Package Level Mechanisms
    1. Ionic Contamination
    2. Moisture/Corrosion
        1. Failure Mechanisms
        2. Models for Humidity
        3. Tja Considerations
        4. Static and Periodic stresses
        5. Exercises
    3. Thermo-Mechanical Stress
        1. Models
        2. Failure Mechanisms
    4. Interfacial Fatigue
        1. Low-K fracture
    5. Thermal Degradation/Oxidation

Day 3 (Lecture Time 8 Hours)

1. Package Attach (Solder) Reliability
    1. Creep/Sheer/Strain
    2. Lead-Free Issues
    3. Electromigration/Thermomigration
    4. MSL Testing
    5. Exercises
2. TSV Reliability Overview
3. Board Level Reliability Mechanisms
    1. Interposer
    2. Substrate
4. Electrical Overstress/ESD
5. Test Structures and Test Equipment
6. Developing Screens, Stress Tests, and Life Tests
    1. Burn-In
    2. Life Testing
    3. HAST
    4. JEDEC-based Tests
    5. Exercises

Day 4 (Lecture Time 8 Hours)

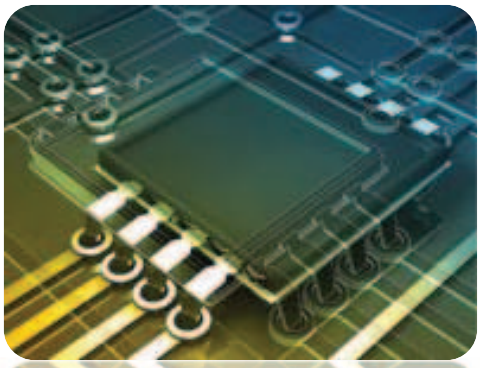
1. Calculating Chip and System Level Reliability
2. Developing a Qualification Program
    1. Process
    2. Standards-Based Qualification
    3. Knowledge-Based Qualification
    4. MIL-STD Qualification
    5. JEDEC Documents (JESD47H, JESD94, JEP148)
    6. AEC-Q100 Qualification
    7. When do I deviate? How do I handle additional requirements?
    8. Exercises and Discussion

INSTRUCTIONAL STRATEGY

By using a combination of instruction by lecture, video, problem solving and question/answer sessions, participants will learn practical approaches to the failure analysis process. From the very first moments of the seminar until the last sentence of the training, the driving instructional factor is **application**. We use instructors who are internationally recognized experts in their fields that have years of experience (both current and relevant) in this field. The handbook offers hundreds of pages of additional reference material the participants can use back at their daily activities.

The Semitracks Analysis Instructional Videos™

One unique feature of this workshop is the video segments used to help train the students. Reliability Analysis is a visual discipline. The ability to identify nuances and subtleties in graphical data is critical to locating and understanding the defect. Some tools output video images that must be interpreted by engineers and scientists. No other course of this type uses this medium to help train the participants. These videos allow the analysts to directly compare material they learn in this course with real analysis work they do in their daily activities.



Upcoming Webinars

(Click on each item for details)

Wafer Fab Processing

4 sessions of 4 hours each
US: February 28 – March 3, 2022
(Mon – Thur), 11:00 A.M. – 3:00 P.M. EST;
8:00 A.M. – 12:00 noon PST

Semiconductor Reliability / Product Qualification

4 sessions of 4 hours each
US: March 7 – 10, 2022 (Mon – Thur),
11:00 A.M. – 3:00 P.M. EST;
8:00 A.M. – 12:00 noon PST

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To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered in the next newsletter, please contact Jeremy Henderson by Email (jeremy.henderson@semitracks.com).

We are always looking for ways to enhance our courses and educational materials.

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To post, read, or answer a question, visit our forums.
We look forward to hearing from you!