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Decapsulation Overview

By Christopher Henderson

This month we will cover an overview of decapsulation. For standard plastic packages, there are two basic methods for exposing the die surface—a standard chemical etch by hand, or an automated approach that uses a machine called a Jet Etch. The manual approach is quite inexpensive. Assuming one has the appropriate chemical handling facilities such as an acid storage cabinet, appropriate protective gear, beakers, and a fume hood, the etch can be accomplished with a small amount of red fuming nitric acid. Red fuming nitric acid is quite dangerous, and should not be handled carelessly. One should always wear the appropriate protective clothing when performing a chemical etch of this type. The analyst should wear acid-resistant gloves, a smock, goggles or more preferably, a face shield, and closed-toed shoes. The red fuming nitric acid must also be heated to approximately 80°C to achieve decent results. Red fuming nitric acid emits toxic vapors, so this type of etch should always be performed in a fume hood with a working exhaust system. An etch performed by hand can lead to uneven results. It is preferable to practice on one or more parts before attempting the etch on the actual failed device. In contrast the Jet Etch machine can use either sulfuric or nitric acid. The machine heats the acid internally and uses a small amount to accomplish the etch. Although it is best to place the machine in a fume hood, it can be operated safely outside of one. The biggest drawback is the initial expense of the system. A new Jet Etch system will cost between $35,000 and

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$50,000 (US). However, once purchased, the machine will use less acid and deliver more consistent results than can be done by hand.

Jet Etch decapsulation is normally the preferred method for decapping plastic packaged parts. The system can accommodate a variety of package configurations and die sizes. It is also safe to use, fast, and easy to operate.

Figure 1. A typical Jet Etch decapsulation system (Photo courtesy Nisene Technology)

The plumbing for a Jet Etch system is shown in Figure 2. Acid is pumped from one or both of the acid supply containers into the pump mix/flow control chamber, where the acid is heated and mixed. The hot mixture then travels to the chamber where it is then sprayed onto the surface of the plastic package. A gasket can be used to help control the area over which the acid contacts the package. The heat exchanger helps to cool the package during the etch process. The used acid and the waste then travel to an acid waste bottle. A waste diversion valve can help make the job of disposal easier by separating various types of waste products from decap to decap operation.

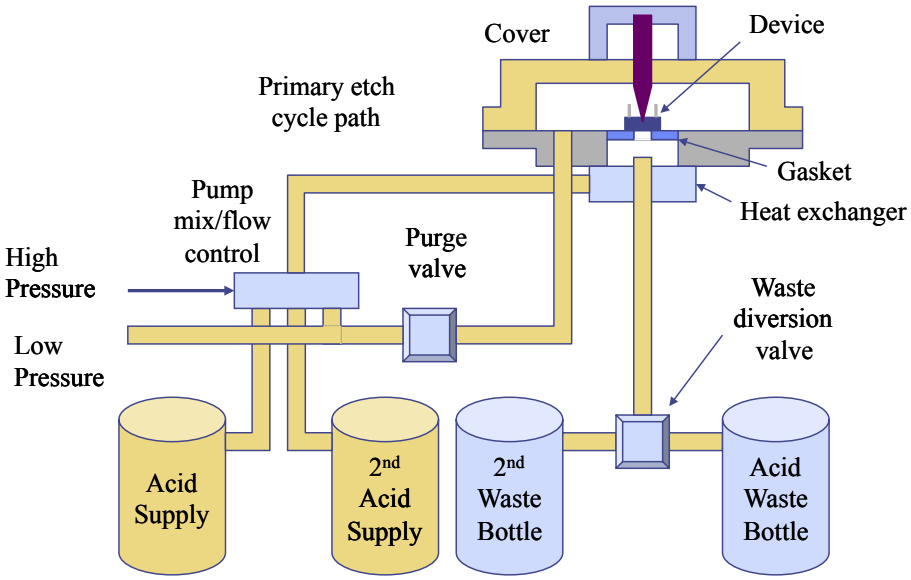


Figure 2. Plumbing system for an acid decapsulation system.

Here is an example of the results of a Jet Etch machine. The image on the right is an SEM image of a portion of the die surface, bond wires, and mold compound after a Jet Etch. If performed properly, a Jet Etch should leave the device electrically intact, with little or no corrosion. There should also be no damage to the die. Most problems occur when a second etch is performed without thoroughly drying the part after the first etch. The moisture from the rinse after the first etch can react with the acid and exposed aluminum or copper, damaging the bond wires and bond pads. The Jet Etch can also quickly decapsulate a device. The process takes sixty seconds or less, and therefore, causes limited exposure to heat and alteration of failure mechanisms sensitive to heat, such as charge buildup in the oxides.

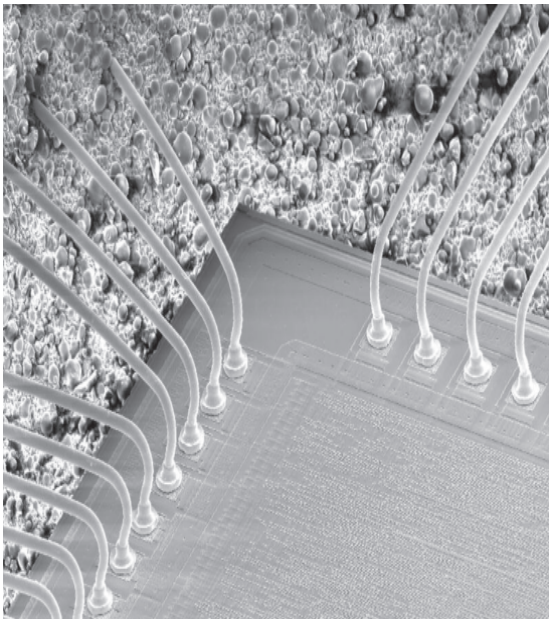


Figure 3. SEM image showing the results of a decapsulation operation.

The Jet Etch system can be used on a wide variety of different package types. Figure 4 shows some of the different package types that can be opened with a Jet Etch system. Analysts control the size of the opening by gaskets they place on top of the package to limit the extent of the acid interaction.

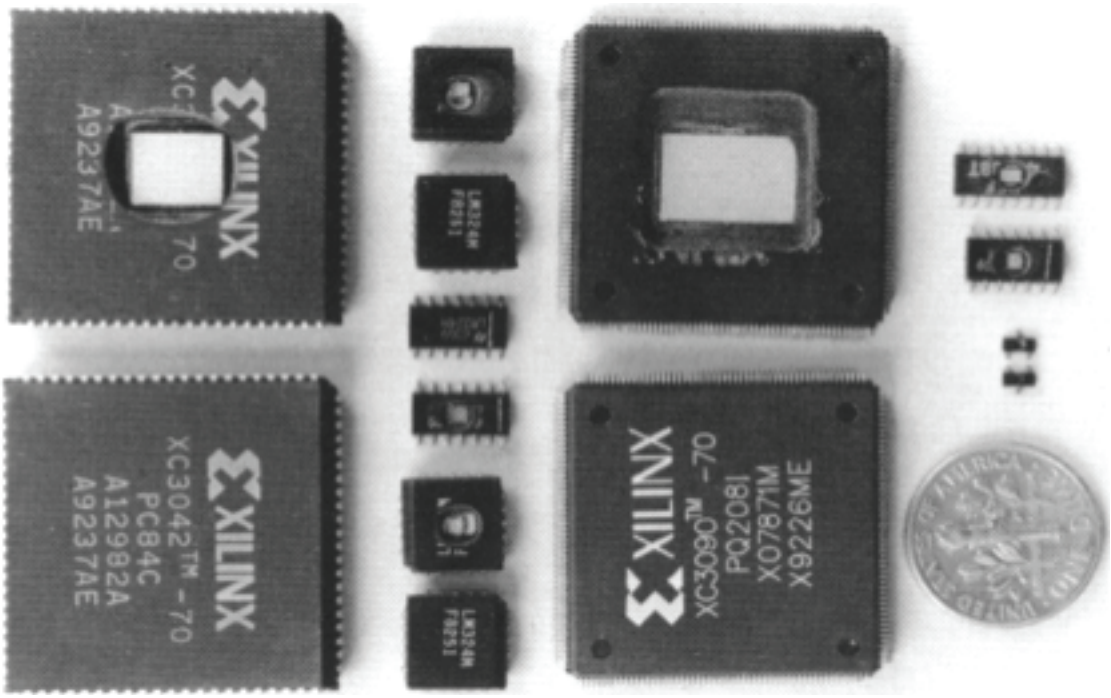


Figure 4. Examples of circuits decapsulated using a Jet Etch system.

Many of today's power semiconductor components, microprocessors, and ASICs reside on large dice. These dice occupy a disproportionately large part of the overall package volume. As such, the Jet Etch process can easily overetch the package sidewall, causing acid to leak out into the Jet Etch machinery and further damage to the package. Large die often require additional support or initial milling to preserve the package and its electrical integrity.

If you want to learn more about these techniques, including how to deal with newer materials like copper wire, consider enrolling in our Online Training System. We cover this topic in more detail, as well as dozens of other topics in failure analysis and reliability. You can learn more about this system on our web site (http://www.semitracks.com/index.php/online-training).

Technical Tidbit

Low Emission Packaging Materials

An increasing problem with modern ICs is their susceptibility to soft errors. A soft error can be caused by an alpha particle striking a sensitive region on a circuit, like a memory cell or register, creating a temporary logical error in the circuit. Alpha particles can come from a variety of sources, but those sources need to be in close proximity to the active transistors in order for the alpha particles to create the charge necessary to cause an error. A leading cause of alpha particles that cause this problem is contamination in the solder bumps and plating materials used to connect the die to the package leadframe or substrate. In order to minimize this problem, some manufacturers have turned to "Low alpha" or "Low emission" materials. Basically, a Low alpha material is a material that has undergone more extensive purification to reduce the contamination level of radioactive elements. These images show examples of some of the materials for which engineers create low emission variants.

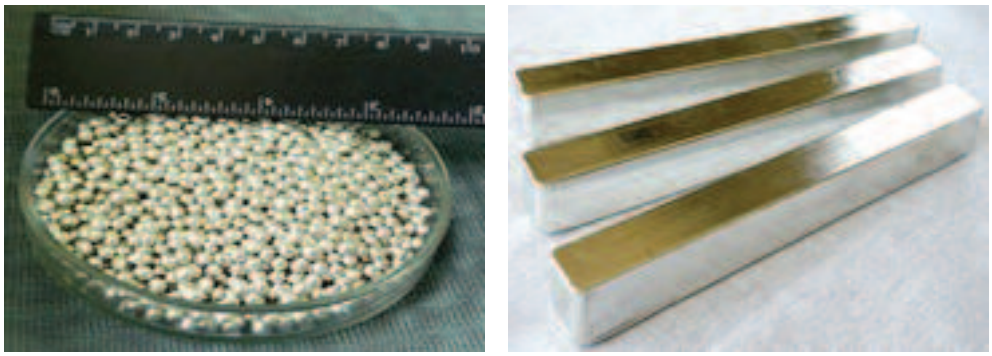


Figure 1. Low alpha tin spheres (left), and low alpha tin-copper (right)

Figure 2. Low alpha tin oxide powder (left), and low alpha tin pellets (right)

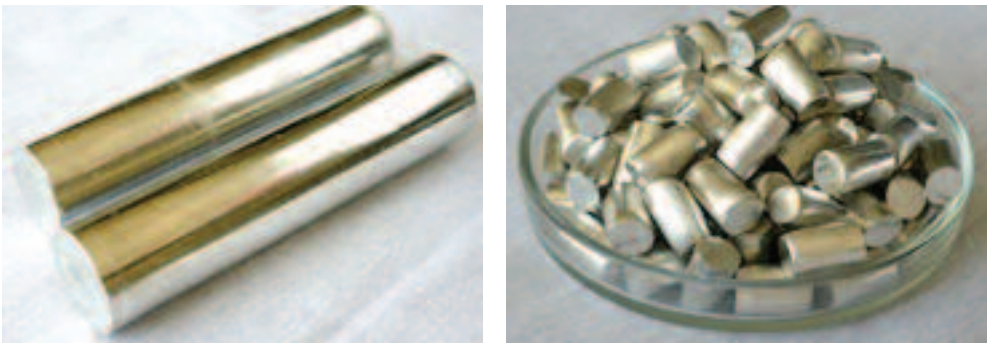


Figure 3. Low alpha lead – 4N purity (left), and low alpha lead pellets (right)

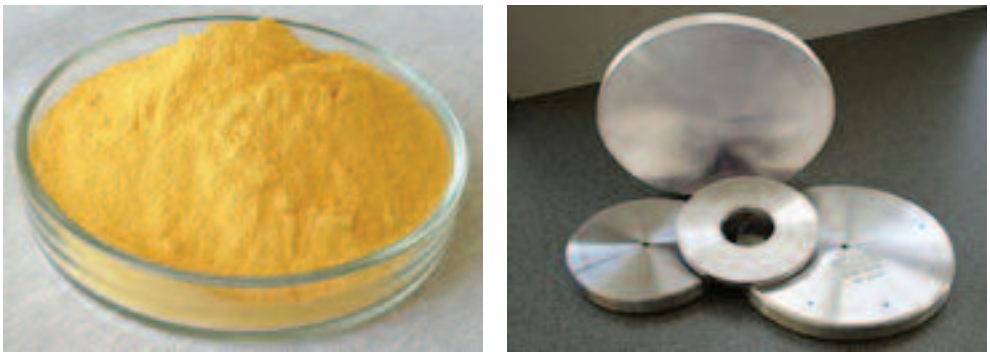


Figure 4. Low alpha lead oxide powder (left), and low alpha anodes (right)

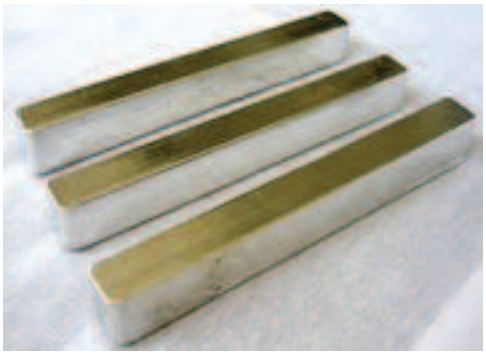


Figure 5. Low alpha tin-silver-copper (images courtesy CSC Pure Technologies)

While not all applications require this care with materials, systems that must operate without errors, or systems with large amounts of memory, can require these materials to avoid potential problems.

Ask the Experts

Q: Will SOI be the path forward for continued CMOS scaling?

A: This is a highly complex question and the source of a lot of debate within the industry. Currently, the thinking is that FinFET technology provides a better path forward because the fin structure permits better channel electrostatic control. However, Fully Depleted SOI (FDSOI) is a less complex process, and would provide a platform for other advances, like Monolithic 3D integration and Silicon Photonics. SOI uses a more expensive substrate, so cost-sensitive applications may not be able to go this route. Stay tuned over the next several years to see how this will play out.

Spotlight: Process Integration Short Course

Our CMOS, BiCMOS and Bipolar Process Integration Course is scheduled for March 25 – 26 in Austin, Texas. We don't offer this course publicly very often, so now is your opportunity to attend it. For further information, please visit the website (http://tinyurl.com/semi1401)

OVERVIEW

Semiconductor and integrated circuit developments continue to proceed at an incredible pace. For example, today's microprocessor chips have one thousand times the processing power of those a decade ago. These challenges have been accomplished because of the integrated circuit industry's ability to track something known as Moore's Law. Moore's Law states that an integrated circuit's processing power will double every two years. This has been accomplished by making devices smaller and smaller. The question looming in everyone's mind is "How far into the future can this continue?" ***CMOS and BiCMOS Process Integration*** is a five-day course that offers detailed instruction on the physics behind the operation of a modern integrated circuit, and the processing technologies required to make them. We place special emphasis on current issues related to designing and manufacturing the next generation devices. This course is a must for every manager, engineer and technician working in the semiconductor industry, using semiconductor components or supplying tools to the industry.

By focusing on the fundamentals of transistor operation and interconnect performance, participants will learn why advances in the industry are occurring along certain lines and not others. Our instructors work hard to explain how semiconductor devices work without delving heavily into the complex physics and mathematical expressions that normally accompany this discipline.

Participants learn basic but powerful aspects about the semiconductor industry. This skill-building series is divided into four segments:

1. **Basic Device Operation.** Participants learn the fundamentals of transistor operation. They learn why CMOS (Complimentary Metal Oxide Semiconductor) devices dominate the industry today
2. **Fabrication Technologies.** Participants learn the fundamental manufacturing technologies that are used to make modern integrated circuits. They learn the typical CMOS and BiCMOS process flows used in integrated circuit fabrication.
3. **Current Issues in Process Integration.** Participants learn how device operation is increasingly constrained by three parameters. They also learn about the impact of using new materials in the fabrication process and how those materials may create problems for the manufacturers in the future.
4. **An Overview of Issues Related to Process Integration.** Participants learn about the image of new materials, yield, reliability and scaling on technology and process integration. They receive an overview of the major reliability mechanisms that affect silicon ICs today.

COURSE OBJECTIVES

1. The seminar will provide participants with an in-depth understanding of the semiconductor industry and its technical issues.
2. Participants will understand the basic concepts behind transistor operation and performance.
3. The seminar will identify the key issues related to the continued growth of the semiconductor industry.
4. The seminar offers a wide variety of sample problems that participants work to help them gain knowledge of the fundamentals of device operation and manufacturing.
5. Participants will be able to identify basic and advanced technology features on semiconductor devices. This includes features like silicon-germanium, strained silicon, copper, and low-k dielectrics.
6. Participants will understand how reliability, power consumption and device performance are interrelated.
7. Participants will be able to make decisions about how to construct and evaluate new CMOS, BiCMOS, and bipolar technologies.

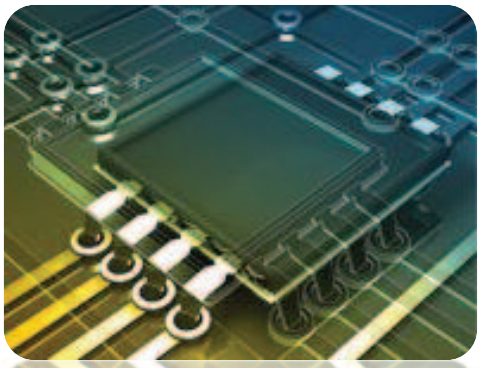
INSTRUCTIONAL STRATEGY

By using a combination of instruction by lecture, classroom exercises, and question/answer sessions, participants will learn practical information on semiconductor devices and the operation of this industry. From the very first moments of the seminar until the last sentence of the training, the driving instructional factor is **application**. We use instructors who are internationally recognized experts in their fields that have years of experience (both current and relevant) in this field. The handbook offers hundreds of pages of additional reference material the participants can use back at their daily activities.

COURSE OUTLINE

1. Introduction
2. Conventional CMOS
   a. Key Components and Parameters
   b. Process Overview and Integration Issues
   c. Scaling and Limitations
3. Mobility Enhancement Techniques
   a. Strained Silicon
   b. Crystal Orientation
4. Gate Stacks, High-k Dielectrics
   a. Gate Conductor Materials and Properties
   b. High-k Materials and Properties
   c. Gate Stack Integration

5. Options for Source-Drain, Extensions
   a. Elevated Source/Drain
   b. Co-Implantation of Inactive Species
   c. Schottky-Barrier Source-Drain
6. Three-Dimensional Structures
   a. FinFETs, Multi-Gates
7. Interconnects
   a. Aluminum Interconnects, Issues
   b. Copper Interconnects, Issues
   c. Low-k Dielectrics
8. Conventional BiCMOS
   a. Bipolar Transistor Fundamentals
   b. BiCMOS Process Overview
   c. Scaling and Limitations
9. Bipolar Enhancement Techniques
   a. SiGe
   b. SiGe:C
10. CMOS/BiCMOS Reliability Considerations
    a. Electrostatic Discharge
    b. Electromigration and Stress Migration
    c. Soft Errors, Plasma Damage
    d. Dielectric Reliability
    e. Bias Temperature Instabilities
    f. Hot Carrier Reliability
    g. Burn-In
11. Yield Considerations
    a. Yield Detractors
    b. Models
    c. Monitors



Upcoming Courses

(Click on each item for details)

ESD Design and Technology
February 11 – 13, 2014 (Tue – Thur)
San Jose, California, USA

Semiconductor Reliability
February 11 – 13, 2014 (Tues – Thur)
San Jose, California, USA

Failure and Yield Analysis
February 17 – 20, 2014 (Mon – Thur)
San Jose, California, USA

Wafer Fab Processing
February 18, 2014 (Tue)
San Jose, California, USA

Fault Isolation
March 5 – 7, 2014 (Wed – Fri)
Penang, Malasia

Fault Isolation
March 10 – 12, 2014 (Mon – Wed)
Singapore

CMOS, BICMOS and Bipolar Process Integraion
March 25 – 26, 2014 (Tue – Wed)
Austin, Texas, USA

Feedback

If you have a suggestion or a comment regarding our courses, online training, discussion forums, or reference materials, or if you wish to suggest a new course or location, please call us at 1-505-858-0454 or Email us (info@semitracks.com).
To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered in the next newsletter, please contact Jeremy Henderson by Email (jeremy.henderson@semitracks.com).
We are always looking for ways to enhance our courses and educational materials.
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http://www.semitracks.com

To post, read, or answer a question, visit our forums.
We look forward to hearing from you!