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YOUR MONTHLY LOOK INSIDE SEMICONDUCTOR TECHNOLOGY

Semiconductor Cleanroom Technology

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In this month's Feature Article, we will continue our discussion of Cleanroom Technology. This article discusses how personnel in the fab contribute to contamination, and how to mitigate the problem.

A major contaminant issue in the fab environment are the people who work in the fab. The contaminants that most impact wafer yield include particulates from skin, hair, clothing, and smoking. It also includes alkali metals like sodium and potassium from skin oils, road salt and other sources. Metals in cosmetics can impact wafer yield, as can trace contaminants from the worker's breath. The main strategy to reduce this problem is to cover the workers from head to toe to contain the contaminants. Figure 1 shows an example of this coverage. It typically includes a body suit, boots, a face mask, gloves, and safety glasses. In some instances, workers even use respirators with filters for breathing. The fabric is a non-shedding, dense-weave polyester or Gore-Tex fabric. This clothing is cleaned after each use and re-packaged to prevent contamination. Particle-free clothing is not sufficient in and of itself, so we need proper procedures to take it on and off to avoid workers getting contamination onto the outside of their clothing while dressing. Proper clean room design is also important, so the changing area must be designed in such a way as to minimize contamination transfer.

WHAT'S INSIDE?

01 Feature Article

06 Technical Tidbit

08 Ask The Experts

09 Course Spotlight

Want to take control of your learning? See page 08

Upcoming Courses:

- Wafer Fab Processing
- Failure and Yield Analysis

See page 13 for more details

Figure 1- Example of cleanroom body suit.

We will cover a typical list for a Cleanroom Gowning Procedure. This list incorporates the current best practices.

First, we will discuss the Pre- Gowning steps. We prepare for cleanroom gowning by:

- Removing jewelry, makeup, heavy coats, sweatshirts, and other "extra" items
- Checking that the tacky mat is fresh; if not, slowly pull it up toward the center and replace it with a clean tacky mat
- Stepping on the tacky mat three times, rotating to ensure your entire shoe contacts the mat
- Once inside the room, prepare all the materials you'll need.

Now, let’s show the main Cleanroom Gowning steps. As you gown, you take a "top-down" approach, starting at your head and working your way down.

1. Put on a cap and beard cover.
2. Check to make sure all of your hair is covered.
3. Select, inspect, clean, and then put on safety glasses or goggles.
4. Put on the first layer of gloves. This set of gloves is considered to be your "gowning gloves" set.
5. Put on a coverall gown.
6. Ensure that the gown never touches the floor by gathering leg and arm cuffs and then releasing them one at a time.
7. If a separate hood is part of the gown, tuck the shoulder panels inside and under the gown before you zip it up.
8. Put on shoe covers one at a time as you step over the line or bench. Note: Take extreme care to avoid contaminating the room's clean side with any contact from the dirty side.
9. Put on the second pair of gloves over the first and stretch them over the gown sleeve cuffs.

You’re now ready to enter the cleanroom, but first, follow these steps:

1. Use hand sanitizer or another cleaning agent approved by your employer.
2. Enter the air shower and use it until it turns off, making sure to turn so the air can get to every spot.
3. Finally, enter the cleanroom.

Next, let’s share the cleanroom protocol for the Cleanroom De-gowning Procedure. This list also incorporates the current best practices.

1. Remove your boot or shoe covers. If they are to be used again, store them in the designated container or bag.
2. If you're wearing two sets of gloves, discard the outer pair. Otherwise, remove your gloves last.
3. De-gown by removing the coverall gown. Hang it in the approved area or discard it.
4. Remove your eyewear and place it in the proper storage container.
5. Remove your hood and place it in an approved area, or discard.
6. Exit the gowning room and enter the antechamber.
7. Remove and discard your face mask.
8. Remove and discard your cap.
9. Remove and discard your inner pair of gloves.
10. Finally, place the disposable items and recyclable items into the appropriate receptacles.

Finally, let's discuss moving equipment and materials into the cleanroom. Multiple cleanroom bags are used to protect materials as they transition into the clean area. For multiple-level classification areas, a single outer bag is removed at each step. Once the item reaches the final destination, the final bag should be removed. This method reduces the likelihood that contaminants from lower-level classifications areas will be tracked into the processing area.

The disinfection method requires spraying or wiping materials and/or packaging materials with a suitable disinfectant before they are transferred to the final processing area. Benefits of this method include greater control of disinfectants used and the amount dispensed. Typically, the materials are wiped using traditional cleanroom wiping techniques – wiping in one direction using parallel, overlapping strokes starting from the cleanest area and wiping towards the least clean area. It should be noted that some cleanroom procedures implement the disinfection method in addition to the multiple bag method. We show examples of the cleanroom bags and disinfectant spray below in Figure 2.

Figure 2- Cleanroom bags and disinfectant spray

Pass Through Boxes, or PTBs, can also be seen in many applications. The use of them and the required dimensions and volume largely depend on the scale of the operation the cleanroom is used for. The use can generally be categorized in terms of inbound or outbound. Inbound transfers typically include: Contained supplies (process materials, media, process utensils, environmental monitoring (EM) materials, cleaning materials and agents). Outbound transfers typically include: partially fabricated products, product samples, EM samples, used instruments, product and utensils packaging waste, cleaning waste. We show an example of the PTB in Figure 3.

Figure 3- Example of a Pass-Through Box (PTB).

In conclusion, we briefly discussed access considerations. All fab personnel require protection to gain access, primarily to protect the cleanroom environment from particulate matter accompanying the personnel. Cleanrooms require controlled access, so as not to permit unauthorized personnel into the cleanroom, and to minimize particle intrusion due to unfavorable airflow conditions. Cleanrooms are pressurized, and access occurs through airlocks to minimize the intrusion of particles. Proper gown procedures are critical, as are proper procedures to move equipment and materials either into or out of the cleanroom.

In next month's Feature Article, we will continue our discussion of semiconductor cleanroom technology and introduce the topic of automated material handling systems.

Technical Tidbit: Direct Copper Bonding

The movement of semiconductor packaging into 3D Heterogeneous Integration requires a number of new processes and technologies. In this month's Technical Tidbit, we will focus on one of those new processes – direct copper bonding. The idea behind direct copper bonding is to reduce resistance, inductance and capacitance between chips, or between a chip and a wafer, or between a chip and a substrate, so that the product can operate with better performance and lower power dissipation. In order to create direct copper bonding, first, one creates a copper bump structure on the surface of the chip. This would typically be done at the wafer-level in a bump facility. The technique for creating the copper bump is the same as creating a copper pillar structure – electroplating the copper to build up the structure. Unlike a typical solder bump, the copper bump must have a flat surface on the top, so that one can create a high-quality connection to another die or wafer with the same copper bump structure. Next, after the bumps are formed on the die or wafer, the surface would be covered with an underfill, like we show at the upper left of Figure 1. Next, one would cut or polish the underfill polymer and the copper bumps to create a flat surface. The two materials, the underfill polymer and copper bumps, can be cut or polished simultaneously. One would then bond the die or wafer to another wafer. The underfill will help provide mechanical strength to the connections, by first, providing rigidity in case of shock to the completed package, and second, by providing a compressive stress to the copper bond. After the underfill is cured, it shrinks back at a faster rate than the copper does, since it has a higher coefficient of thermal expansion. This places the copper bond into a compressive stress, and completes the direct copper bonding process.

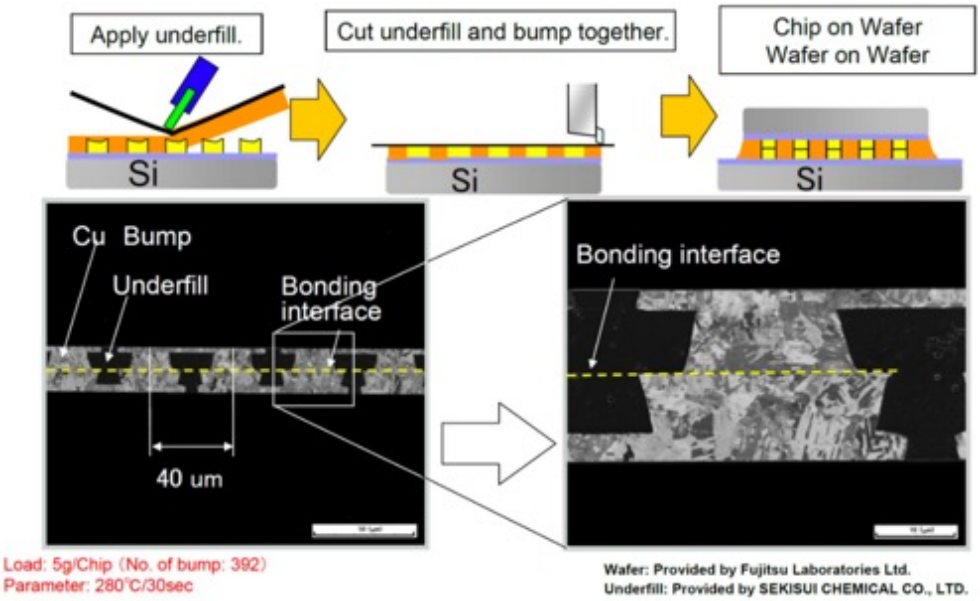

Figure 1- Transmission Electron Microscope (TEM) images of a direct copper bond.

In order for this process to work, we need a flat copper surface. The electroplating process to create the copper pad does not create a completely flat surface, so one would use Chemical Mechanical Polishing to create a flat copper surface. Next, we want to minimize bond temperature and stress. If the stress is too high, then delamination may result. Third, we also require clean copper surfaces, so the die and the wafers or substrates must be cleaned with a plasma etch. The plasma etch will use ammonium hydroxide to remove oxidation from the surface. After polishing and cleaning, the die can be placed on the wafer or substrate, using a standard pick-and-place tool, creating the 3D Heterogenous Integration structure. Lateral alignment must be better than 1 micron. One version of this process being marketed to the industry is DBI®, or Direct Bond Interconnect. DBI®is a trademarked approach that Ziptronix uses.

Ask The Experts

Q: How is the depth of a plasma/reactive ion etch controlled? Do engineers use visual inspection or metrology techniques?

A: The depth of a plasma or reactive ion etch is primarily controlled through understanding the etch rate. During the technology development phase, process engineers will characterize the etch rate on the layers that require etching. This will allow them to then predict how much material will be removed in a given amount of time. However, the depth of an etch may need to be controlled more tightly than one can achieve with a general predictive formula. Therefore, during the technology development phase, process integration engineers will commonly add an etch stop layer beneath the layer to be etched. An etch stop layer is a layer that etches at a much slow rate than the overlying layer, making it possible for the etch process to entirely remove the layer without significant removal of the underlying layer or layers. Process engineers may use visual inspection or metrology after the etch process to characterize the results, but mainly for the purpose of feedback to the process engineers, rather than real-time feedback to the etch process.

Course Spotlight: Fundamentals of High-Volume Production Test

OVERVIEW

During a semiconductor product life cycle, there is a launch into high volume production test that provides sufficient test coverage to meet customer requirements, yet still meet cost targets. Design and test are closely linked, and there is a push to always implement test during the design process to determine what can be designed into the chip to fit seamlessly with test flows/outcomes. Products are typically guaranteed to meet performance in terms of design for testability, test coverage, and operational conditions such as voltage, frequency, and temperature. Test engineers must select automated test equipment (ATE), along with wafer probers, and packaged part handlers that can meet these requirements. There are many nuances to wafer probers and handlers depending on the wafer type and the package. There may be additional requirements associated with production test, such as accelerated life testing (burn-in), and system-level test (SLT). Many applications require testing across temperature and thermal management of dissipated power. All product lifecycles need to include continuous improvements to the point of diminishing return. For production testing, engineers primarily focus their efforts to improve test through test cost reduction and higher test coverage. Furthermore, production testing generates extremely high volumes of data, so the key is how to harvest this data and reduce it to meaningful information for action. This is a 2-day course that offers engineers insight into the Fundamentals of High-Volume Production Test. We focus on the test development process, choosing automated test hardware, and the analysis of test data, to provide the engineer with key insights into the successful fielding of high-volume semiconductor components that work properly in the customers application with high levels of quality.

The course will cover the basic segments of today's high volume production test as found in Outsourced Assembly And Test contractors (OSATs), as well as internal Integrated Device Manufacturers (IDMs). Participants will learn basic, but powerful, aspects about the semiconductor industry. This skill-building series is divided into three segments:

1. **The Test Development Process.** Engineers learn how balance the need for test coverage with the time it takes to perform the testing. Often, these two goals are at odds with one another.

2. **Choosing Appropriate Test Hardware.** Test hardware (the ATE system, the handler or prober, and the interface boards) is expensive. Engineers need to choose the appropriate systems that meet the requirements for testing the semiconductor component without being too expensive.

3. **Analyzing Test Data.** Engineers can gain a wealth of insight into a semiconductor component's performance, quality and reliability by examining the test data. However, the amount of test data generated is enormous. We will discuss strategies for what information should be extracted from the test data to provide these insights.

COURSE OBJECTIVES

1. Participants will gain a greater understanding of their role in test development, the importance of test, and the link between design and design for test.

2. Participants will gain an understanding of how test goals can differ by application and market segment.

3. Participants will learn basic test elements and sequences used across the manufacturing process flow, which includes fab, bump, probe, and final test.

4. The course covers the different types of test and their outcomes, along with appropriate actions that a test engineer should take.

5. Participants will become familiar with the next steps after test.

6. The course provides an overview of various test systems, material handling, and connections between the component and the tester (known as "contact").

7. Participants will learn how to reduce test data to actionable information.

8. Participants will learn how test supports continuous improvement over the semiconductor component lifecycle.

9. The course covers the trends in test, as well as the future of test.

COURSE OUTLINE

DAY 1

1. Introduction
    a. Rationale
    b. Value Added and Non-value Added Aspects of Test
    c. Isolating Defective Parts
    d. Triggering Repair Algorithms
    e. Product Binning
    f. Test as a Complement to Statistical Process Control
    g. Oversight Over the Prior Operations (e.g., Wafer Fab and Assembly)
    h. Detection of Systemic Defects
    i. Design Aspects of Test: Design for Test (DFT), Design for Stress (DFS), Design for Diagnosability (DFD), Telemetry for In-field Aspects
    j. Test Program Creation (i.e., Automated Test Pattern Generation (ATPG))
    k. IEEE 1838 (e.g., Use of Standard for Chiplets)
    l. Linking System Level Test and ATE test

2. IC Applications / Device Types and Test
    a. Sensors/Actuators – MEMS and Stimuli
    b. RF - Conducted vs Radiated (e.g., Antenna in Package (AIP))
    c. Memory, Logic, Mixed Signal, Analog, RF, Power, Niches (e.g., SiC, GaN)
    d. Systems – On a Chip (SoC), On a Board (SoB), In a Package (SiP)

3. Basic Test Segments and Flows
    a. Fab Parametric In-line Tests
    b. Wafer Probe Test – Known Good Die (KGD) vs Known Tested Die (KTD)
    c. In Circuit Testing (ICT) (e.g., Bed of Nails)
    d. Final Test, System Level Test
    e. Pre/Post Burn-in and Test During Burn-in
    f. End of Line – Packing Media, Electrostatic Discharge (ESD), Moisture Sensitivity Level (MSL), Non-Volatile Memory Bakes and Subsequent Testing

4. Test Types, Information and Actions
    a. Scalar vs Vector
    b. Stress Testing
    c. Standard Digital Testing, Stuck At Fault (SAF) Testing, Quiescent Power Supply Current (IDDQ), Timing, Low Voltage Tests
    d. Shmoo Plots
    e. Other Test Visualization Maps
    f. Repair, Binning, Grading
    g. Temperature

DAY 2

5. Testers and Interface Hardware
    a. Testers – RF, Mixed-Signal, Analog, Power, Memory, Logic, SoC
    b. Rack and Stack, ATE, SLT, Hybrid
    c. Load boards

6. Probers, Handlers, Contactors
    a. Probers
        i. Standard
        ii. Film frame
        iii. Special variants
        iv. Prober interface boards
    b. Handlers
        i. Basic groups: Gravity, Turret, "Pick and Place"
            1. Corresponding Drivers
            2. Packages
        ii. System Level – Synchronous vs Asynchronous
        iii. Change Kits
        iv. Handler interface boards
        v. Assembly strips, Panel Level Processing (PLP)
        vi. Managing thermal (more on this in prober/handler section)

    c. Contactors
        i. Probe cards
            1. Standard PCB, Ceramic, Vertical probe cards, MEMS Microcantilever Probe Cards
        ii. Test Sockets
        iii. Importance of Maintenance and FPY (First Pass Yield)

7. Data, Analytics and Action
    a. Data Everywhere – Reducing it to Information for Action
    b. Analytics
        i. Outlier Detection and Algorithms
        ii. Adaptive Test
        iii. End to End - Unit Level Traceability (ULT)
    c. Actions to take
    d. Future trends

8. Putting It All Together – Product Lifecycle Management
    a. Lifecycle – New Production Introduction, Ramp-up, Continuous Improvement, Ramp-down
    b. Coverage/Refinement, Field Returns
    c. Test Time Reduction (TTR)
    d. Multi-site Testing – Finding the Sweet Spot
    e. Test Economics (e.g., Power of Depreciated Assets, Typical Cost and Pricing Factors)

9. Summary and Industry Test Challenges
    a. Summary
    b. Trends, Future Directions, Challenges
        i. Combating Silent Data Corruption (SDC) Behaviors and Root Cause; and Methods to Address
        ii. How to Increase Observability in Interconnections in Chiplet Designs
        iii. Physical Probing <10um pitch (e.g., hybrid bonding) and Alternatives
        iv. 3D Heterogeneous Integration and Its Impact on Test
        v. IEEE 1838 – Bridging Design and Test
        vi. UCIe and "Bunch of Wires"
        vii. Improving Unification Across ATE & SLT for Better Coverage
        viii. Future Uses of SLT and Its Advantages and Disadvantages

Upcoming Courses:

Public Course Schedule:

Wafer Fab Processing - February 26-29, 2024 (Mon.-Thurs.) | Munich, Germany - $2,095

Failure and Yield Analysis - March 4-7, 2024 (Mon.-Thurs.) | Munich, Germany - $2,095 until Mon. Feb. 12

Semiconductor Reliability and Product Qualification - March 11-14, 2024 (Mon.-Thurs.) | Munich, Germany - $2,095 until Mon. Feb. 19

Defect-Based Testing - March 20-21, 2024 (Wed.-Thurs.) | Munich, Germany - $1,195 until Wed. Feb. 28

Advanced CMOS/FinFET Fabrication - May 6-7, 2024 (Mon.-Tues.) | Phoenix, AZ - $995

Failure and Yield Analysis - May 13-16, 2024 (Mon.-Thurs.) | Phoenix, AZ - $2,095 until Mon. Apr. 22

Semiconductor Reliability and Product Qualification - May 20-23, 2024 (Mon.-Thurs.) | Phoenix, AZ - $2,095 until Mon. Apr. 29

Fundamentals of High-Volume Production Test - May 20-21, 2024 (Mon.-Tues.) | Phoenix, AZ - $1,195 until Mon. Apr. 29

Defect-Based Testing - November 18-19, 2024 (Mon.-Tues.) | Munich, Germany - $1,195 until Mon. Oct. 28

Wafer Fab Processing - November 25-28, 2024 (Mon.-Thurs.) | Munich, Germany -$2,095 until Mon. Nov. 4

Failure and Yield Analysis - December 2-5, 2024 (Mon.-Thurs.) | Munich, Germany - $2,095 until Mon. Nov. 11

Semiconductor Reliability and Product Qualification - December 9-12, 2024 (Mon.-Thurs.) | Munich, Germany - $2,095 until Mon. Nov. 18

Have an idea for a course? If you have a suggestion or a comment regarding our courses, online training, discussion forums, or reference materials, or if you wish to suggest a new course or location, please email us at info@semitracks.com

To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered, please contact Jeremy Henderson at jeremy.henderson@semitracks.com

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