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INFOTRACKS

YOUR MONTHLY LOOK INSIDE SEMICONDUCTOR TECHNOLOGY

Semiconductor Cleanroom Technology

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In last month's Feature Article, we continued our series on Cleanroom Technology by discussing the Heating, Ventilation and Air Conditioning aspect of Cleanroom Construction. In this Feature Article, we will continue our discussion on Cleanroom Technology by discussing Equipment Placement.

There are two main configurations for equipment placement – Ballroom and Bay-Chase. Figure 1 is an example of a ballroom arrangement in a cleanroom.

Figure 1- Picture showing a ballroom-style cleanroom nearing completion of construction.

This arrangement has the advantage of the most flexibility for equipment placement. It also works best when the manufacturer plans to use an automated material handling

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UPCOMING WEBINARS:

Semiconductor Reliability and Product Qualification

Wafer Fab Processing

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system. However, the equipment will also exhaust into the same cleanroom space, so greater care may be required to prevent hazardous chemical leaks from harming personnel and contaminating the cleanroom environment.

Figure 2 is an example of a bay-chase arrangement in a cleanroom. The bay portion of the cleanroom is shown on the left of the figure, and the chase portion of the cleanroom is shown on the right.

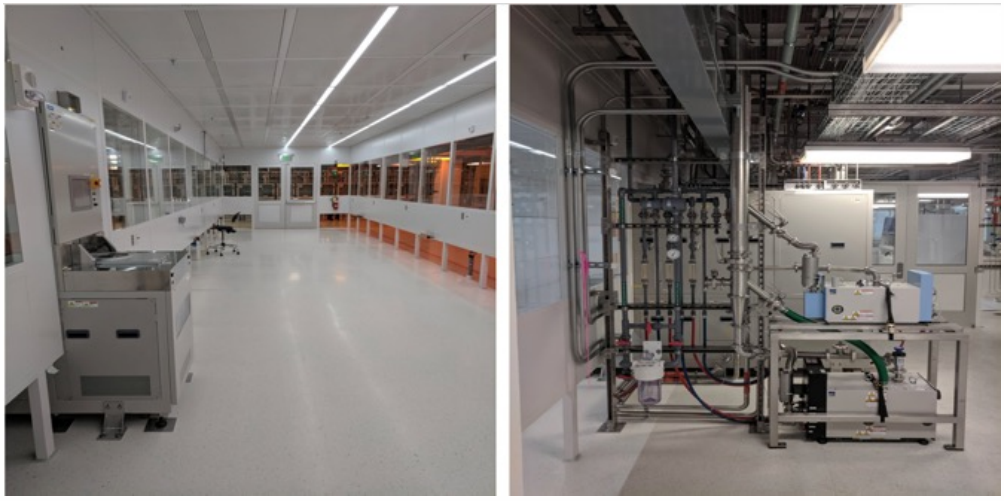

Figure 2- Cleanroom bay (left) and cleanroom chase (right) in a bay-chase configuration

This arrangement has the advantage of allowing the utilities to be plumbed in to the tool through a chase environment, making servicing tools easier and preventing harm to personnel easier to implement. However, the bay-chase arrangement does not provide as much flexibility for equipment placement, which we will discuss next.

In general, in a state-of-the-art fab, engineers try to place process tools in order to limit movement. Additional movement consumes time, so limiting movement is important. One can accomplish this by grouping module level tools together. For example, the gate stack module might consist of cleaning tools for the silicon surface; thermal oxidation furnaces for the gate oxide growth; and low-pressure chemical vapor deposition for the polysilicon gate. These tools might be grouped in a local area, or bay, to reduce movement. Another factor in equipment placement is lighting. For example, lithography requires specialized light to prevent the premature exposure of photoresist. Furthermore, vibration isolation is more important for some processes. Process steps like lithography and ion implantation require nanometer-level placement, so vibration must be tightly controlled. Finally, Chemical Mechanical Polishing, or CMP, must often be dealt with independently. Since it is a dirty process, the process tools for CMP are often placed away from other tools, since the process can run the risk of contaminating other tools.

Fabs have historically been laid out so that all of the copies of the same type of tool appear together. There are several advantages to this type of functional layout. First, process tools have historically been quite unreliable, so it is desirable for all copies of a tool to be grouped together so that the copies can back each other up. Second, there will be some tools that perform multiple steps. For example, 17 steppers may be used to perform 22 masking operations. The steppers are grouped together because it is impossible to have a one-to-one assignment of steppers to masking steps. Third, one operator may be able to run multiple tools (for example, furnaces) as long as these tools are close enough together that the operator can access any of the tools easily. Last, similar tools may share a common set of facility needs. Despite these advantages, there is a growing cost of functional layouts as well. Since functional layouts do not reflect the sequence in which the tools are used in the process recipe, lots may have to traverse long, complicated, overlapping paths through the fab as they move from process step to process step. This problem becomes more serious as the number of steps increases, and as lot transportation is automated. Factory modeling may be needed to evaluate different layout alternatives, such as a hybrid between functional layouts and a layout reflecting the process sequence. Figure 3 shows an example of a basic factory model to help understand the need for layout alternatives.

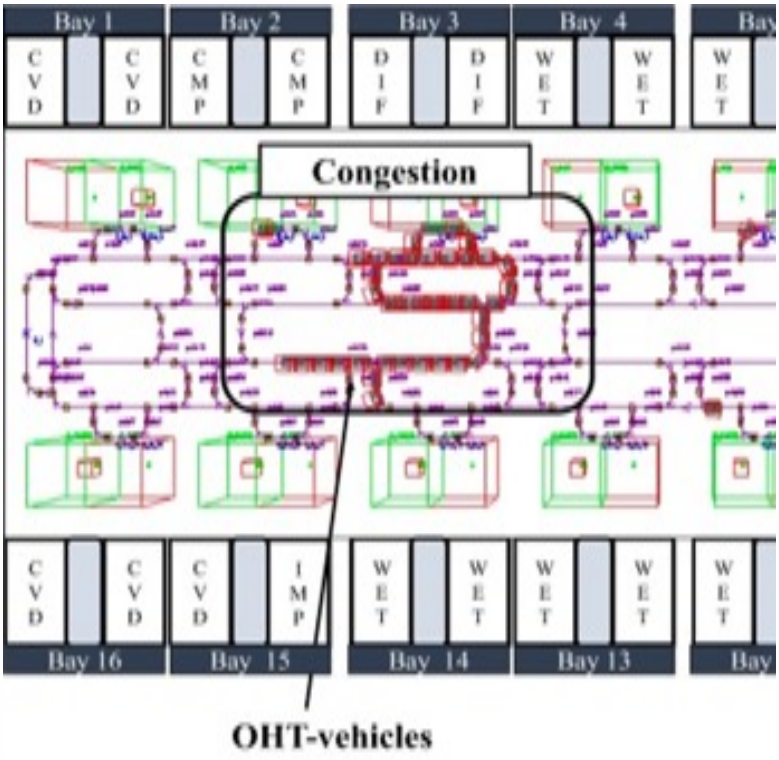

Figure 3- Basic factory model of a cleanroom showing congestion, which might be targeted as an opportunity to improve the workflow.

Another important component of a modern fab is the Automated Material Handling System, orAMHS. We show a diagram of such a system in Figure 4.

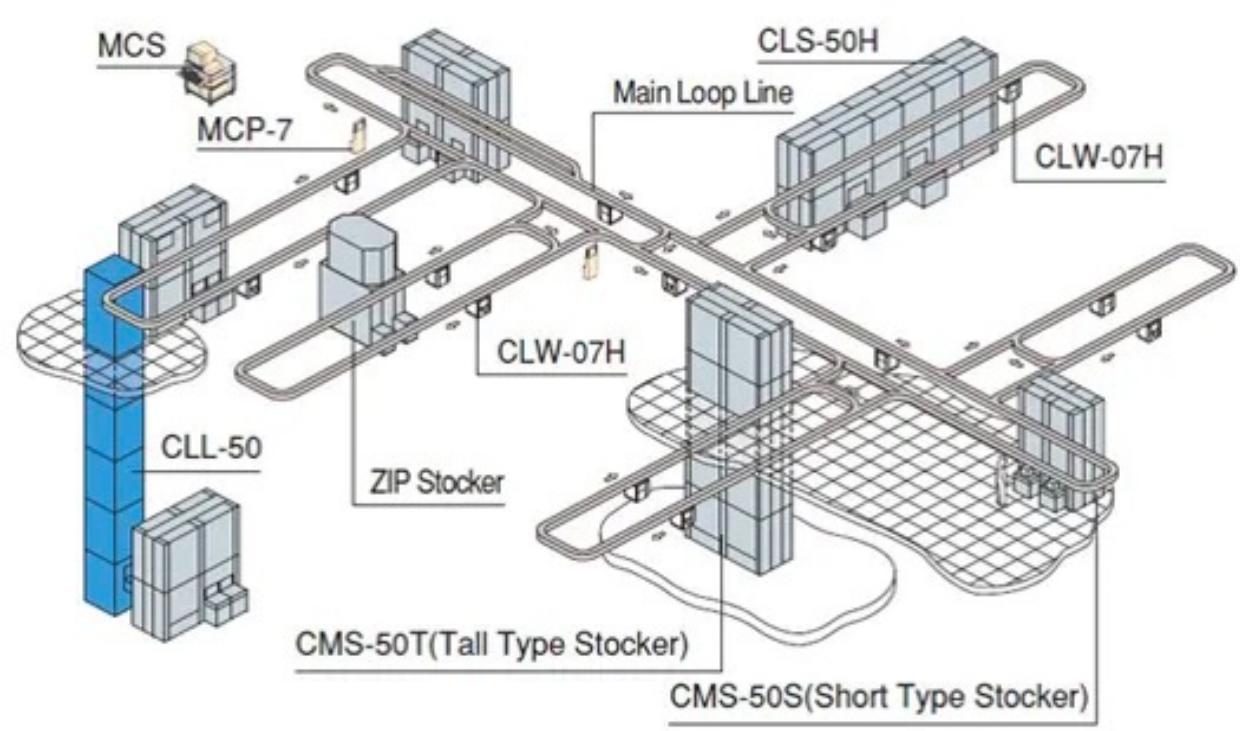

Figure 4- Diagram showing a schematic of an Automated Material Handling System, or AMHS

There are different types of AMHS implementations. These implementations can include one or more of the following systems: Automated Guidance Vehicles (AGVs), Rail Guided Vehicles (RGVs), Overhead Hoist Vehicle (OHV), and Overhead Transport (OHT) systems. AGV and RGV systems are more common in older 200mm fabs, while OHV and OHT systems are more common in 300mm fabs. In Figure 4, we show an example of an AMHS that contains both OHV and OHT systems. In conjunction with these systems in 300mm fabs, wafers are processed and transported in an enclosed container called a Front Opening Unified Pod (FOUP). A FOUP is transported from one set of equipment to another using an Overhead Hoist Transfer vehicle (OHT) system. The OHT travel rail can extend up to 10 kilometers with up to several hundred cars in large fabs, according to Daifuku, a major integrator of AMHS. To get everything working in unison, fabs use various factory automation technologies. Vendors also use Wafers In Process (WIP) flow techniques, such as real-time dispatching and scheduling, to coordinate the fab flow.

In conclusion, state-of-the-art high-volume cleanrooms are highly complex building projects, so considerable planning and preparation are necessary. Equipment placement and fab process goals play a key role in the construction of the fab. Since these construction projects are so complex, they are often classified as some of the most expensive construction projects when construction is underway. Just the shell of the building and cleanroom can run well in excess of $1Billion.

This concludes our discussion on Cleanroom Construction. In next month's Feature Article, we will continue our discussion on Cleanroom Technology with a focus on Power Usage in the Fab.

Technical Tidbit: PECVD Showerhead

This month's Technical Tidbit covers Plasma Enhanced Chemical Vapor Deposition (PECVD) Showerhead Issues. The showerhead is the component within the PECVD reactor that helps to spread the gases more uniformly throughout the chamber. Figure 1 shows an example of a PECVD showerhead.

Figure 1- Example of a PECVD Showerhead (image courtesy Entegris Technologies).

There are two major issues that process engineers must contend with: cleaning showerheads, and deposition on the showerhead, which can result in a phenomenon known colloquially to process engineers as "bright spots."

First, let's discuss cleaning issues. If a high pressure, high power clean process runs for too long, then the cleaning process itself can attack the showerhead, forming a brown film/powder on the showerhead. This can be removed either by a wet cleaning process or it can be removed through beadblasting. We will first discuss the basic process for the wet cleaning process. A typical wet clean interval would be after 500-1000µm of coating builds up on the showerhead. The basic steps are as follows:

1. Plasma clean the chamber to remove any oxide build-up. One should note that the intervals will be different for different systems and different applications.
2. Cool the electrodes to avoid the potential hazards associated with a hot surface
3. Examine the chamber – vacuum out any flakes/particles
4. Use an isopropyl alcohol (IPA) wipe to wipe of the chamber walls if necessary
5. Dry wipe the showerhead, or beadblast showerhead as a follow-on procedure, if necessary
6. Re-install showerhead; pump and purge the chamber; and then condition the chamber

Next, let's discuss the basic process for beadblasting. The basic steps are as follows:

1. Beadblast the surface of the showerhead using alumina powder (aluminium oxide beads) of 180 grit size or less. A typical grit size would be 120 grit for this activity. Do not use any solvents during the process.
2. Clean the showerhead after beadblasting using compressed air only.
3. Hold the showerhead up to the light to check that none of the holes are blocked by any grit from the beadblasting.
4. Clean out holes with paper clip or similar, if blocked.

If one chooses to remove the film or powder using beadblasting, one needs to ensure that the holes are clear by using compressed air and a 'paper clip' like object. There are coatings available that can reduce the intervals for cleaning.

The second issue we will discuss is known as showerhead 'bright spots.' Bright spots are small regions where the plasma glows more strongly because of constrictions or clogs in the showerhead. It is quite common to see PECVD showerhead holes become enlarged after a certain interval of use. This is caused by high-power processing (typically during plasma cleaning). Any holes which have slightly sharper edges will form an intense discharge over the hole, due to the high fields generated by the sharper edges. This can be seen as a 'bright spot' in the plasma located over the hole during the clean process. This can cause some erosion of the hole and widening of the hole opening, but only on the outlet side. Eventually, the bright spot will burn itself out, i.e., the erosion will remove the sharp edges and the bright spot will no longer occur at that hole. This may happen for several holes during the initial run-up of the system, until the showerhead 'stabilizes' itself. A bright spot may also result in some black/brown polymer deposition around the holes which can cause premature flaking of the deposited films. Equipment manufacturers typically recommend that the showerhead is bead-blasted to remove such residues. Once clean, the bright spots should not be observed during low power (<50W) deposition processes. If they are, it is recommended that the showerhead is plasma cleaned and bead-blasted until the bright spots are eliminated. It is sometimes possible to eliminate a bright spot by using a de-burring tool to clean out any machining residues from the hole in question. After that, if bright spots are still present then it may be necessary to obtain a replacement showerhead. The effect of the enlarged holes on the deposition results should be minimal, since they only enlarge the outlet of the hole, and they do not affect the gas flow.

For general reference on this topic, please see the article, "Basic PECVD Plasma Processes (SiH based)" by Oxford Instruments, published in 2003.

Ask The Experts

Q: Can you use a collimator in conjunction with an Ionized Physical Vapor Deposition (I-PVD) system?

A: Typically, one would not do this. The I-PVD system provides better control than a collimator would. Furthermore, the collimator would simply limit the deposition and eventually clog up if used in this manner, leading to the need to clean the collimator. In other words, there is no advantage to doing this, and there is the disadvantage of needing to do extra cleans.

Course Spotlight: FAILURE AND YIELD ANALYSIS

OVERVIEW

Failure and Yield Analysis is an increasingly difficult and complex process. Today, engineers are required to locate defects on complex integrated circuits. In many ways, this is akin to locating a needle in a haystack, where the needles get smaller and the haystack gets bigger every year. Engineers are required to understand a variety of disciplines in order to effectively perform failure analysis. This requires knowledge of subjects like: design, testing, technology, processing, materials science, chemistry, and even optics! Failed devices and low yields can lead to customer returns and idle manufacturing lines that can cost a company millions of dollars a day. Your industry needs competent analysts to help solve these problems. ***Failure and Yield Analysis*** is a 4 day course that offers detailed instruction on a variety of effective tools, as well as the overall process flow for locating and characterizing the defect responsible for the failure. This course is designed for every manager, engineer, and technician working in the semiconductor field, using semiconductor components or supplying tools to the industry.

By focusing on a ***Do It Right the First Time*** approach to the analysis, participants will learn the appropriate methodology to successfully locate defects, characterize them, and determine the root cause of failure. Participants learn to develop the skills to determine what tools and techniques should be applied, and when they should be applied. This skill-building series is divided into three segments:

1. The Process of Failure and Yield Analysis. Participants learn to recognize correct philosophical principles that lead to a successful analysis. This includes concepts like destructive vs. non-destructive techniques, fast techniques vs. brute force techniques, and correct verification.

2. The Tools and Techniques. Participants learn the strengths and weaknesses of a variety of tools used for analysis, including electrical testing techniques, package analysis tools, light emission, electron beam tools, optical beam tools, decapping and sample preparation, and surface science tools.

3. Case Histories. Participants identify how to use their knowledge through the case histories. They learn to identify key pieces of information that allow them to determine the possible cause of failure and how to proceed.

COURSE OBJECTIVES

1. The seminar will provide participants with an in-depth understanding of the tools, techniques and processes used in failure and yield analysis.

2. Participants will be able to determine how to proceed with a submitted request for analysis, ensuring that the analysis is done with the greatest probability of success.

3. The seminar will identify the advantages and disadvantages of a wide variety of tools and techniques that are used for failure and yield analysis.

4. The seminar offers a wide variety of video demonstrations of analysis techniques, so the analyst can get an understanding of the types of results they might expect to see with their equipment.

5. Participants will be able to identify basic technology features on semiconductor devices.

6. Participants will be able to identify a variety of different failure mechanisms and how they manifest themselves.

7. Participants will be able to identify appropriate tools to purchase when starting or expanding a laboratory.

INSTRUCTIONAL STRATEGY

By using a combination of instruction by lecture, video, and question/answer sessions, participants will learn practical approaches to the failure analysis process. From the very first moments of the seminar until the last sentence of the training, the driving instructional factor is **application**. We use instructors who are internationally recognized experts in their fields that have years of experience (both current and relevant) in this field. The handbook offers hundreds of pages of additional reference material the participants can use back at their daily activities.

THE SEMITRACKS ANALYSIS INSTRUCTIONAL VIDEOS™

One unique feature of this workshop is the video segments used to help train the students. Failure and Yield Analysis is a visual discipline. The ability to identify nuances and subtleties in images is critical to locating and understanding the defect. Many tools output video images that must be interpreted by analysts. No other course of this type uses this medium to help train the participants. These videos allow the analysts to directly compare material they learn in this course with real analysis work they do in their daily activities.

COURSE OUTLINE

1. Introduction
2. Failure Analysis Principles/Procedures
    a. Philosophy of Failure Analysis
    b. Flowcharts
3. Gathering Information
4. Package Level Testing
    a. Optical Microscopy
    b. Acoustic Microscopy
    c. X-Ray Radiography
    d. Hermetic Seal Testing
    e. Residual Gas Analysis
5. Electrical Testing
    a. Basics of Circuit Operation
    b. Curve Tracer/Parameter Analyzer Operation
    c. Quiescent Power Supply Current
    d. Parametric Tests (Input Leakage, Output voltage levels, Output current levels, etc.)
    e. Timing Tests (Propagation Delay, Rise/Fall Times, etc.)
    f. Automatic Test Equipment
    g. Basics of Digital Circuit Troubleshooting
    h. Basics of Analog Circuit Troubleshooting
6. Decapsulation/Backside Sample Preparation
    a. Mechanical Delidding Techniques
    b. Chemical Delidding Techniques
    c. Backside Sample Preparation Techniques
7. Die Inspection
    a. Optical Microscopy
    b. Scanning Electron Microscopy
8. Photon Emission Microscopy
    a. Mechanisms for Photon Emission
    b. Instrumentation
    c. Frontside
    d. Backside
    e. Interpretation
9. Electron Beam Tools
    a. Voltage Contrast
        i. Passive Voltage Contrast
        ii. Static Voltage Contrast
        iii. Capacitive Coupled Voltage Contrast
        iv. Introduction to Electron Beam Probing
    b. Electron Beam Induced Current
    c. Resistive Contrast Imaging
    d. Charge-Induced Voltage Alteration
10. Optical Beam Tools
    a. Optical Beam Induced Current
    b. Light-Induced Voltage Alteration
    c. Thermally-Induced Voltage Alteration
    d. Seebeck Effect Imaging
    e. Electro-optical Probing
11. Thermal Detection Techniques
    a. Infrared Thermal Imaging
    b. Liquid Crystal Hot Spot Detection
    c. Fluorescent Microthermal Imaging
12. Chemical Unlayering
    a. Wet Chemical Etching
    b. Reactive Ion Etching
    c. Parallel Polishing
13. Analytical Techniques
    a. TEM
    b. SIMS
    c. Auger
    d. ESCA/XPS
14. Focused Ion Beam Technology
    a. Physics of Operation
    b. Instrumentation
    c. Examples
    d. Gas-Assisted Etching
    e. Insulator Deposition
    f. Electrical Circuit Effects
15. Case Histories

Upcoming Courses:

EOS, ESD and How to Differentiate - March 6-7, 2023 (Mon.-Tues.) | Munich, Germany

Semiconductor Reliability and Product Qualification - March 13-16, 2023 (Mon.-Thurs.) | Munich, Germany

Wafer Fab Processing - March 13-16, 2023 (Mon.-Thurs.) | Munich, Germany

Failure and Yield Analysis - March 20-23, 2023 (Mon.-Thurs.) | Munich, Germany

Failure and Yield Analysis - May 1-4, 2023 (Mon.-Thurs.) | Oro Valley, Arizona

Semiconductor Reliability and Product Qualification - May 8-11, 2023 (Mon.-Thurs.) | Oro Valley, Arizona

Have an idea for a course? If you have a suggestion or a comment regarding our courses, online training, discussion forums, or reference materials, or if you wish to suggest a new course or location, please email us at info@semitracks.com

To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered, please contact Jeremy Henderson at jeremy.henderson@semitracks.com

We are always looking for ways to enhance our courses and educational materials and look forward to hearing from you!