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Applications Overview Part 2

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In this document, we complete our coverage of some of the applications for optoelectronics circuits.

We cover the outline for this section here. In Part 1 we briefly discussed CCD image detectors, photomultipliers, x-ray detectors, and plasmonic devices. In Part 2 we will briefly discuss quantum dot devices, terahertz applications, and optical MEMS devices.

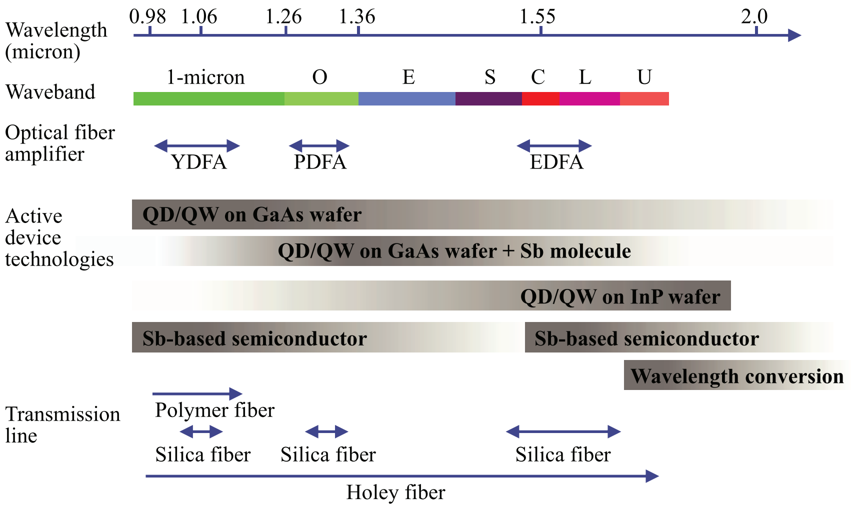

Figure 10. Quantum dot devices: operating wavelengths.

This chart in Figure 10 shows the operating wavelengths for quantum dot devices. Depending on the type of transmission line

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shown at the bottom, different semiconductor materials can be used to create the quantum dot structures.

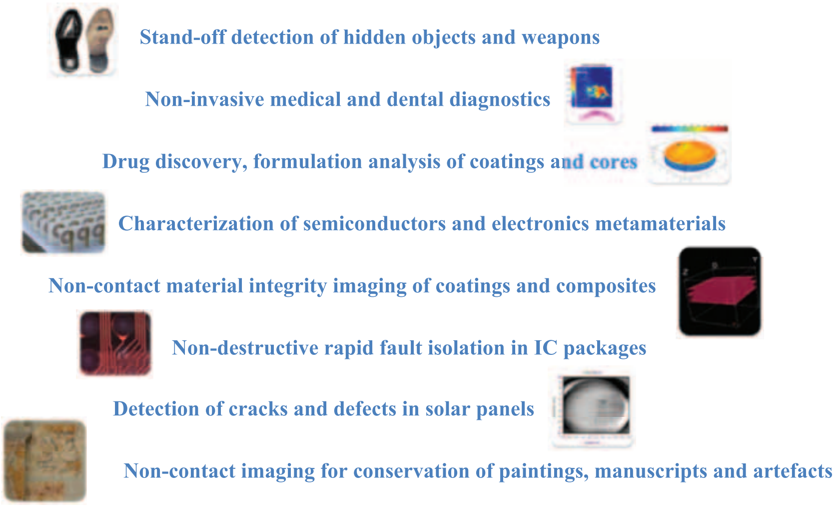

Figure 11. Terahertz applications examples.

Another set of applications in optoelectronics are those that involve terahertz frequencies. We show some applications here in Figure 11. They can range from stand-off detection of hidden objects and weapons, to drug discovery, to non-destructive fault isolation in semiconductor packages, to non-contact imaging for preservation of ancient relics, paintings, manuscripts and other artefacts.

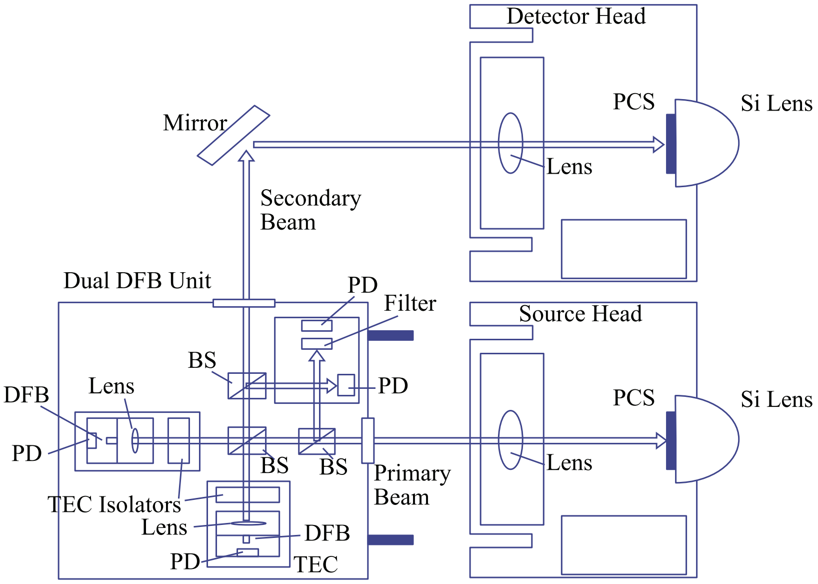

Figure 12. Diagram of Emcore's terahertz spectrometer.

Here in Figure 12 we show the diagram of a terahertz spectrometer from Emcore. At the right are the detector and source heads. Both contain photoconductive switches and lenses. The Dual Distributed

Feedback, or DFB unit contains two laser-diode chips mounted on independent Peltier thermoelectric coolers. This system allows for indirect frequency measurement. Direct measurement of the terahertz frequency is not practical due to the extremely high frequencies involved and the lack of commercial diagnostic tools.

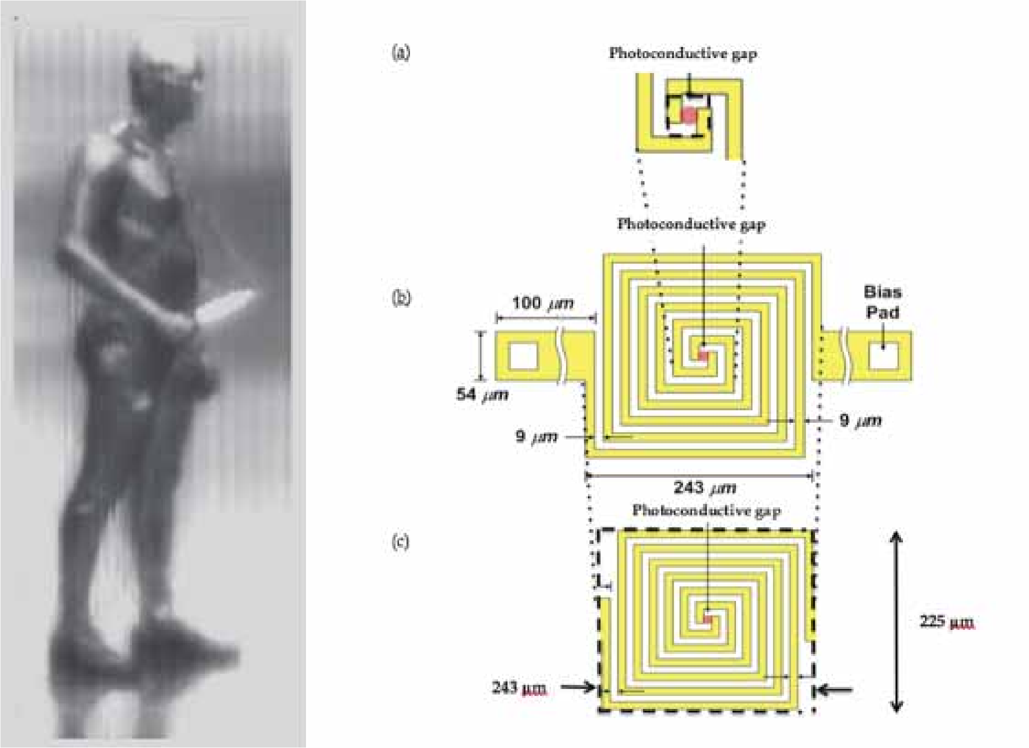

Figure 13. Illustration of Auston photoconductive switch.

Another terahertz imaging component is the Auston photoconductive switch. We show a diagram of the device on the right in Figure 13. The device uses a photoconductive gap. In this configuration, the gap is 9 microns. There are two interleaved spiral tracks leading to two bias pads. One can use the bias to allow light through, or to stop the light propagation. On the left we show a terahertz image generated in part by the switch.

Another set of optoelectronics applications are photonic integrated circuits. These ICs have multiple optical devices monolithically integrated onto a single substrate. The photonic integrated circuit can be used to guide optical signals, amplification, and logic functions. In particular, one might use the PIC to allow light to turn a sharp corner, which is difficult to accomplish with other techniques. Photonic ICs have several potential advantages over electronic ICs, which include higher processing speeds, less crosstalk, and potentially novel applications using optics that might not be possible with electronic signals.

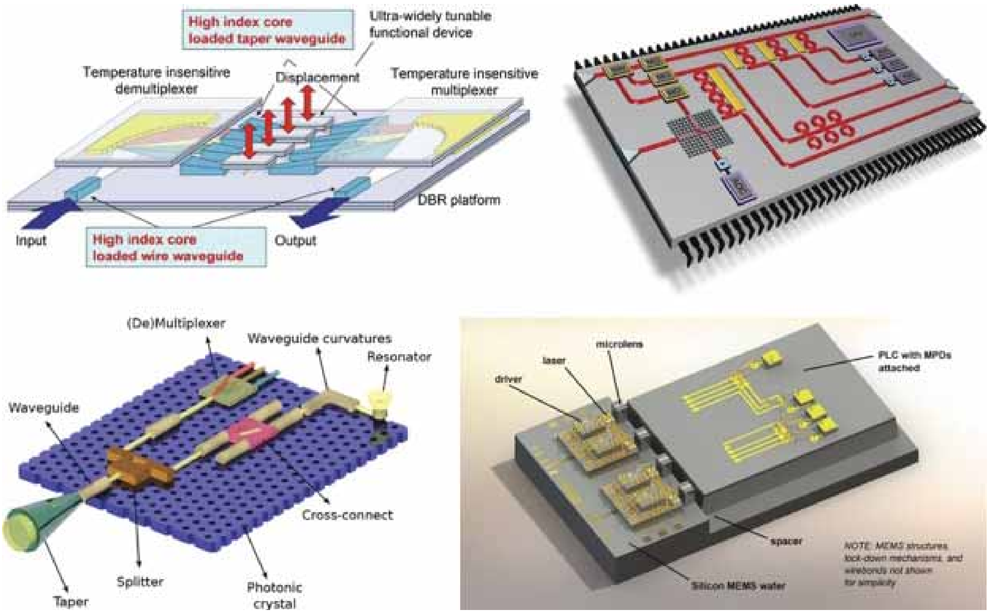

Figure 14. Examples of photonic integration.

The main advantage of Photonic Integrated Circuits is of course, integration. We show several examples of photonic integration here in Figure 14. The figure at the upper left is a Distributed Bragg Reflector platform, and the figure on the lower right is a Planar Lightwave Circuit with Monitor Photodiodes. Some Photonic Integrated Circuits may also contain Microelectromechanical, or MEMS, structures as well.

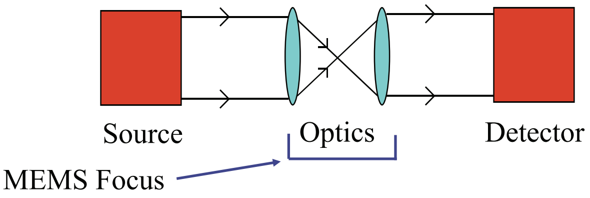

Figure 15. Illustration of micro optical electro mechanical systems (MOEMS).

Let's say a few more words about MEMS. Optical MEMS, or Micro optical electro mechanical systems, also known as MOEMS, are increasingly used in optoelectronics applications. We show the general system here in Figure 15, which contains a source, an optics element, and a detector. The optics section will have a MEMS focus to influence the light in waveguides or in free space. These elements might perform reflection, transmission, interference, or diffraction functions.

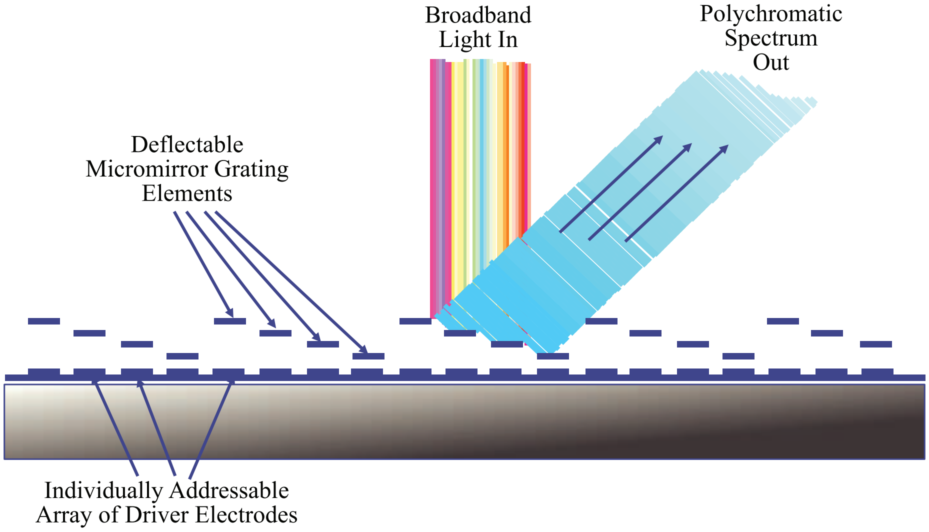

Figure 16. Illustration of MEMS variable diffraction grating.

Figure 16 is an example of a MEMS Variable Diffraction Grating. This device has an array of individually addressable driver electrodes that drive an array of deflectable micromirror grating elements. It can take broadband light in, and create a polychromatic spectrum out.

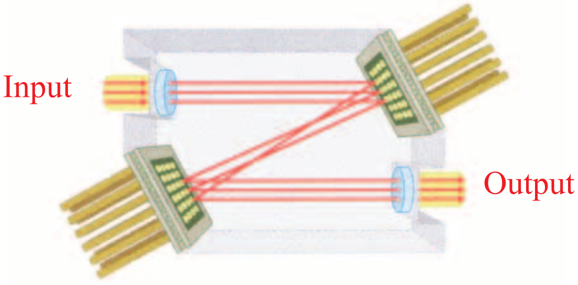

Figure 17. Illustration of micromirror array.

Another MEMS element is the Micromirror array. These can be made in various sizings, but 256 by 256 is quite common to switch light from one fiber to another. Although the array is quite useful, there are design and fabrication issues with this structure. The tilt angle will affect the array size. More tilt allows the beam access to more mirrors, but the tilt is limited by the non-linear electrostatic force in the array and the substrate clearance. Increasing the clearance and tilt will increase the actuation voltage, so there are limits as to what can be accomplished with this type of an array.

Another application of MEMS in optoelectronics is to create a variable wavelength laser. The emission wavelength of a laser depends on the length of the optical cavity, so we can use MEMS structures to make one side of the optical cavity movable, which allows one to change the emission wavelength or wavelengths. One could potentially use MOEMS actuators to enable the positioning.

In summary, there are a number of potential applications for optoelectronics. We discussed some of them here in Parts 1 and 2 of Applications Overview. Currently transmission and detection are the main applications, but manipulation of light is becoming more common. Look for many additional applications in the future.

Technical Tidbit

Film Resistors

In this month’s technical tidbit, we will discuss an older but still widely used system component: the film resistor.

The film resistor consists of a thin film of metal, carbon or metal oxide on a ceramic rod or tube. It uses metal end caps with wire leads that are either pressed or crimped on the ends of the rod or tube. Sometimes the end caps might be soldered to the rod or tube. The manufacturer uses an abrasive or a laser system to trim the metal film to give it the correct resistance value. The manufacturer then coats the tube, film and caps conformally with a polymer or epoxy. The materials are typically not hermetic, so moisture and contamination can work their way in. Some manufacturers may encase the resistor in a hermetically-sealed glass shell.

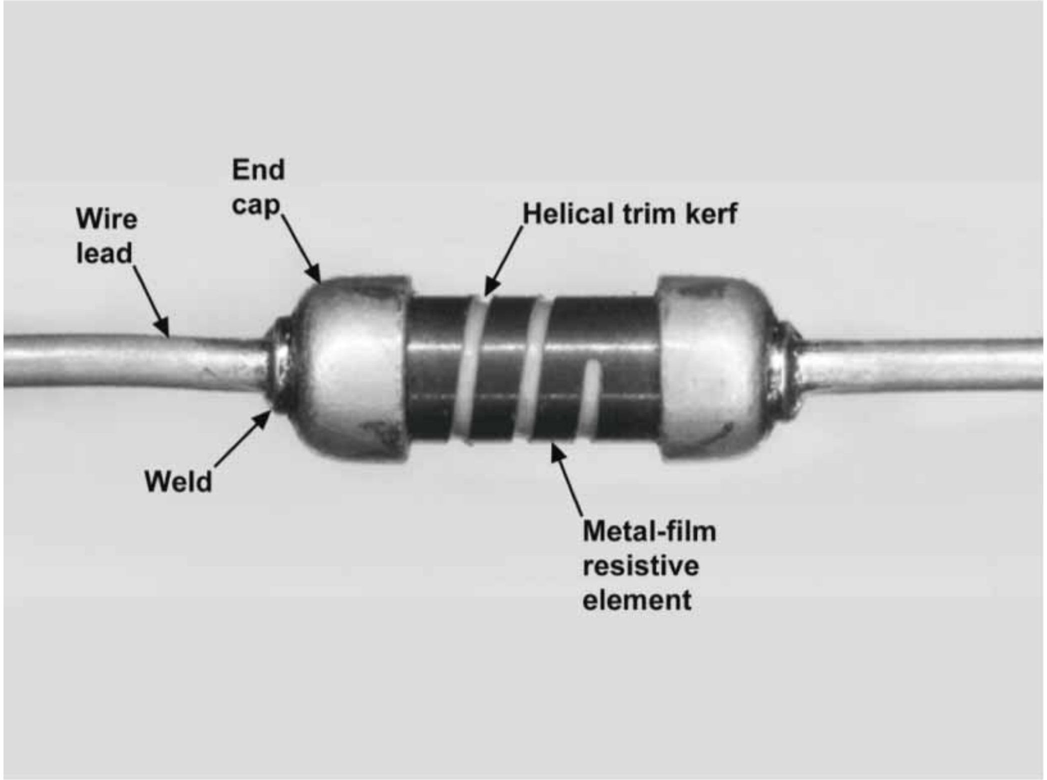

Figure 1.

This image in Figure 1 shows an example of the construction of a thin film resistor. In this image, we removed the exterior coating. One can see the wires, end caps, rod, metal film resistance element, and the trim kerf. In this resistor, the trim kerf creates a helical pattern. The wires are welded to the end caps in this resistor as well.

Figure 2.

The images in Figure 2 show examples of hermetically sealed thin film resistors. These resistors use a nickel-chromium, or nichrome alloy as the resistor element. The manufacturer seals the resistors using a glass envelope. The image on the left shows the envelopes of the two resistors intact, and the image on the right shows a resistor with the glass envelope removed. One can also see the spiral trim cut on the nichrome film.

Ask the Experts

Q: Is there a math model for the cost associated with improving the yield?

A: There have been papers published on this topic. Here is an example of one such paper:

Israel Tirkel, Gad Rabinowitz, David Price, Doug Sutherland, “Wafer Fabrication Yield Learning and Cost Analysis Based on In-line Inspection,” International Journal of Production Research, Vol. 54, No. 12, pp. 3578 – 3590, 2016

IRPS

International Reliability Physics Symposium

2020 IEEE International Reliability Physics Symposium

IEEE

March 29- April 2, 2020
Hilton DFW Lakes Executive Conference Center
1800 Highway 26E
Grapevine, TX, 76051-9641, USA

Registration is available at www.irps.org

Chris Henderson, Semitracks President

Chris would be happy to meet with you and discuss any training needs you have. Contact him at henderson@semitracks.com anytime before the symposium!

Spotlight: Advanced CMOS/FinFET Fabrication

OVERVIEW

Semiconductor and integrated circuit developments continue to proceed at an incredible pace. For example, today's microprocessor chips have one thousand times the processing power of those a decade ago. These challenges have been accomplished because of the integrated circuit industry's ability to track something known as Moore's Law. Moore's Law states that an integrated circuit's processing power will double every two years. This has been accomplished by making devices smaller and smaller. The question looming in everyone's mind is "How far into the future can this continue?" Advanced CMOS/ FinFET Fabrication is a 1-day course that offers detailed instruction on the processing used in a modern integrated circuit, and the processing technologies required to make them. We place special emphasis on current issues related to manufacturing the next generation devices. This course is a must for every manager, engineer and technician working in the semiconductor industry, using semiconductor components or supplying tools to the industry.

WHAT WILL I LEARN BY TAKING THIS CLASS

By concentrating on the latest developments in CMOS and FinFET technology, participants will learn why FinFETs and FD-SOI are fast becoming the technologies of choice at feature sizes below 20nm. Our instructors work hard to explain semiconductor processing without delving heavily into the complex physics and materials science that normally accompany this discipline.

Participants learn basic but powerful aspects about FinFET technology. This skill-building series is divided into four segments:

1. Front End Of Line (FEOL) Overview. Participants study the major developments associated with FEOL processing, including ion implantation, Rapid Thermal Annealing (RTA) for implants and silicides, and Pulsed Plasma Doping. They also study alternate substrate technologies like SOI as well as High-k/Metal Gates for improved leakage control.
2. Back End Of Line (BEOL) Overview. Participants study the major developments associated with BEOL processing, including copper metallization and Low-k Dielectrics. They learn about why they're necessary for improved performance.
3. FinFET Manufacturing Overview. Participants learn how semiconductor manufacturers are currently processing FinFET devices and the difficulties associated with three-dimensional structures from a processing and metrology standpoint.
4. FinFET Reliability. They also study the failure mechanisms and techniques used for studying the reliability of these devices.

COURSE OBJECTIVES

1. The seminar will provide participants with an in-depth understanding of SOI technology and the technical issues.
2. Participants will understand how Hi-K/Metal Gate devices are manufactured.
3. Participants will also understand how FinFET devices are manufactured.

4. The seminar provides a look into the latest challenges with copper metallization and Low-k dielectrics.
5. Participants will understand the difficulties associated with non-planar structures and methods to alleviate the problems.
6. Participants will be able to make decisions about how to evaluate FinFET devices and what changes are likely to emerge in the coming years.
7. Participants will briefly learn about IC reliability and the failure modes associated with these devices.
8. Finally, the participants see a comparison between FD-SOI (the leading alternative) and FinFETs.

COURSE OUTLINE

1. Advanced CMOS Fabrication – Introduction
2. Front End Of Line (FEOL) Processing
    a. SOI and FD-SOI
    b. Ion Implantation and Rapid Thermal Annealing
    c. Pulsed Plasma Doping
    d. Hi-K/Metal Gates
    e. Processing Issues
        i. Lithography
        ii. Etch
        iii. Metrology
3. Back End Of Line (BEOL) Processing
    a. Introduction and Performance Issues
    b. Copper
        i. Deposition Methods
        ii. Liners
        iii. Capping Materials
        iv. Damascene Processing Steps
    c. Lo-k Dielectrics
        i. Materials
        ii. Processing Methods
    d. Reliability Issues
4. FinFET Manufacturing Overview
    a. Substrates
        i. Bulk
        ii. SOI
    b. FinFET Types
    c. Process Sequence
    d. Processing Issues
        i. Lithography
        ii. Etch
        iii. Metrology

5. FinFET Reliability
    a. Defect density issues
    b. Gate Stack
    c. Transistor Reliability (BTI and Hot Carriers)
    d. Heat dissipation issues
    e. Failure analysis challenges
6. Future Directions for FinFETs
    a. Comparison of FD-SOI and FinFETs – Are FinFETs a better choice?
    b. Scaling

You may want to stress some aspects more than others or conduct a simple one-day overview course. Many of our clients seek ongoing just-in-time training that builds in-depth, advanced levels of reliability expertise. We'll work with you to determine the best course of action and create a statement of work that emulates the very best practices of semiconductor reliability analysis.

Our instructors are active in the field and they practice the disciplines daily. Please give us a call (505) 858-0454 or drop us an e-mail (info@semitracks.com).

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We look forward to hearing from you!

Upcoming Courses

(Click on each item for details)

Introduction to Processing

March 2 – 3, 2020 (Mon – Tue)
Portland, Oregon, USA

Failure and Yield Analysis

March 2 – 5, 2020 (Mon – Thur)
Portland, Oregon, USA

Advanced CMOS/FinFET Fabrication

March 4, 2020 (Wed)
Portland, Oregon, USA

IC Packaging Technology

March 5 – 6, 2020 (Thur – Fri)
Portland, Oregon, USA

Semiconductor Reliability / Product Qualification

March 9 – 12, 2020 (Mon – Thur)
Portland, Oregon, USA

Wafer Fab Processing

April 14 – 17, 2020 (Tue – Fri)
Munich, Germany

Semiconductor Reliability / Product Qualification

April 14 – 17, 2020 (Tue – Fri)
Munich, Germany

Failure and Yield Analysis

April 20 – 23, 2020 (Mon – Thur)
Munich, Germany

IC Packaging Technology

April 27 – 28, 2020 (Mon – Tue)
Munich, Germany

Advanced CMOS/FinFET Fabrication

April 30, 2020 (Thur)
Munich, Germany