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Test Structures—Basics Part 2

By Christopher Henderson

Last month, we discussed basic transistor reliability test structures. This month, we will continue to provide an overview of test structures as they pertain to reliability. Our focus will be on metallization test structures, gate oxide test structures, and ring oscillators. As a reminder, test structures can provide critical insight into the reliability of a semiconductor process. The advantage of using test structures is that one can evaluate a specific part of the process without having to design a complex integrated circuit. One can also provide feedback quickly, since many test structures can be realized without a full fabrication flow.

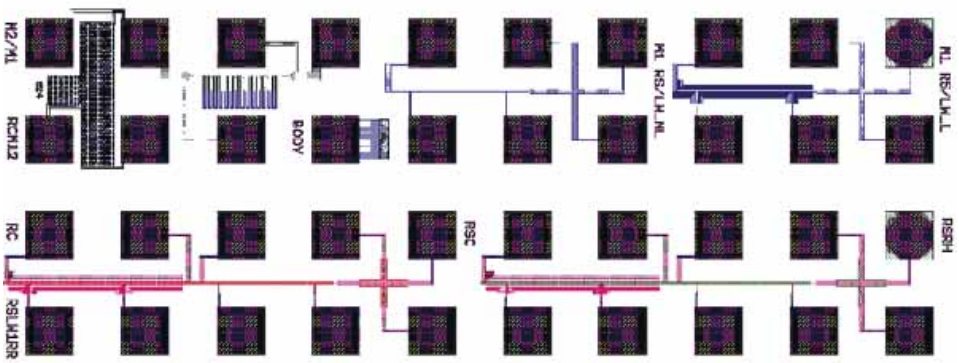


Figure 6. Test structures: M1 and M2 sheet resistance.

In this Issue:

In order to characterize the resistance of thin films, one can create test structures for measuring sheet resistance. Sheet resistance measurements utilize four-point—or Kelvin—probe measurement techniques where one forces a current and measures the voltage drop. The structures shown here in Figure 6 examine metal 1 and metal 2 sheet resistance.

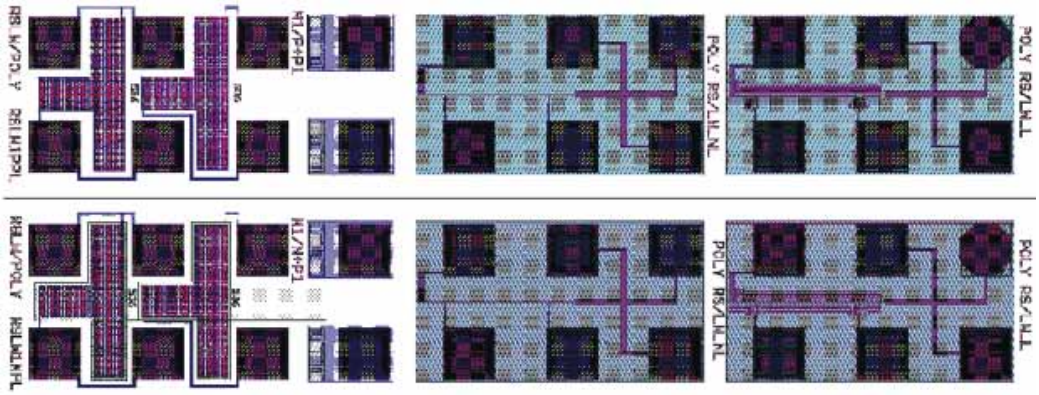


Figure 7. Test structures: poly sheet resistance.

In addition to metal thin films, some technologies contain other conductive thin films such as polysilicon. This test structure in Figure 7 is used to make 4-point measurements on polysilicon.

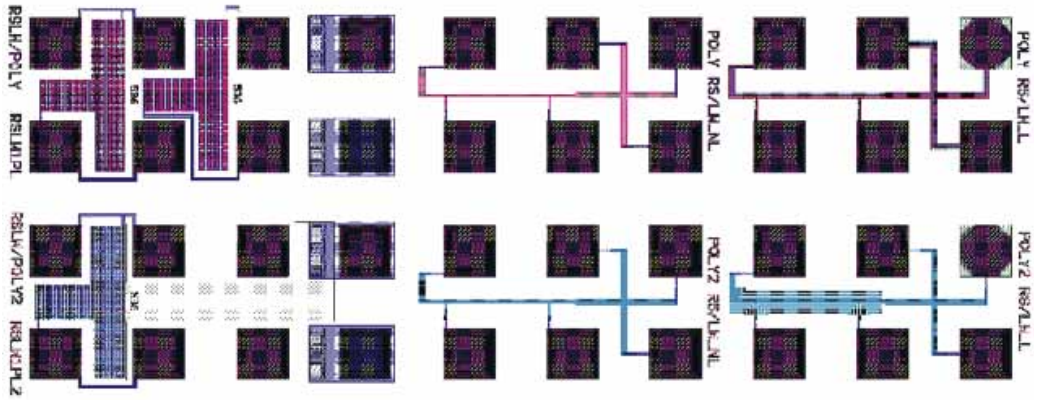


Figure 8. Test structures: silicided polysilicon structures.

Polysilicon must be examined in its silicided and non-silicided states. These test structures in Figure 8 do not have the silicide block mask, so the polysilicon structures here have been silicided.

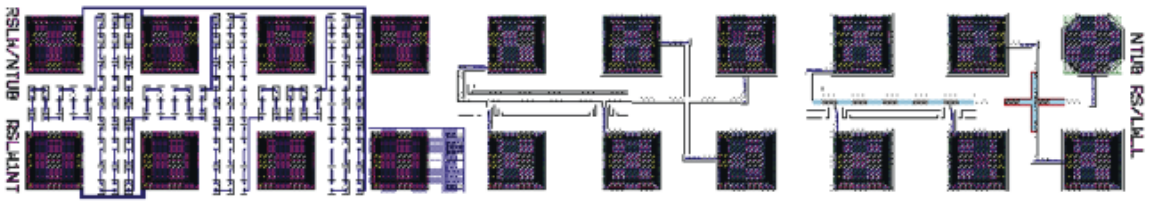


Figure 9. Test structures: N-tub resistance.

In addition to metal and polysilicon thin films, one must be able to characterize implant and well regions. Although implants and wells—or tubs as they are sometimes called—are quite stable under most conditions, they can affect the reliability of the transistor. This image in Figure 9 shows test structures designed to measure n-well resistance.

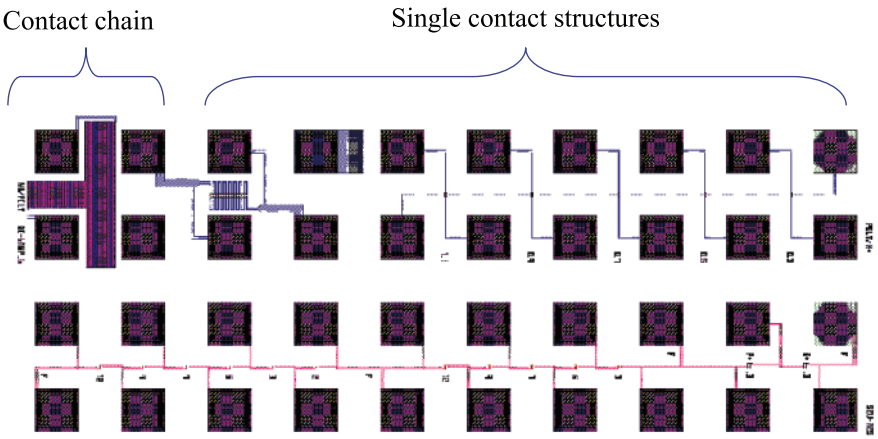


Figure 10. Test structures: M1-poly contacts.

Contacts are an important aspect of the design and must be examined in detail. This set of structures in Figure 10 contains single contacts of varying sizes and contact chains. Single contacts allow the engineer to characterize differences between individual contacts, and contact chains allow the engineer to examine systematic changes that cause more subtle resistance changes. The structures shown here are used to characterize metal-1 to polysilicon contacts.

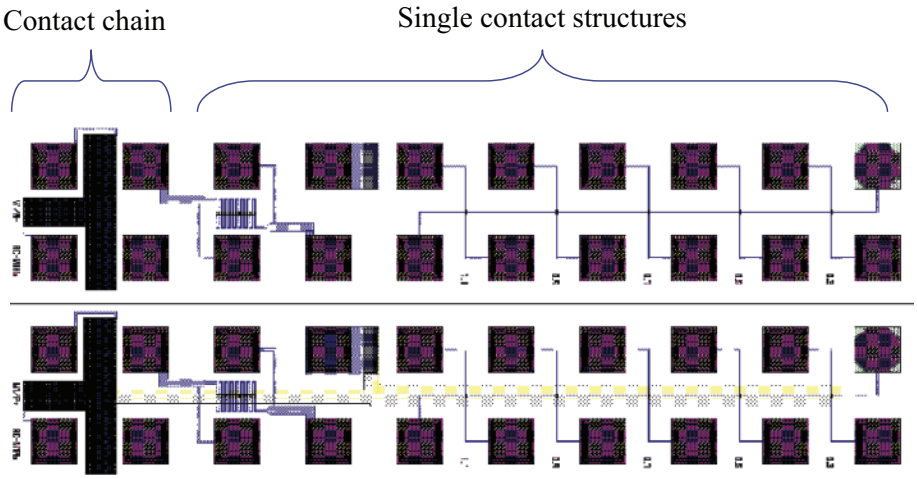


Figure 11. Test structures: M1-silicon contacts.

The structures shown in Figure 11 are used to characterize metal-1 to silicon contacts. In order to properly characterize the contact process, one requires contacts to both n+ and p+ implant regions.

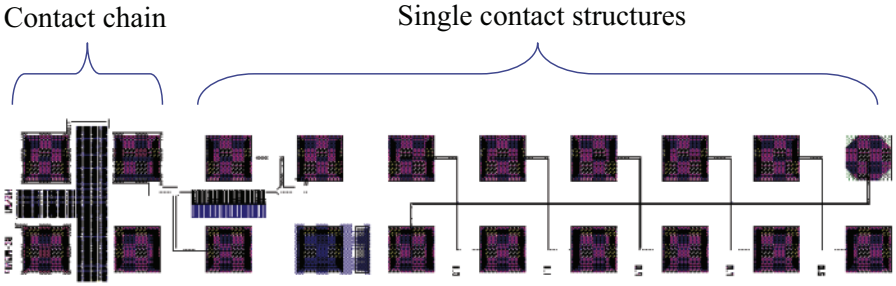


Figure 12. Test structures: metal-1 to metal-2 vias.

The structures shown in Figure 12 are used to characterize metal-1 to metal-2 vias. In a multilevel process, one would need via test structures for each of the vias allowed in the process.

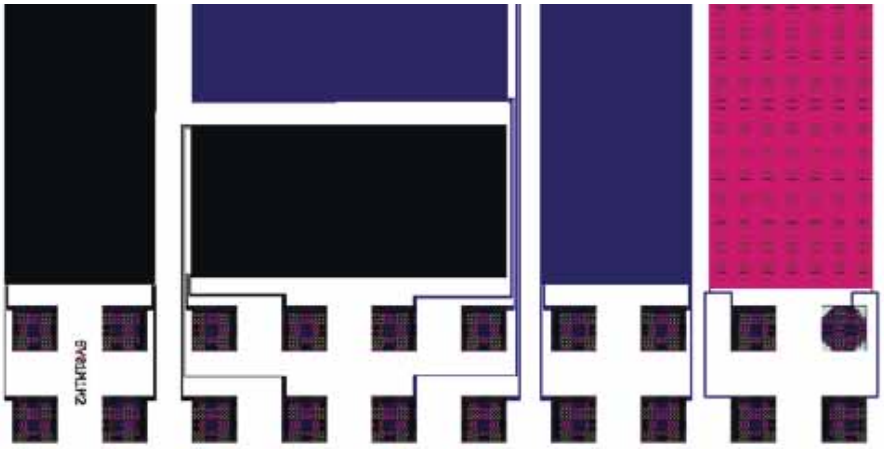


Figure 13. Test structures: M1 – M2 shorts.

One must look not only for increased resistance and opens, but also leakage paths and shorts to adjacent layers. This structure allows the engineer to look for metal-1 to metal-2 shorts. The dark areas shown in the image in Figure 13 are actually long lengths of metal-1 and metal-2 that crisscross over each other. The test structure contains long lengths of metal-1 lines adjacent to each other on a minimum pitch or closest allowed spacing. It also contains long lengths of metal-2 lines adjacent to each other on minimum pitch.

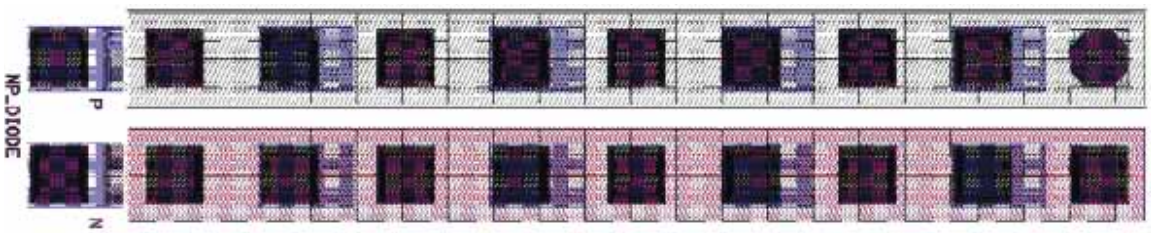


Figure 14. Test structures: diodes.

The diode is another common test structure. These are large area diode test structures. This particular structure allows accurate checking of diode characteristics and indirect observation of doping information.

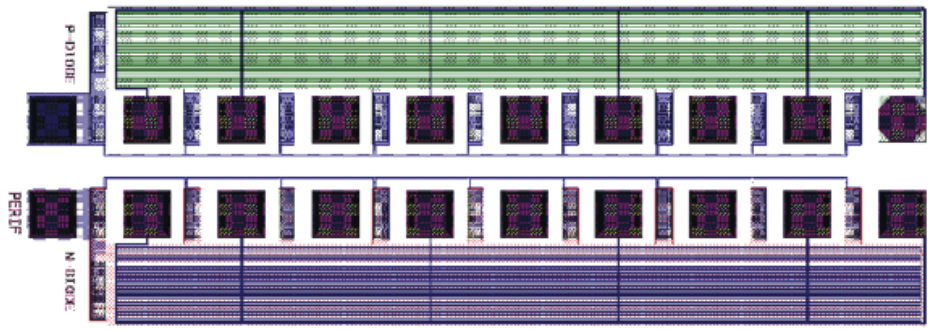


Figure 15. Test structures: diodes in parallel.

Another common diode test structure places many smaller diodes in parallel with one another. This allows the engineer to more accurately check junction capacitance values and monitor forward current characteristics.

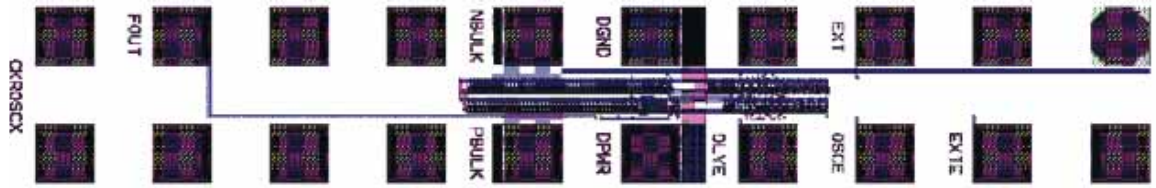


Figure 16. Test structures: ring oscillator.

The ring oscillator is another common test structure. A ring oscillator is a series of inverters where the number of inverters is an odd number. The output of the last inverter drives the input of the first inverter. Normally, ring oscillators are used to evaluate the frequency response of the circuit technology. The smaller the feature size, the faster the circuit will tend to operate. This structure can also be used to monitor hot carrier damage, since hot carrier damage tends to slow the switching speed of the n-channel transistor. Since the circuit switches at the highest frequency possible, it represents a worst-case scenario for a digital circuit.

Technical Tidbit

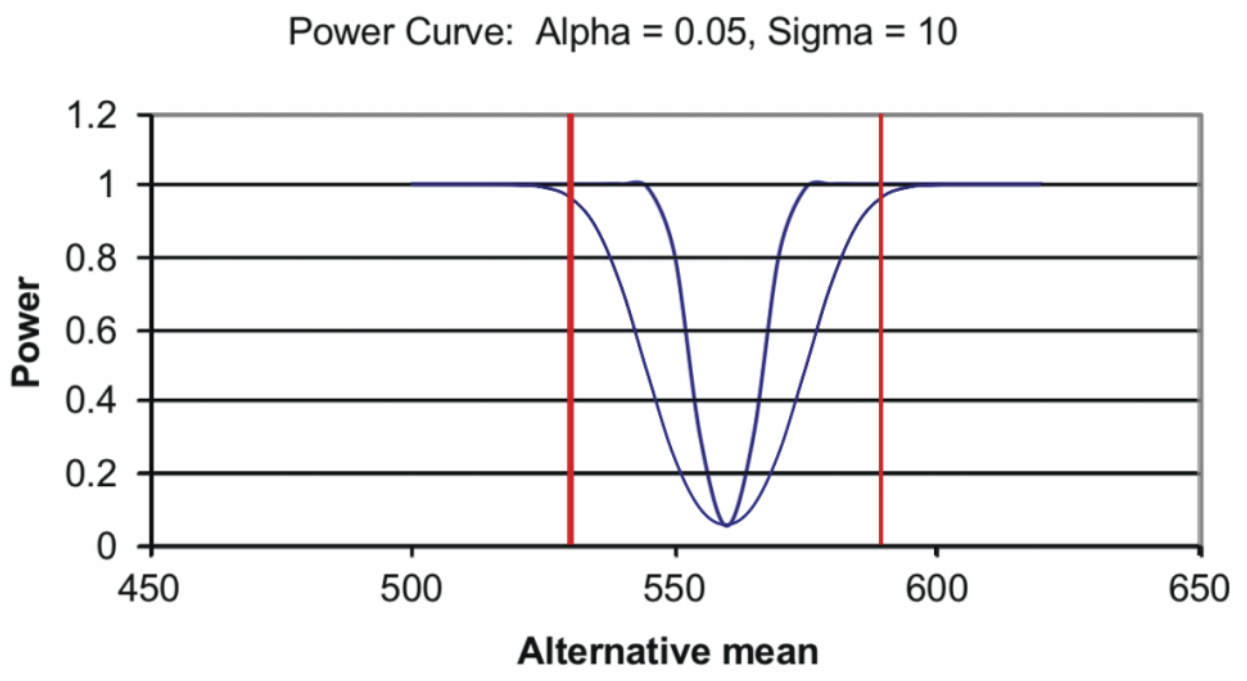
Single Mean Hypothesis Testing

In this technical tidbit, we will discuss a test sometimes used in conjunction with a Design of Experiments, or DOE, called the single mean hypothesis test. Occasionally, engineers would like to know if experimental data lines up with predicted data. Because a Design of Experiments uses a limited number of samples, we need a method to determine if the actual data fits to the predicted data. The method that we use is called the single mean hypothesis test.

To illustrate, let's use an example. Let's assume a CVD Tool Manufacturer claims that the exhaust pumping rate does not have any effect on deposition. Suppose the manufacturer claims that the average oxide thickness is 570Å with standard deviation of 50Å. To test the vendor's claim we choose a random sample of wafers and increase the pumping rate. Furthermore, let's assume we need a level of significance, or an alpha value of 0.05. We measure the actual deposition thickness, and then ask ourselves, does this data indicate the manufacturer's claims are correct, or incorrect?

So the actual sample mean is 560Å with an actual sample deviation of 25Å. Let's assume a sample size of 10 wafers. In this case, the computed t-statistic is 1.264911 and the P-value is 0.004678. The t-statistic is less than the t-critical value of 1.959964, which corresponds to an alpha value of 0.05. We can then conclude that since the t-statistic is less than t-critical, and the P-value is greater than 0.05, we would accept the hypothesis, and therefore we would assume the manufacturer's claims are true.

Next, let's assume a larger sample size of 50 wafers. In this case, the computed t-statistic is 2.828427 and the P-value is 0.004678. The t-statistic is greater than the t-critical value of 1.959964, which corresponds to an alpha value of 0.05. We can then conclude that since the t-statistic is greater than t-critical, and the P-value is less than 0.05, we would reject the hypothesis, and therefore we would assume the manufacturer's claims are false. So we see that the sample size plays a key role in our ability to confirm or deny the manufacturer's claims.



One way to represent this concept is to do it graphically using something called the power curve. The outer curve shows the power curve for the single mean hypothesis test for a sample size of 10 wafers. The power curve is a method to help the analyst understand the probability of rejecting the null hypothesis. Overlaid on top of this, the inner curve shows the power curve for a sample size of 50 wafers. Values closer to 1 mean a greater chance of rejecting the null hypothesis. Notice that for a given mean value, the increased number of samples produces a greater chance of rejecting the null hypothesis when the experiment yields a value away from the original mean, since we have more data points to better identify the mean value.

Ask the Experts

Q: Does the probe mark from wafer probe affect the wire bonding process?

A: It can, but it is usually not a big issue. The uneven metal on the pad caused by the probe tip can reduce the bonding surface of the wire bond, but normally there is sufficient area to still achieve a good bond. However, sometimes there is sufficient disturbance of the metal to lead to a weak or failed bond.

Spotlight: Failure and Yield Analysis

OVERVIEW

Failure and Yield Analysis is an increasingly difficult and complex process. Today, engineers are required to locate defects on complex integrated circuits. In many ways, this is akin to locating a needle in a haystack, where the needles get smaller and the haystack gets bigger every year. Engineers are required to understand a variety of disciplines in order to effectively perform failure analysis. This requires knowledge of subjects like: design, testing, technology, processing, materials science, chemistry, and even optics! Failed devices and low yields can lead to customer returns and idle manufacturing lines that can cost a company millions of dollars a day. Your industry needs competent analysts to help solve these problems. ***Advanced Failure and Yield Analysis*** is a four-day course that offers detailed instruction on a variety of effective tools, as well as the overall process flow for locating and characterizing the defect responsible for the failure. This course is designed for every manager, engineer, and technician working in the semiconductor field, using semiconductor components or supplying tools to the industry.

By focusing on a ***Do It Right the First Time*** approach to the analysis, participants will learn the appropriate methodology to successfully locate defects, characterize them, and determine the root cause of failure.

Participants learn to develop the skills to determine what tools and techniques should be applied, and when they should be applied. This skill-building series is divided into three segments:

1. **The Process of Failure and Yield Analysis.**Participants learn to recognize correct philosophical principles that lead to a successful analysis. This includes concepts like destructive vs. non-destructive techniques, fast techniques vs. brute force techniques, and correct verification.
2. **The Tools and Techniques.** Participants learn the strengths and weaknesses of a variety of tools used for analysis, including electrical testing techniques, package analysis tools, light emission, electron beam tools, optical beam tools, decapping and sample preparation, and surface science tools.
3. **Case Histories.** Participants identify how to use their knowledge through the case histories. They learn to identify key pieces of information that allow them to determine the possible cause of failure and how to proceed.

COURSE OBJECTIVES

1. The seminar will provide participants with an in-depth understanding of the tools, techniques and processes used in failure and yield analysis.
2. Participants will be able to determine how to proceed with a submitted request for analysis, ensuring that the analysis is done with the greatest probability of success.
3. The seminar will identify the advantages and disadvantages of a wide variety of tools and techniques that are used for failure and yield analysis.
4. The seminar offers a wide variety of video demonstrations of analysis techniques, so the analyst can get an understanding of the types of results they might expect to see with their equipment.
5. Participants will be able to identify basic technology features on semiconductor devices.
6. Participants will be able to identify a variety of different failure mechanisms and how they manifest themselves.
7. Participants will be able to identify appropriate tools to purchase when starting or expanding a laboratory.

INSTRUCTIONAL STRATEGY

By using a combination of instruction by lecture, video, and question/answer sessions, participants will learn practical approaches to the failure analysis process. From the very first moments of the seminar until the last sentence of the training, the driving instructional factor is **application**. We use instructors who are internationally recognized experts in their fields that have years of experience (both current and relevant) in this field. The handbook offers hundreds of pages of additional reference material the participants can use back at their daily activities.

THE SEMITRACKS ANALYSIS INSTRUCTIONAL VIDEOS™

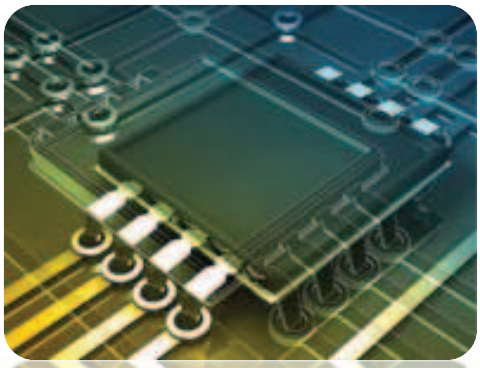
One unique feature of this workshop is the video segments used to help train the students. Failure and Yield Analysis is a visual discipline. The ability to identify nuances and subtleties in images is critical to locating and understanding the defect. Many tools output video images that must be interpreted by analysts. No other course of this type uses this medium to help train the participants. These videos allow the analysts to directly compare material they learn in this course with real analysis work they do in their daily activities.

COURSE OUTLINE

1. Introduction
2. Failure Analysis Principles/Procedures
    a. Philosophy of Failure Analysis
    b. Flowcharts
3. Gathering Information
4. Package Level Testing
    a. Optical Microscopy
    b. Acoustic Microscopy
    c. X-Ray Radiography
    d. Hermetic Seal Testing
    e. Residual Gas Analysis
5. Electrical Testing
    a. Basics of Circuit Operation
    b. Curve Tracer/Parameter Analyzer Operation
    c. Quiescent Power Supply Current
    d. Parametric Tests (Input Leakage, Output voltage levels, Output current levels, etc.)
    e. Timing Tests (Propagation Delay, Rise/Fall Times, etc.)
    f. Automatic Test Equipment
    g. Basics of Digital Circuit Troubleshooting
    h. Basics of Analog Circuit Troubleshooting

6. Decapsulation/Backside Sample Preparation
    a. Mechanical Delidding Techniques
    b. Chemical Delidding Techniques
    c. Backside Sample Preparation Techniques
7. Die Inspection
    a. Optical Microscopy
    b. Scanning Electron Microscopy
8. Photon Emission Microscopy
    a. Mechanisms for Photon Emission
    b. Instrumentation
    c. Frontside
    d. Backside
    e. Interpretation
9. Electron Beam Tools
    a. Voltage Contrast
        i. Passive Voltage Contrast
        ii. Static Voltage Contrast
        iii. Capacitive Coupled Voltage Contrast
        iv. Introduction to Electron Beam Probing
    b. Electron Beam Induced Current
    c. Resistive Contrast Imaging
    d. Charge-Induced Voltage Alteration
10. Optical Beam Tools
    a. Optical Beam Induced Current
    b. Light-Induced Voltage Alteration
    c. Thermally-Induced Voltage Alteration
    d. Seebeck Effect Imaging
    e. Electro-optical Probing
11. Thermal Detection Techniques
    a. Infrared Thermal Imaging
    b. Liquid Crystal Hot Spot Detection
    c. Fluorescent Microthermal Imaging
12. Chemical Unlayering
    a. Wet Chemical Etching
    b. Reactive Ion Etching
    c. Parallel Polishing
13. Analytical Techniques
    a. TEM
    b. SIMS
    c. Auger
    d. ESCA/XPS

14. Focused Ion Beam Technology
    a. Physics of Operation
    b. Instrumentation
    c. Examples
    d. Gas-Assisted Etching
    e. Insulator Deposition
    f. Electrical Circuit Effects
15. Case Histories



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To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered in the next newsletter, please contact Jeremy Henderson by Email (jeremy.henderson@semitracks.com).

We are always looking for ways to enhance our courses and educational materials.

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We look forward to hearing from you!

Upcoming Courses

(Click on each item for details)

Failure and Yield Analysis
April 23 – 26, 2019 (Tue – Fri)
Munich, Germany

Wafer Fab Processing
April 23 – 26, 2019 (Tue – Fri)
Munich, Germany

EOS, ESD and How to Differentiate
April 29 – 30, 2019 (Mon – Tue)
Munich, Germany

Semiconductor Reliability / Product Qualification
May 6 – 9, 2019 (Mon – Thur)
Munich, Germany

Semiconductor Reliability / Product Qualification
May 13 – 16, 2019 (Mon – Thur)
Tel Aviv, Israel

Introduction to Processing
June 3 – 4, 2019 (Mon – Tue)
San Jose, California, USA

Advanced CMOS/FinFET Fabrication
June 5, 2019 (Wed)
San Jose, California, USA

Interconnect Process Integration
June 6, 2019 (Thur)
San Jose, California, USA

Failure and Yield Analysis
June 3 – 6, 2019 (Mon – Thur)
San Jose, California, USA