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Low-K Materials Properties Part 1

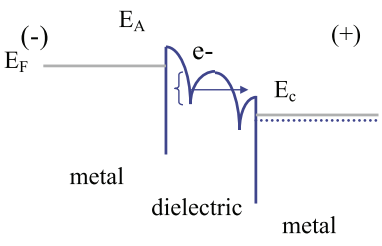
By Christopher Henderson

In this section, we will discuss the materials properties of low-k materials. The properties of these materials are key to understanding the reliability in these applications. The industry is just beginning to understand these materials and how they behave in thin films and semiconductor applications.

This discussion will center on two materials properties groups. They include the electrical properties of the materials and the mechanical properties. To begin this discussion, we will cover the electrical properties. This includes thermionic emission, Frenkel-Poole conduction, ohmic conduction, space charge limited current, as well as other leakage mechanisms.

Important at low fields for SiC, Si_3N_4 and organic materials (i.e. any materials with traps)

$$J \approx \sigma\varepsilon \cdot exp\left(\frac{-qE_A}{Kt}\right)$$



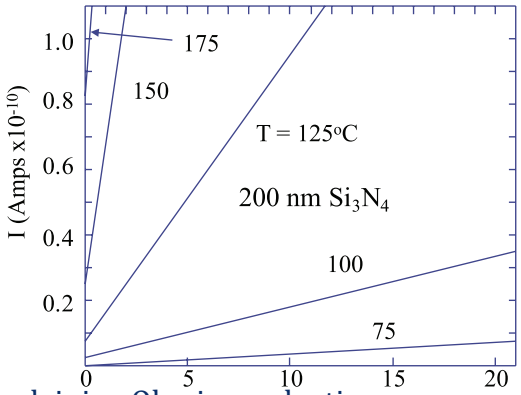


Figure 1. Diagram explaining Ohmic conduction.

In this Issue:

The three main breakdown mechanisms are Ohmic conduction, Frenkel-Poole emission and thermionic emission. First, we'll discuss ohmic conduction. This mechanism is important at low electric fields for materials that exhibit high trap densities. This includes silicon carbides, silicon nitrides, and organic materials. With ohmic conduction, the leakage current is directly proportional to the voltage across the dielectric.

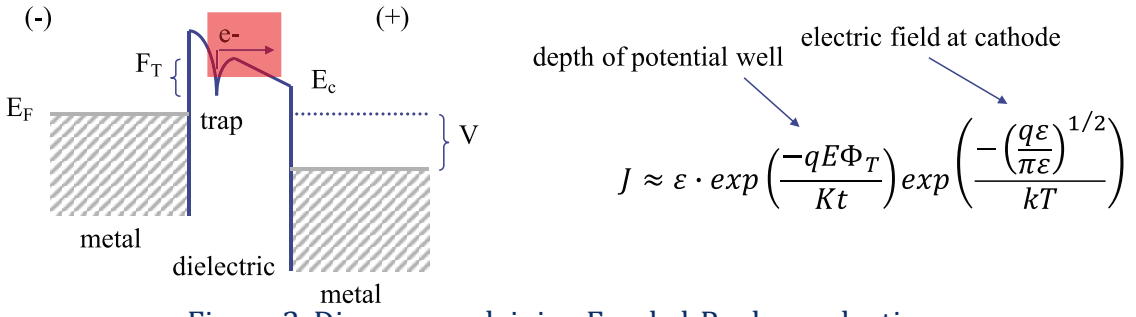


Figure 2. Diagram explaining Frenkel-Poole conduction.

Next, we'll discuss Frenkel-Poole conduction. When one performs a time-dependent dielectric breakdown test, there will be leakage between the metal lines. This leakage can occur between horizontal or vertical lines. One places a voltage between two lines of interest and determines the time it takes for a breakdown to occur. The current occurs as electrons travel into traps in the dielectric and then are emitted thermally. This mechanism has been observed in several materials the industry currently uses, such as carbon-doped oxides and the silicon carbide and silicon nitride capping layers.

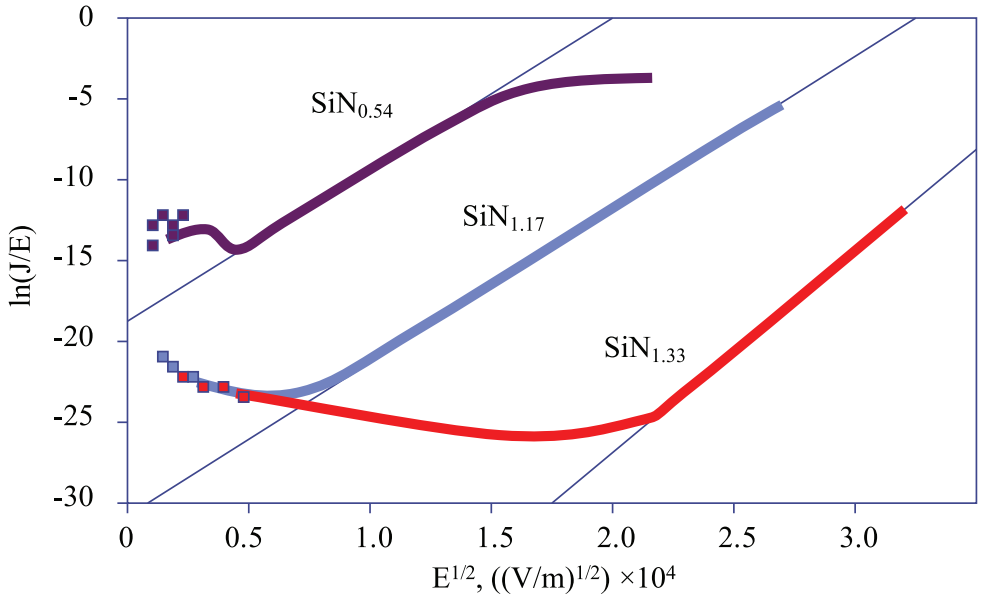
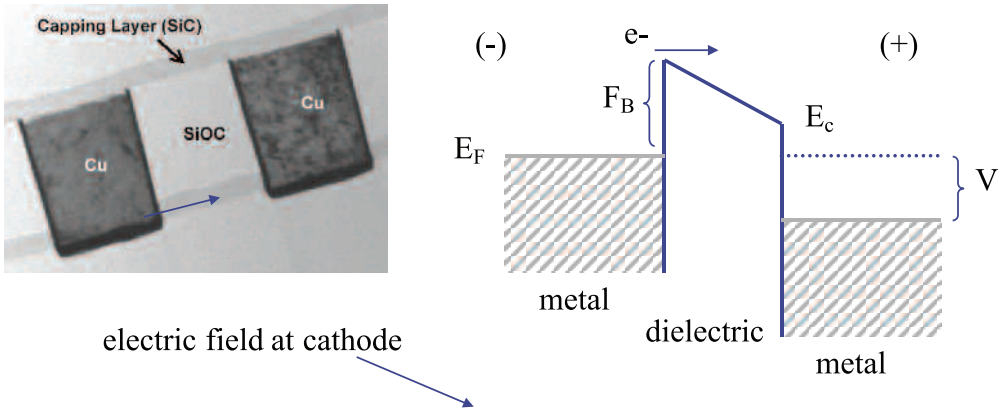


Figure 3. Frenkel-Poole conduction data as function of electric field.

The graph in Figure 3 shows experimental Frenkel-Poole conduction data as a function of electric field. Notice that the field dependence is proportional to the square root of the electric field. It is also a thermally activated process.



$$J \approx A^* T^2 \cdot exp\left(\frac{-q\Phi_T}{Kt}\right) exp\left(\frac{-\left(\frac{q\varepsilon}{4\pi\varepsilon}\right)^{1/2}}{kT}\right)$$

Figure 4. Thermionic (Schottky)-emission.

Another type of leakage that researchers observe in these materials is thermionic emission or Schottky emission as it is sometimes called. In this case, the electrons surmount the barrier between the dielectric and the metal due to thermal activation. The field and temperature dependence is very similar to that of Frenkel-Poole conduction. The way researchers distinguish between Frenkel-Poole conduction and thermionic emission is to extract the dielectric constant of the material and determine if it agrees with the type of materials involved in the experiment.

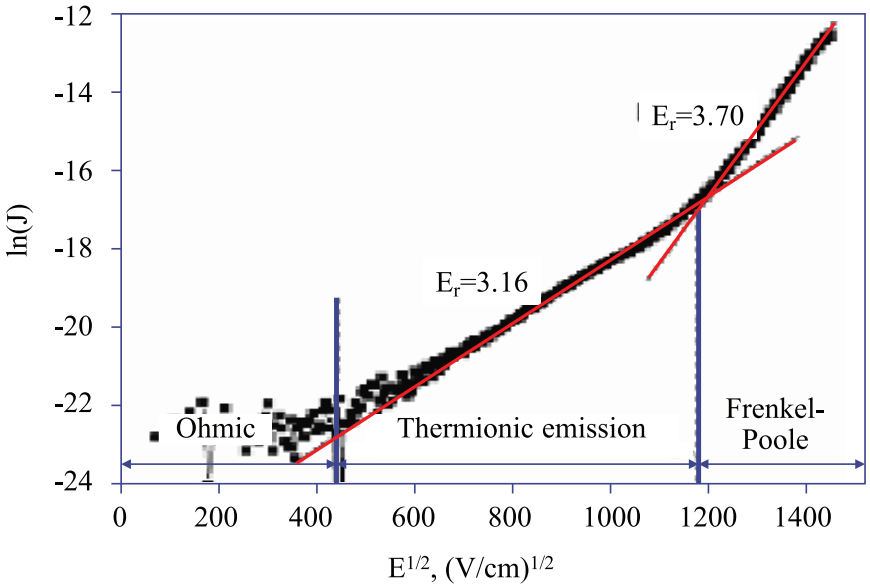


Figure 5. Conduction in integrated structures: multiple mechanisms.

The graph in Figure 5 shows the three leakage mechanisms and their relationship with one another. The ohmic regime operates at the lowest fields, thermionic emission is active at moderate fields, and Frenkel-Poole emission is active at high fields. Notice that one can distinguish between thermionic emission and Frenkel-Poole emission by the slope of the lines.

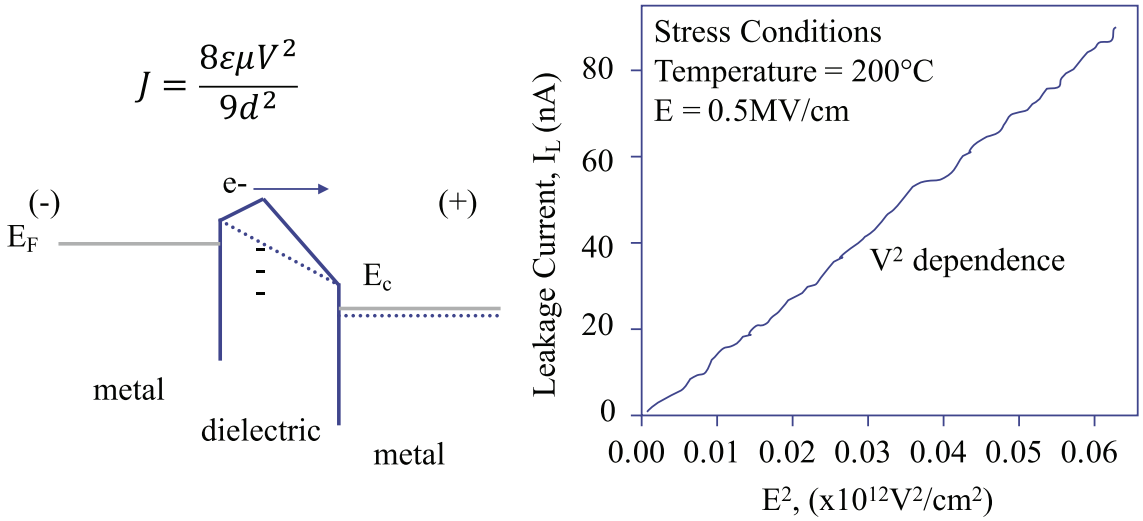


Figure 6. Diagram and data showing space-charge-limited current.

Another type of current that can occur in low-k dielectrics is space-charge-limited current. It is important in materials when the barrier height is low, typically organic materials. In this situation, the space-charge region effectively lowers the barrier height of the dielectric, allowing electrons to more easily surmount the barrier. This leakage current has a dependence on the square of the electric field.

Other leakage mechanisms include ionic conduction and Fowler-Nordeim tunneling. Ionic conduction is important for dielectrics with a high concentration of mobile ions. In ionic conduction, the current is proportional to the electric field and the reciprocal of the temperature. Fowler-Nordheim tunneling is important at high fields. This is not an issue yet for low-k materials, since the spacing between lines restricts the electric fields to values below one megavolt per centimeter. In Fowler-Nordheim tunneling, the current is proportional to the square root of the electric field, and is independent of temperature.

In summary, we discussed four major types of leakage currents in low-k dielectrics: ohmic conduction, thermionic emission, Frenkel-Poole emission, and space-charge-limited current. Ohmic conduction is important at low electric fields for materials with traps. Thermally activated carriers can move through the material along shallow traps. Thermionic emission is a moderate field mechanism where electrons are thermally activated over the metal-insulator barrier. This is important in dielectrics with few or no traps. Frenkel-Poole emission is a high field mechanism that is important for materials with traps. In this situation, the electrons tunnel into a trap and are then thermally activated out of the trap. This is more common in materials with interfaces and can be thought of as interface conduction.

[To be continued in next month's issue.]

Technical Tidbit

A Brief Contrast Between Formal Verification and Simulation

In this month's technical tidbit, we will compare Formal Verification to Simulation. Formal verification is becoming increasingly important for high reliability applications, and is an important technique for demonstrating design correctness and demonstrating correct behavior to the customer. In particular in this technical tidbit, we will compare formal property verification (FPV) to functional simulation.

Key area of difference	Simulation	FPV
What types and sizes of models can be run?	Up to full-chip level, and both synthesizable and behavioral code	Unit of cluster level, or full-chip with lots of removed logic and synthesizable code only
How to reach targeted behaviors?	Describe the journey: generate input values to create desired behaviors	Describe the destination: specify target property or state, tool finds if it's reachable
What values are checked?	Specific values: simulator checks design based on user-specified inputs	Universe of all possible values: tool analyzes space of legal values under current constraints
How do we constrain the model?	Active constraints: we implicitly constrain the model by limiting the values passed in during simulation	Passive constraints: use assumptions to rule out all illegal cases
How are constraints on internal nodes handled?	Forced values: a love constraint on an internal signal affects only downstream logic	Back-propagation + Forward-propagation: a constraint affects the universe of possible values, in its fan-in and fan-out logic
What do we use for debug?	Single trace: when a simulation fails, you need to debug what was simulated	Example from FPV space: the tool presents one example from a family of possible failures
How long are typical traces?	Thousands of cycles: typically need to represent full machine startup and do many random things before hitting complex ones	Tens of cycles: FPV usually generates a minimal path to any target, resulting in much smaller traces with little extra activity

This table summarizes the differences between simulation and formal property verification. We show the key areas of difference on the left, the way this item is handled in simulation in the center, and the way this item is handled in formal property verification or the right.

Let's summarize the advantage using a combination lock example. In simulation, each attempt at opening the lock requires three cycles during which we can input a total of 10,000 possible values on each cycle. As such, we would need to go through 10 raised to the power 4 times 3, divided by 2, or about 500 billion simulation cycles. We would require 1 trillion simulation cycles for complete coverage. Using formal property verification, we can use a single FPV to cover the entire verification space. If there is a problem, we simply correct the RTL or bug, and re-run the single FPV run. In FPV, a typical failure trace will be very short, in many cases just 10 – 20 cycles after reset.

Ask the Experts

Q: Why do some technologies use both shallow and deep wells for transistors?

A: A common use for shallow and deep wells in a CMOS process is to accommodate both low and high voltages on an IC. We can use the shallow well to contain the transistors that operate in the core of the IC, and the deep well to contain the transistors that interface to the outside world. The deep well can support a larger diffusion region, and therefore higher voltages. An example of a core voltage might be 1.5 volts, and an example of an interface voltage might be 3.3 volts..

Spotlight: Wafer Fab Processing

OVERVIEW

Semiconductor and integrated circuit developments continue to proceed at an incredible pace. The industry as a whole has gotten to this point of incredible complexity through the process of countless breakthroughs and developments in wafer fab processing. Today's wafer fab contains some of the most complex and intricate procedures ever developed by mankind. ***Wafer Fab Processing*** is a 4-day course that offers an in-depth look into the semiconductor manufacturing process, and the individual processing technologies required to make them. We place special emphasis on the basics surrounding each technique, and we delve into the current issues related to manufacturing the next generation devices. This course is a must for every manager, engineer and technician working in the semiconductor industry, using semiconductor components or supplying tools to the industry.

By focusing on the basics of each processing step and the issues surrounding them, participants will learn why certain techniques are preferred over others. Our instructors work hard to explain how semiconductor processing works without delving heavily into the complex physics and mathematical expressions that normally accompany this discipline.

Participants learn basic but powerful aspects about the semiconductor industry. This skill-building series is divided into three segments:

1. **Basic Processing Steps.** Each processing step addresses a specific need in IC creation. Participants learn the fundamentals of each processing step and why they are used in the industry today.
2. **The Evolution of Each Processing Step.** It is important to understand how wafer fab processing came to the point where it is today. Participants learn how each technique has evolved for use in previous and current generation ICs.
3. **Current Issues in Wafer Fab Processing.** Participants learn how many processing steps are increasingly constrained by physics and materials science. They also learn about the impact of using new materials in the fabrication process and how those materials may create problems for the manufacturers in the future.

COURSE OBJECTIVES

1. The seminar will provide participants with an in-depth understanding of the semiconductor industry and its technical issues.
2. Participants will understand the basic concepts behind the fundamental wafer fab processing steps.
3. The seminar will identify the key issues related to each of the processing techniques and their impact on the continued scaling of the semiconductor industry.
4. The seminar offers a wide variety of sample problems that participants work to help them gain knowledge of the fundamentals of wafer fab processing.
5. Participants will be able to identify the basic features and principles associated with each major processing step. These include processes like chemical vapor deposition, ion implantation, lithography, and etching.
6. Participants will understand how processing, reliability, power consumption and device performance are interrelated.

7. Participants will be able to make decisions about how to construct and evaluate processing steps for CMOS, BiCMOS, and bipolar technologies.

INSTRUCTIONAL STRATEGY

By using a combination of instruction by lecture, classroom exercises, and question/answer sessions, participants will learn practical information on semiconductor processing and the operation of this industry. From the very first moments of the seminar until the last sentence of the training, the driving instructional factor is **application**. We use instructors who are internationally recognized experts in their fields that have years of experience (both current and relevant) in this field. The accompanying textbook offers hundreds of pages of additional reference material participants can use back at their daily activities.

COURSE OUTLINE

Day 1

1. Module 1: Basics & Fundamentals; Semiconductor Devices and ICs
    a. Acronyms
    b. Common Terminology
    c. Brief History
    d. Semiconductor Materials
    e. Electrical Conductivity
    f. Semiconductor Devices
    g. Classification of ICs & IC Processes
    h. Integrated Circuit Types
2. Module 2: Crystallinity, Crystal Defects, Crystal Growth
    a. Crystallinity
    b. Crystal Defects
    c. Crystal Growth
    d. Controlling Crystal Defects
3. Module 3: Basic CMOS Process Flow
    a. Transistors and Isolation
    b. Contacts/Vias Formation
    c. Interconnects
    d. Parametric Testing
4. Module 4: Ion Implantation 1 (The Science)
    a. Doping Basics
    b. Ion Implantation Basics
    c. Dopant Profiles
    d. Crystal Damage & Annealing
5. Module 5: Ion Implantation 2 (Equipment, Process Issues)
    a. Equipment
    b. Process Challenges
    c. Process Monitoring & Characterization
    d. New Techniques

Day 2

6. Module 6: Thermal Processing
    a. Overview of Thermal Processing
    b. Process Applications of SiO2
    c. Thermal Oxidation
    d. Thermal Oxidation Reaction Kinetics
    e. Oxide Quality
    f. Atomistic Models of Thermal Diffusion
    g. Thermal Diffusion Kinetics
    h. Thermal Annealing
    i. Thermal Processing Hardware
    j. Process Control
7. Module 7: Contamination Monitoring and Control
    a. Contamination Forms & Effects
    b. Contamination Sources & Control
    c. Contamination Characterization & Measurement
8. Module 8: Wafer Cleaning
    a. Wafer Cleaning Strategies
    b. Chemical Cleaning
    c. Mechanical Cleaning
9. Module 9: Vacuum, Thin Film, & Plasma Basics
    a. Vacuum Basics
    b. Thin Film Basics
    c. Plasma Basics
10. Module 10: CVD 1 (Basics, LPCVD, Epitaxy)
    a. CVD Basics
    b. LPCVD Films
    c. LPCVD Equipment
    d. Epi Basics
    e. Epi Process Applications
    f. Epi Deposition Process
    g. Epi Deposition Equipment

Day 3

11. Module 11: PVD
    a. PVD (Physical Vapor Deposition) Basics
    b. Sputter Deposition Process
    c. Sputter Deposition Equipment
    d. Al-Based Films
    e. Step Coverage and Contact/Via Hole Filling
    f. Metal Film Evaluation
12. Module 12: Lithography 1 (Photoresist Processing)
    a. Basic Lithography Process
    b. Photoresist Materials
    c. Photoresist Process Flow
    d. Photoresist Processing Systems

13. Module 13: Lithography 2 (Image Formation)
    a. Basic Optics
    b. Imaging
    c. Equipment Overview
    d. Actinic Illumination
    e. Exposure Tools
14. Module 14: Lithgroaphy 3 (Registration, Photomasks, RETs)
    a. Registration
    b. Photomasks
    c. Resolution Enhancement Techniques
    d. The Evolution of Optical Lithography
15. Module 15: Etch 1 (Basics, Wet Etch, Dry Etch)
    a. Etch Basics
    b. Etch Terminology
    c. Wet Etch Overview
    d. Wet Etch Chemistries
    e. Types of Dry Etch Processes
    f. Physics & Chemistry of Plasma Etching

Day 4

16. Module 16: Etch 2 (Dry Etch Applications and Equipment)
    a. Dry Etch Applications
    b. SiO2
    c. Polysilicon
    d. Al & Al Alloys
    e. Photoresist Strip
    f. Silicon Nitride
    g. Dry Etch Equipment
    h. Batch Etchers
    i. Single Wafer Etchers
    j. Endpoint Detection
    k. Wafer Chucks
17. Module 17: CVD 2 (PECVD)
    a. CVD Basics
    b. PECVD Equipment
    c. CVD Films
    d. Step Coverage
18. Module 18: Chemical Mechanical Polishing
    a. Planarization Basics
    b. CMP Basics
    c. CMP Processes
    d. Process Challenges
    e. Equipment
    f. Process Control

19. Module 19: Copper Interconnect, Low-k Dielectrics
    a. Limitations of "Conventional" Interconnect
    b. Copper Interconnect
    c. Cu Electroplating
    d. Damascene Structures
    e. Low-k IMDs
    f. Cleaning Cu and low-k IMDs
20. Module 20: Leading Edge Technologies & Techniques
    a. Process Evolution
    b. Atomic Layer Deposition (ALD)
    c. High-k Gate and Capacitor Dielectrics
    d. Ni Silicide Contacts
    e. Metal Gates
    f. Silicon on Insulator (SOI) Technology
    g. Strained Silicon
    h. Hard Mask Trim Etch
    i. New Doping Techniques
    j. New Annealing Techniques
    k. Other New Techniques
    l. Summary of Industry Trends

References:

Wolf, Microchip Manufacturing,
Doering & Nishi, Semiconductor Manufacturing Technology, 2nd ed.
Wolf, Silicon Processing, Vol. 4
Wolf, Silicon Processing, Vol. 1, 2nd ed.

IRPS

International Reliability Physics Symposium

2018 IEEE International Reliability Physics Symposium

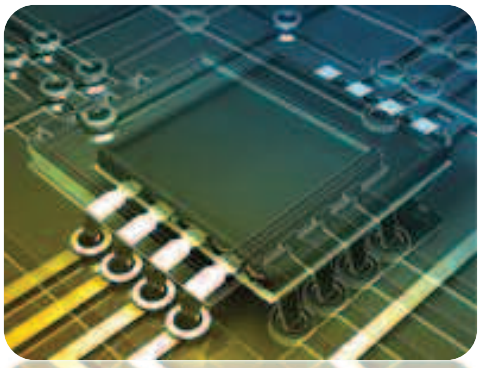
IEEE

March 11-15, 2018
Hyatt Regency San Francisco Airport
1333 Bayshore Highway
Burlingame, CA, USA 94010

Registration is available at www.irps.org

Chris Henderson, Semitracks President

Chris would be happy to meet with you and discuss any training needs you have. Contact him at henderson@semitracks.com anytime before the symposium!



Upcoming Courses

(Click on each item for details)

Failure and Yield Analysis
March 19 – 22, 2018 (Mon – Thur)
San Jose, California, USA

Semiconductor Reliability / Product Qualification
March 26 – 29, 2018 (Mon – Thur)
Portland, Oregon, USA

Failure and Yield Analysis
April 9 – 12, 2018 (Mon – Thur)
Munich, Germany

Wafer Fab Processing
April 9 – 12, 2018 (Mon – Thur)
Munich, Germany

Semiconductor Reliability / Product Qualification
April 16 – 19, 2018 (Mon – Thur)
Munich, Germany

CMOS, BiCMOS and Bipolar Process Integration
September 10 – 12, 2018 (Mon – Tue)
San Jose, California, USA

Feedback

If you have a suggestion or a comment regarding our courses, online training, discussion forums, or reference materials, or if you wish to suggest a new course or location, please call us at 1-505-858-0454 or Email us (info@semitracks.com).
To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered in the next newsletter, please contact Jeremy Henderson by Email (jeremy.henderson@semitracks.com).
We are always looking for ways to enhance our courses and educational materials.

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