Issue 73 February 2016

InfoTracks

Semitracks Monthly Newsletter

Underfills, Part 1

By Christopher Henderson

In this section we will discuss underfills and their use in the electronics assembly process. Underfills are a class of polymers used to help enhance the connection between the die and the substrate. With the advent of solder bumping and BGA packages came the need for underfills. First, we will discuss why underfills are needed. Next, we will discuss the underfill process. Finally, we will discuss the reliability of underfill materials.

BGA underfills are now commonly used for chip-on-board as well as BGA and Chip Scale Package mounting. The underfill helps to distribute the stress evenly across the die, making the solder joints more reliable. It can also provide mechanical strength to a portable system, such as a cell phone, PDA, or other portable device. Because the underfill holds the component rigidly in place on the board, it can also improve the electrical conductivity of the solder joints. Finally, underfills can be used to protect the surface of the die.

The electronics industry increasingly uses flip chips and chip-scale packages in electronic assemblies for portable devices. An early decision engineers must make is the choice of the underfill material. Underfills without filler particles flow more rapidly, but have higher coefficients of thermal expansion. Underfill with filler particles flow more slowly, but have lower coefficients of thermal expansion and better shock-absorbing properties. Several considerations are involved in the design of a board using flip chips or chip-scale packages that will be underfilled. One significant consideration is

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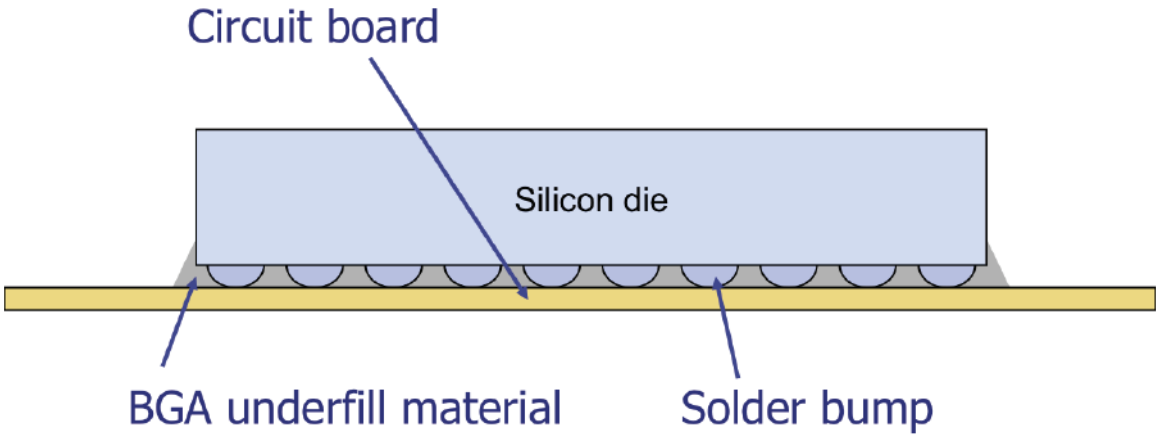
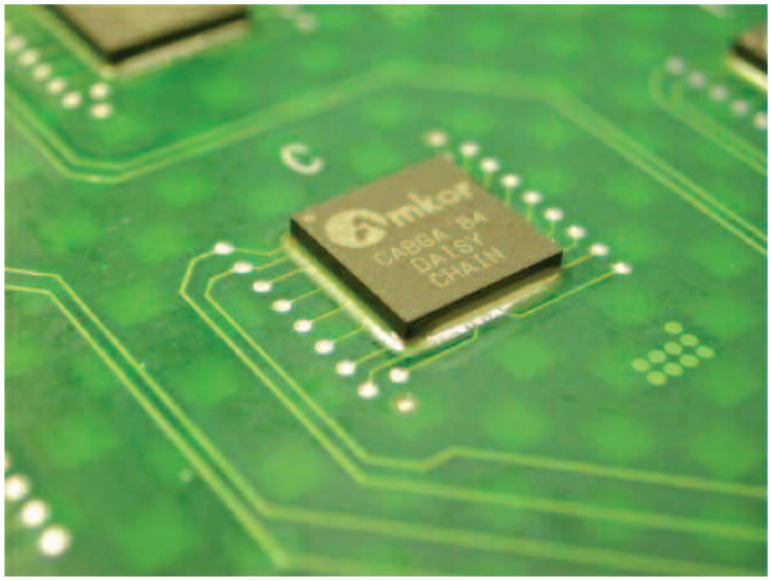
Semiconductor, Microelectronics, Microsystems, and Nanotechnology Training

component density. Components that are placed close to a component that is being underfilled may either draw fluid underfill away from the target component, or assist keeping the fluid underfill in place. Fluid underfill that flows to adjacent components generally causes no harm to the adjacent components, but it subtracts underfill from the precisely measured quantity delivered to the target component. Underfill that flows to adjacent components may also make rework far more difficult.





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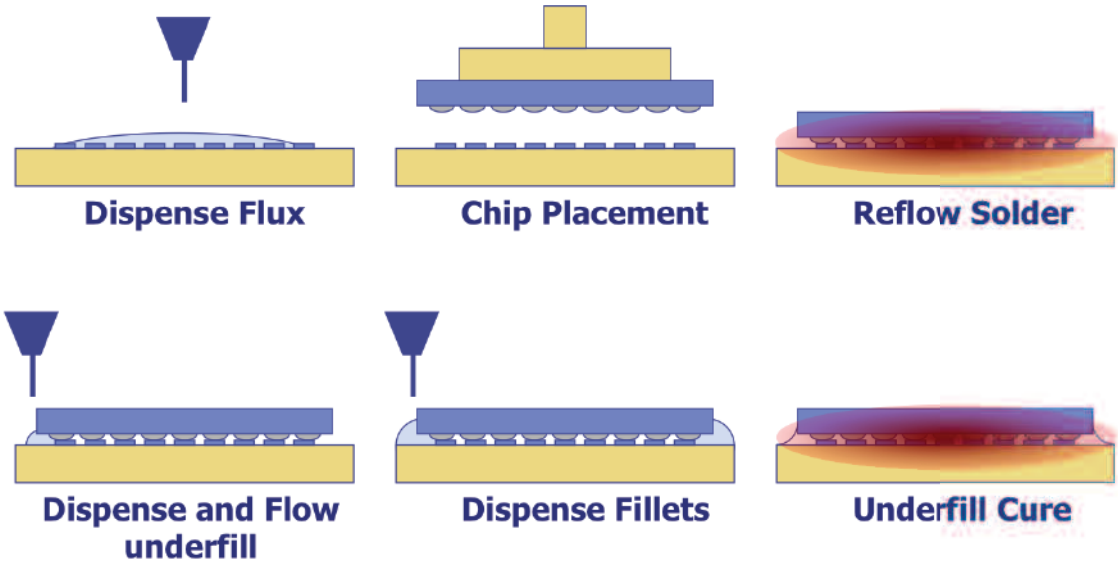
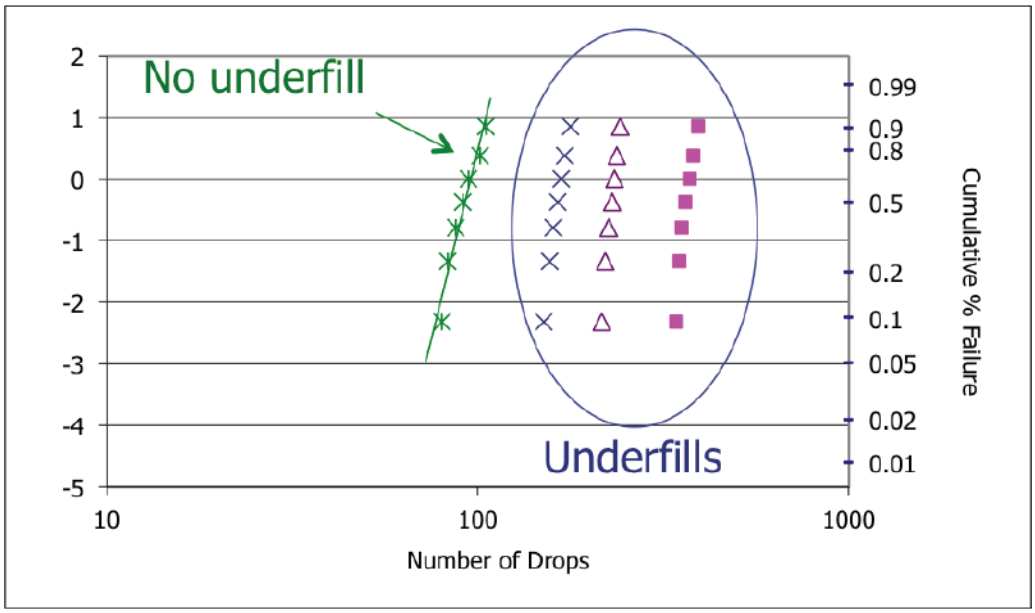
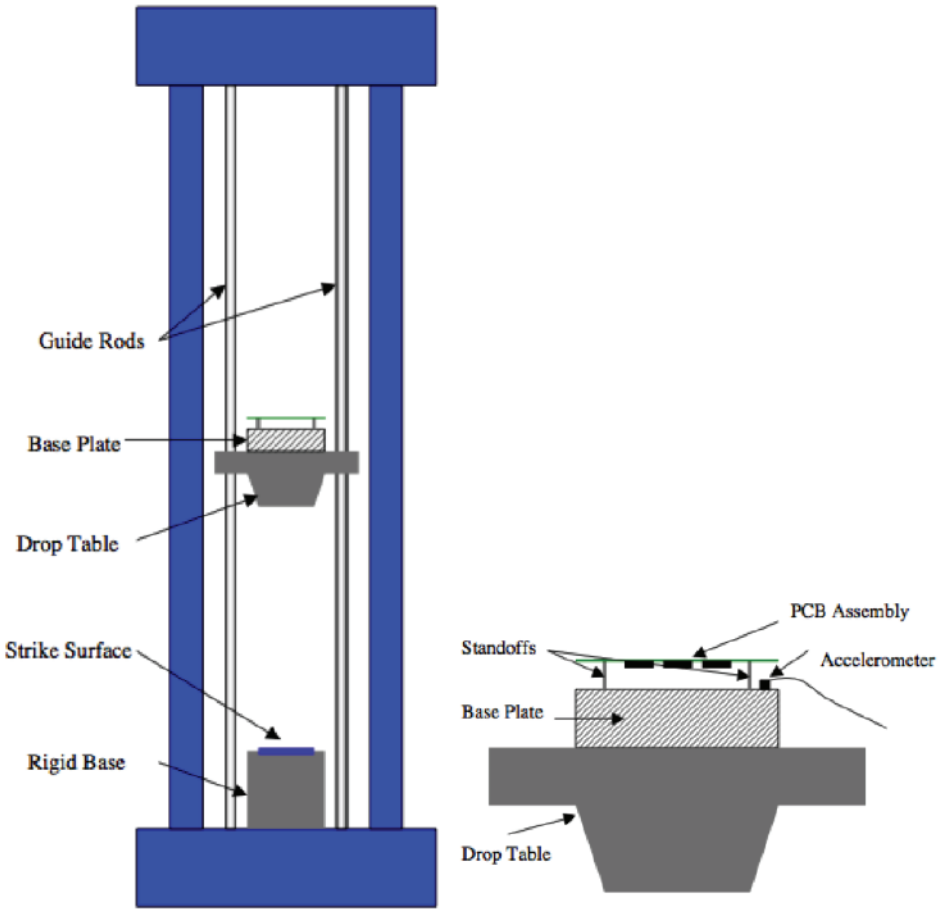
Underfill with filler particles flow more slowly, but have lower coefficients of thermal expansion and better shock-absorbing properties. Several considerations are involved in the design of a board using flip chips or chip-scale packages that will be underfilled. One significant consideration is component density. Components that are placed close to a component that is being underfilled may either draw fluid underfill away from the target component, or assist keeping the fluid underfill in place. Fluid underfill that flows to adjacent components generally causes no harm to the adjacent components, but it subtracts underfill from the precisely measured quantity delivered to the target component. Underfill that flows to adjacent components may also make rework far more difficult.



This diagram shows the basic ball grid array underfill process. First, one begins by dispensing flux on the surface of the substrate. This will help ensure the solder makes adequate contact to the solder pads on the board or substrate. Next, the chip is placed over the appropriate pads. Alignment is critical to help ensure a proper solder joint is formed. Next, the assembly is heated to reflow the solder. This can be done using hot air, infrared heating, vapor phase, or other methods. Next, the underfill is dispensed. There are two different methods for achieving a proper underfill. One is to dispense the epoxy at one end of the chip and allow capillary action to pull the epoxy under the entire part. The other method is to put epoxy on the chip before mounting it to the board or substrate. Many manufacturers are turning to the latter method, since the throughput is higher and the cost is approximately 60% less than the conventional capillary action method. After the underfill is dispensed, one can deposit fillets on the side to provide additional mechanical strength and help reduce stress. Finally, the epoxy is cured, resulting in an assembly that is mechanically strong.



One of the main reasons the electronics industry uses underfills is to improve the reliability of the solder joint. The underfill helps to distribute stress and hold the solder bump in compression to maintain a more permanent connection to both the board and the chip. Engineers use a standardized test from JEDEC known as the drop test to demonstrate reliability. The test involves placing the board assembly in various orientations on a base plate mounted to a drop table. A motor raises the drop table to specified heights depending on the service condition, and releases the drop table onto a rigid base, creating a large mechanical shock. The data in the chart above shows how an underfill will improve the reliability by a factor of 2 to 10.

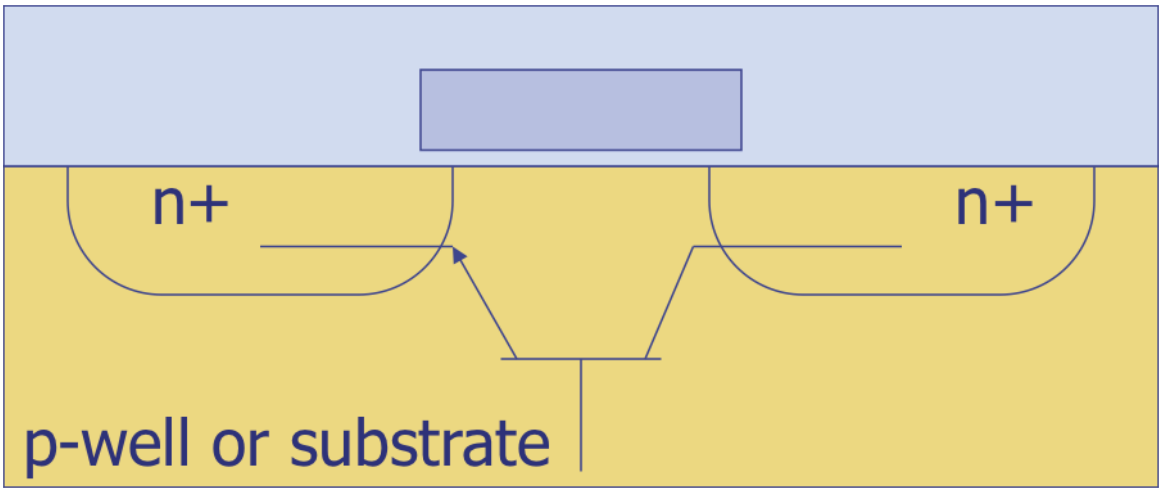


Technical Tidbit

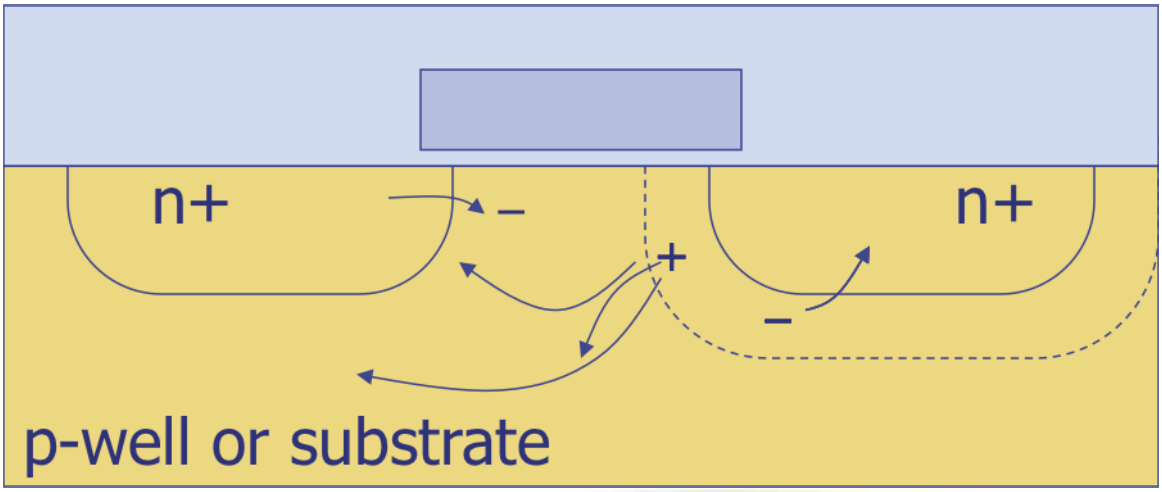
Snapback

Snapback is a less studied phenomenon, but has been receiving more attention recently as a component of ESD research.

Snapback is the forward-biasing of the parasitic npn transistor that exists in the n-channel MOSFET structure. This cross section shows the location of the parasitic npn structure.



The snapback phenomenon was first reported by Albert Ochoa and his colleagues at Sandia National Laboratories in 1983. They observed circuits entering a high current condition when exposed to an ESD event. The circuit configuration precluded the possibility of latchup, so they investigated it further. When an ESD pulse reaches the drain of an n-channel transistor, the avalanche voltage is exceeded. This generates hot carriers, a portion of which are injected into the oxide, and another portion of which are injected into the well. The drain voltage increases until the well voltage is greater than the turn-on voltage of the parasitic npn transistor. The source then injects carriers into the well, lowering the drain voltage and causing the device to go into a negative resistance region. If the drain voltage is greater than the snapback holding voltage, the device will continue to conduct current. If the drain voltage continues to increase, the transistor can be forced into second breakdown where the intrinsic carrier density exceeds the doping levels. Aluminum and silicon melting can ensure if the supply current remains connected and can deliver the current.



This diagram depicts the carrier flow during snapback. Initially, the drain avalanches along the entire perimeter. The hole current flows into the substrate and the electrons flow back into the drain. As the source becomes forward-biased, it begins to inject electrons in to the channel region. The bipolar current adds to the avalanche current near the source region. The drain-to-source voltage drops and the drain remains in avalanche only near the channel region. As the snapback event progresses, the focused drain avalanche current increases the emitter injection. The added carriers drop the resistance of the intrinsic base region and the substrate terminal current drops due to shunting by the base region into the emitter region.

Ask the Experts

Q: What is the biggest reliability risk for Light Emitting Diodes (LEDs)?

A: In general, allowing the LED to run too hot is the biggest reliability risk. Many important semiconductor degradation mechanisms in LEDs, like dark line defects and encapsulant yellowing, accelerate with temperature. Therefore, running the LED at as low a temperature as possible will help reduce the progression of these failure mechanisms, and lead to a longer lifetime and better reliability.

Global Semiconductor & Electronics Forum

March 9th-11th 2016
Shanghai Marriot Hotel City Centre
Shanghai, China

Semitracks will be attending the Global Semiconductor Forum in Shanghai, China. If you would like to talk with us regarding education and training programs, please send us an email at info@semitracks.com

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Registration is available at www.arena-international.com/gsef

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Semitracks will also be offering an **Introduction to Processing Course** just prior to the GSF meeting, on March 7-8. This course will give attendees an overview of the wafer fabrication and package assembly processes. It is a great way to get up-to-speed quickly on semiconductor manufacturing. For more information, please go to: **http://www.semi-tracks.com/courses/processing/introduction-to-processing.php**

Spotlight: Introduction to Processing

OVERVIEW

Semiconductor and integrated circuit developments continue to proceed at an incredible pace. The industry as a whole has gotten to this point of incredible complexity through the process of countless breakthroughs and developments in wafer fab processing. Today's wafer fab contains some of the most complex and intricate procedures ever developed by mankind. ***Introduction to Processing*** is a 2-day course that offers an overview look into the semiconductor manufacturing process, and the individual processing technologies required to make them. We place special emphasis on the basics surrounding each technique, and we summarize the current issues related to manufacturing the next generation devices. This course is a must for every manager, engineer and technician working in the semiconductor industry, using semiconductor components or supplying tools to the industry.

By focusing on the basics of each processing step and the issues surrounding them, participants will learn why certain techniques are preferred over others. Our instructors work hard to explain how semiconductor processing works without delving heavily into the complex physics and mathematical expressions that normally accompany this discipline.

Participants learn basic but powerful aspects about the semiconductor industry. This skill-building series is divided into three segments:

1. **Basic Processing Steps.** Each processing step addresses a specific need in IC creation. Participants learn the fundamentals of each processing step and why they are used in the industry today.
2. **The Evolution of Each Processing Step.** It is important to understand how wafer fab processing came to the point where it is today. Participants learn how each technique has evolved for use in previous and current generation ICs.
3. **Current Issues in Wafer Fab Processing.** Participants learn how many processing steps are increasingly constrained by physics and materials science. They also learn about the impact of using new materials in the fabrication process and how those materials may create problems for the manufacturers in the future.
4. **Current Issues in Assembly and Packaging.** Participants learn how packaging is a key enabler for semiconductor components. They also learn why we are seeing an explosion of different packaging types.

COURSE OBJECTIVES

1. The seminar will provide participants with an overview of the semiconductor industry and its technical issues.
2. Participants will understand the basic concepts behind the fundamental wafer fab processing steps.
3. The seminar will identify the key issues related to each of the processing techniques and their impact on the continued scaling of the semiconductor industry.
4. Participants will be able to identify the basic features and principles associated with each major processing step. These include processes like chemical vapor deposition, ion implantation, lithography, and etching.

5. Participants will understand how processing, reliability, power consumption and device performance are interrelated.
6. Participants will be able to make decisions about how to construct and evaluate processing steps for CMOS, BiCMOS, and bipolar technologies.
7. The seminar will provide an introduction to the packaging process and discuss the fundamental drivers behind the current developments in packaging.

INSTRUCTIONAL STRATEGY

By using a combination of instruction by lecture, classroom exercises, and question/answer sessions, participants will learn practical information on semiconductor processing and the operation of this industry. From the very first moments of the seminar until the last sentence of the training, the driving instructional factor is **application**. We use instructors who are internationally recognized experts in their fields that have years of experience (both current and relevant) in this field. The accompanying textbook offers hundreds of pages of additional reference material participants can use back at their daily activities.

COURSE OUTLINE

1. Raw Silicon Wafers
2. Ion Implantation
3. Thermal Processing
4. Contamination Monitoring and Control
5. Wafer Cleaning and Surface Preparation
6. Chemical Vapor Deposition
7. Physical Vapor Deposition
8. Lithography
9. Etch
10. Chemical Mechanical Polishing
11. Cu Interconnect and low-k Dielectrics
12. Leading Edge Technologies and Techniques
    a. ALD
    b. High-k gate and capacitor dielectrics
    c. Metal gates
    d. SOI
    e. Strained silicon
    f. Plasma doping
13. Overview of Semiconductor Packaging
    a. Purpose of the package
    b. Drivers
    c. Types of Packages
    d. Packaging Processes

For each of these modules, the following topics will be addressed:

1) fundamentals necessary for a basic understanding of the technique
2) its role(s) and importance in contemporary wafer fab processes
3) type of equipment used
4) challenges
5) trends

IRPS

International Reliability Physics Symposium

2016 IEEE International Reliability Physics Symposium

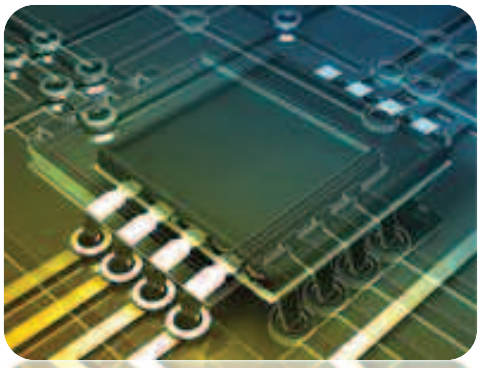
IEEE

April 17-21, 2016
Pasadena Convention Center
Pasadena, CA, USA

Registration is available at www.irps.org

Chris Henderson, IRPS General Chair

Chris would be happy to meet with you and discuss any training needs you have. Contact him at henderson@semitracks.com during the symposium!



Upcoming Courses

(Click on each item for details)

Packaging Failure and Yield Analysis
February 22 – 24, 2016 (Mon – Wed)
Manila, Phillippines

Introduction to Processing
March 7 – 8, 2016 (Mon – Tue)
Shanghai, China

CMOS, BiCMOS and Bipolar Process Integration
March 21 – 22, 2016 (Mon – Tue)
Albuquerque, New Mexico, USA

Wafer Fab Processing
March 29 – April 1, 2016 (Tue – Fri)
San Jose, California, USA

Failure and Yield Analysis
May 17 – 20, 2016 (Tue – Fri)
Munich, Germany

EOS, ESD and How to Differentiate
May 23 – 24, 2016 (Mon – Tue)
Munich, Germany

Semiconductor Reliability / Product Qualification
May 30 – June 2, 2016 (Mon – Thur)
Munich, Germany

Advanced Thermal Management and Packaging Materials
June 7 – 8, 2016 (Tue – Wed)
Albuquerque, New Mexico, USA

Semiconductor Reliability
July 11 – 13, 2016 (Mon – Wed)
Singapore

Feedback

If you have a suggestion or a comment regarding our courses, online training, discussion forums, or reference materials, or if you wish to suggest a new course or location, please call us at 1-505-858-0454 or Email us (info@semitracks.com).
To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered in the next newsletter, please contact Jeremy Henderson by Email (jeremy.henderson@semitracks.com).
We are always looking for ways to enhance our courses and educational materials.

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For more information on Semitracks online training or public courses, visit our web site!
http://www.semitracks.com

To post, read, or answer a question, visit our forums.
We look forward to hearing from you!