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Thermal Processing, Issues and Effects, Part 1

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Last month, we delved a little deeper into Thermal Processing, covering [Equipment and Processing]. This month we'll focus on some issues and effects associated with thermal processing. While thermal oxidation is primarily driven by temperature, there are second order effects that modify oxide growth. We will review these.

As a quick review, we show the basic Deal-Grove model here: where x is the oxide thickness, B is the parabolic rate constant, B over A is the linear rate constant, and tau is a factor to account for oxide present at the start of the oxidation. Let's take a closer look at the inputs to constants A and B.

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Semiconductor, Microelectronics, Microsystems, and Nanotechnology Training

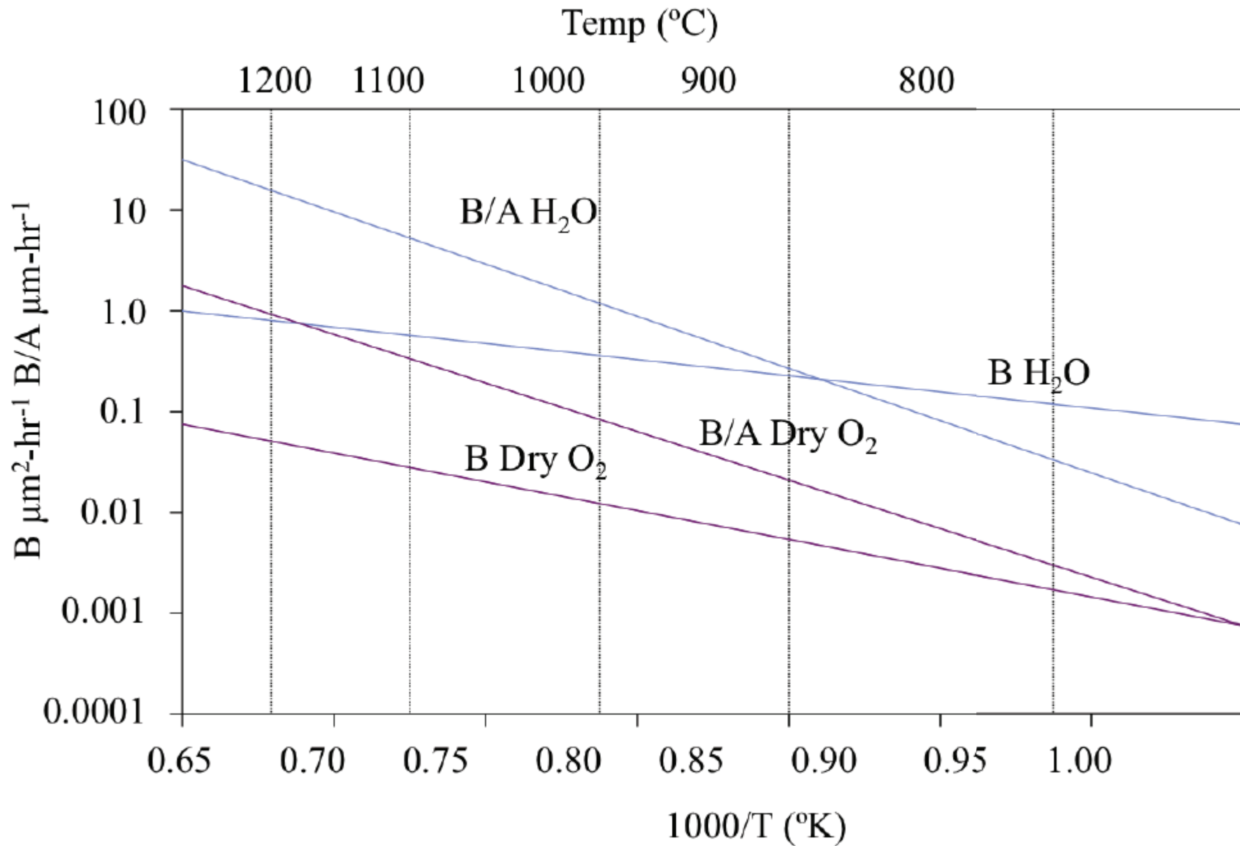
$$x_{ox}(t) = \frac{A}{2}\left[\left(1 + \frac{(t+\tau)}{(A^2/4B)}\right)^{1/2} - 1\right] \Rightarrow \frac{x_{ox}^{\;2}}{B} + \frac{x_{ox}}{B/A} = t + \tau$$

$$B = C_1 \exp\left(-\frac{E_1}{kT}\right), \frac{B}{A} = C_2 \exp\left(-\frac{E_2}{kT}\right)$$

Ambient	B	B/A
Dry O_2	C_1=7.72×10^{2}µm^{2}hr^{-1}	C_2=6.23×10^{6}µm$^-$hr^{-1}<111> C_2=3.71×10^{6}µm$^-$hr^{-1}<100>
	E_1=1.23eV	E_2=2.00eV
Wet O_2	C_1=2.14×10^{2}µm^{2}hr^{-1}	C_2=8.95×10^{7}µm-hr^{-1}<111> C_2=5.33×10^{7}µm-hr^{-1}<100>
	E_1=0.71eV	E_2=2.05eV
H_2O	C_1=3.86×10^{2}µm^{2}hr^{-1}	C_2=1.63×10^{8}µm$^-$hr^{-1}<111> C_2=9.70×10^{7}µm$^-$hr^{-1}<100>
	E_1=0.78eV	E_2=2.05eV

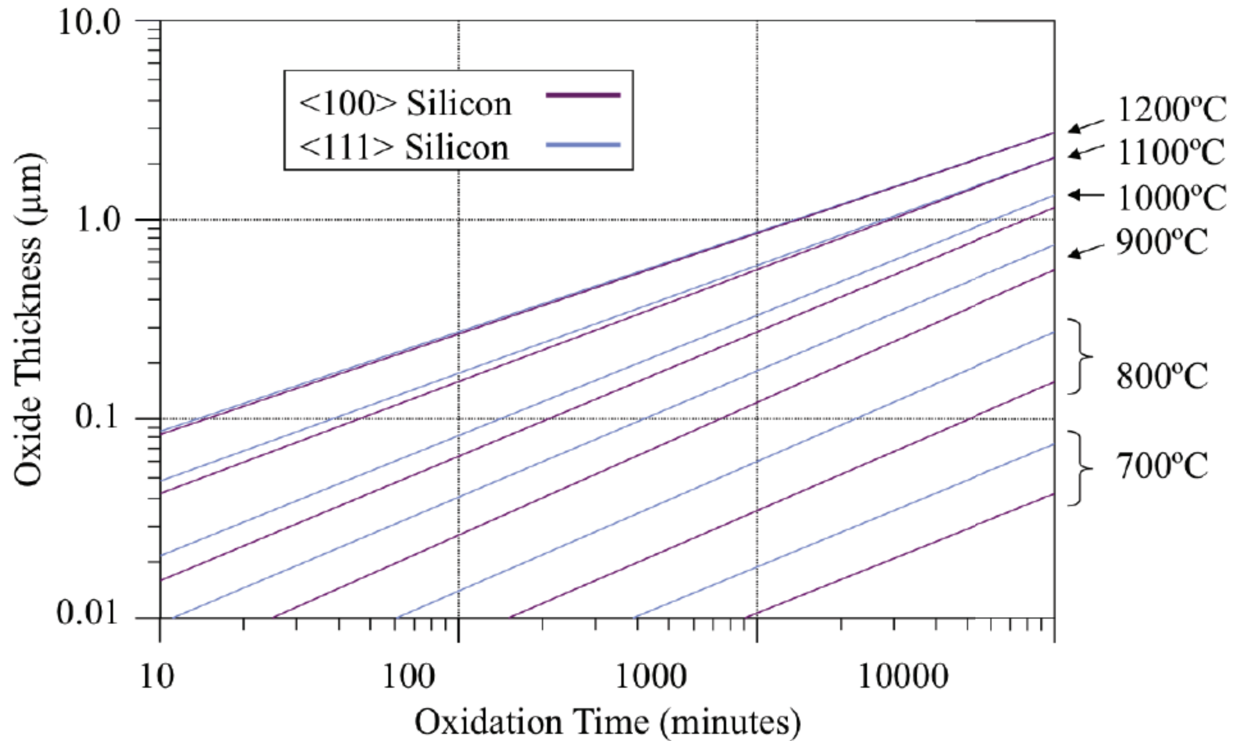
Rate constants describing silicon oxidation kinetics at 1 atm total pressure.

In order to solve for B and A, one must first know the values of C1, C2, E1, and E2. These values can be determined experimentally. This table shows values for the four constants under three different oxidation conditions: dry oxygen, wet oxygen, and steam. Wet oxygen is a condition where oxygen is bubbled through water prior to entering the oxidation furnace. These constants are for one atmosphere total pressure. The constant C2 is different depending on the crystal face exposed. In general, the <111> crystal face exposed results in a C2 constant that is about 1.68 times greater than with the <100> face exposed.

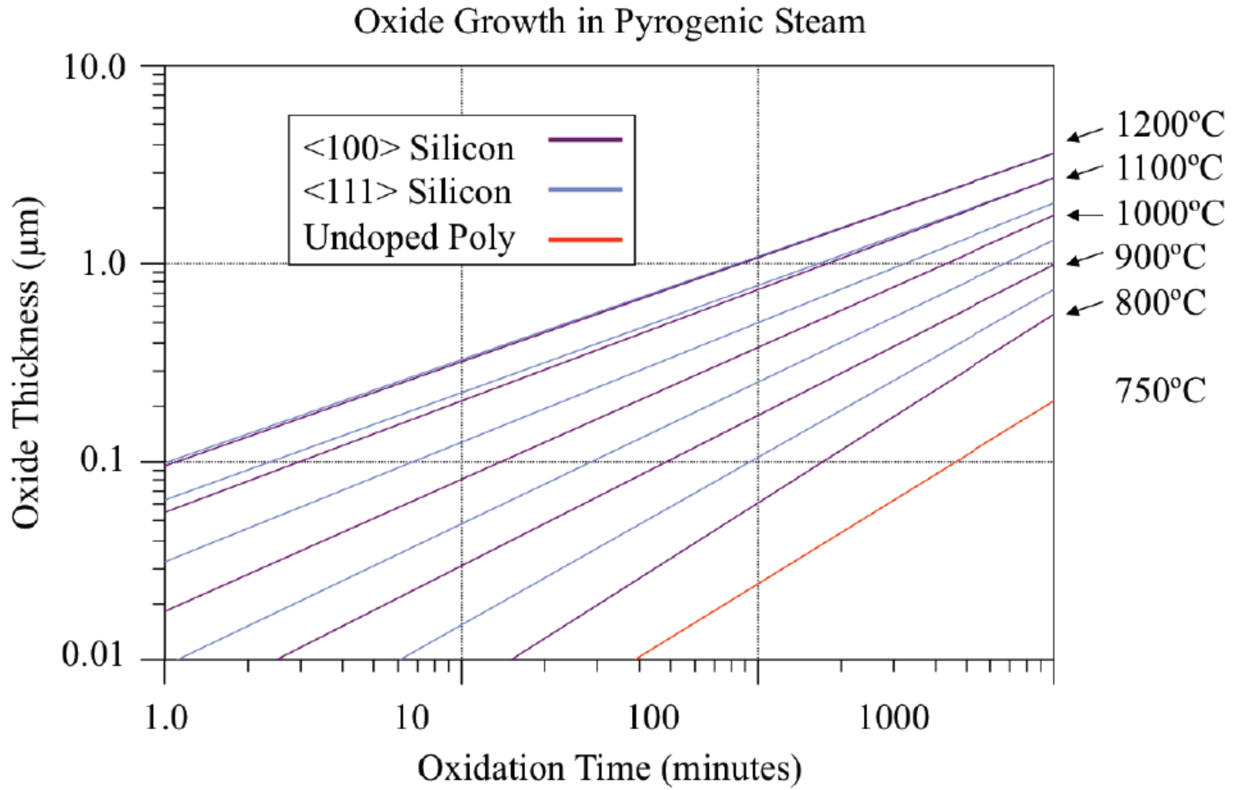


This slide shows the rate constants B and B over A as a function of temperature. In general the rate constants trend higher with increasing temperature. Also, the B over A rate constant has a higher slope than the B constant.

There are three basic factors which affect the oxidation process at the surface: temperature, availability of the oxidizing species, and the surface potential of the wafer. As is the case with many reactions, the rate of oxidation is greater at higher temperatures. The availability of oxygen at the surface is also important. Finally, the surface potential or surface energy can come into play. The crystal orientation, the silicon doping concentration, and any pre-oxidation surface treatments can affect the electro-chemical potential of the surface, increasing or decreasing the rate of reaction.



This graph shows the oxide growth in dry oxygen. The graph shows the oxide thickness as a function of oxidation time for several different growth temperatures. Notice that the oxide growth is approximately a straight line on a log-log plot. Also notice that the growth rates on <111> silicon are slightly faster than on <100> silicon. This is because the electro-chemical potential is slightly greater for the <111> face.

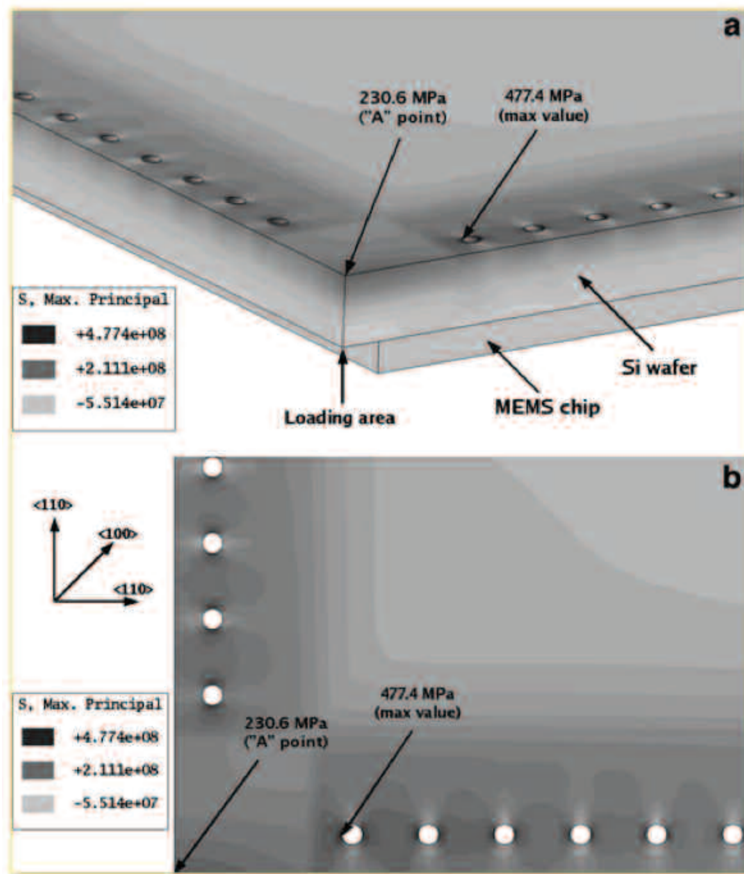


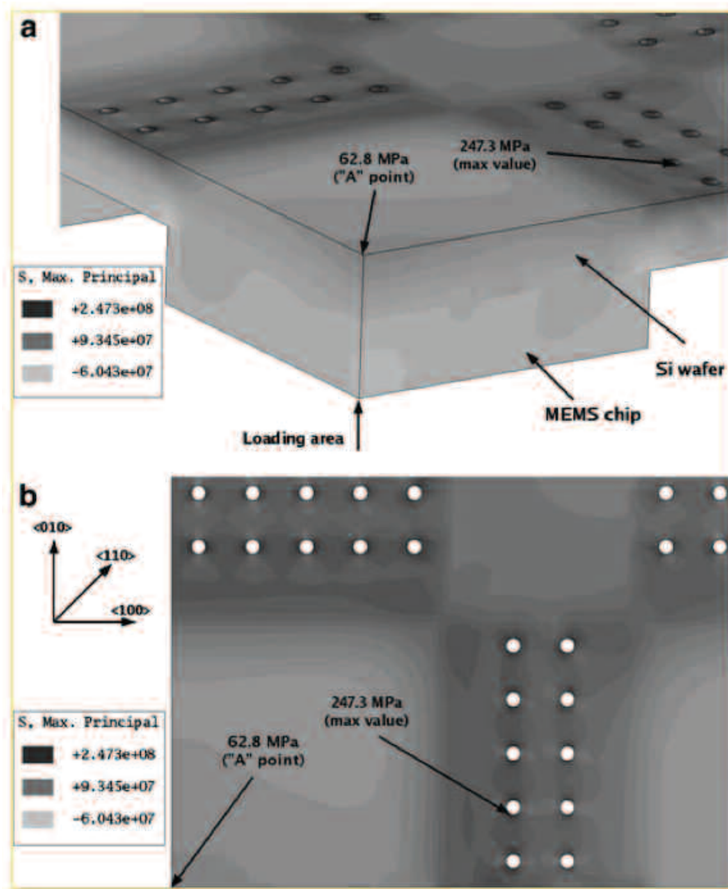
This graph shows the oxide growth in pyrogenic (pronounced pie-ro-jen-ik) steam. The graph shows the oxide thickness as a function of oxidation time for several different growth temperatures. Notice that the oxide growth is approximately a straight line on a log-log plot. The growth rates are about a factor of ten faster than shown on the previous slide in dry oxygen. Also notice that the growth rates on <111> silicon are slightly faster than on <100> silicon. This is because the electro-chemical potential is slightly greater for the <111> face. We also show a growth line for undoped polysilicon at 750°C.

Technical Tidbit

TSV Stresses

The stresses generated by the TSV not only affect the interconnect ends, but they also affect the stress in the silicon. In fact, sufficient stress is generated to result in transistor mobility variations. In today's nanometer-scale technologies, a slight variation in mobility in some transistor can result in the design not working. Researchers at CEA-LETI in France have modeled the effects of stress. Here are two examples of modeling work showing how the TSVs affect stress during temperature cycling, and the molding process.





In these examples, the silicon die with TSVs is stacked on top of a MEMS chip. Notice the high stress values at the corner, but even these are significantly less than the stress values associated with the maximum point in the vicinity of the TSVs. This requires coordination between the silicon chip designers and the packaging engineers – an activity we normally refer to as chip-package co-design. The result might mean the creation of Keep Out Zones (KOZs) for sensitive transistors.

Ask the Experts

Q: I have heard the term NSOL and NSOP. What do they mean?

A: NSOL and NSOP mean Non Stick On Lead and Non Stick On Pad respectively. Lead refers to the exposed leadframe, and Pad refers to the bond pads on the integrated circuit. This can happen for several reasons, but typically occurs when the die attach bake process releases volatile compounds, which coat the leadframe and bond pads. This can interfere with the bonding process, leading to a wire bond that doesn't bond correctly to the bond pad or lead frame.

Spotlight: Semiconductor Reliability

OVERVIEW

Semiconductor reliability is at a crossroads. In the past, reliability meant discovering, characterizing and modeling failure mechanisms and determining their impact on the reliability of the circuit. Today, reliability can involve tradeoffs between performance and reliability, assessing the impact of new materials, dealing with limited margins, etc. Analysis and experimentation is now performed at the wafer level instead of the packaging level. This requires knowledge of subjects like: design of experiments, testing, technology, processing, materials science, chemistry, and customer expectations. While reliability levels are at an all-time high level in the industry, rapid changes may quickly cause reliability to deteriorate. Your company needs competent engineers and scientists to help solve these problems. ***Semiconductor Reliability*** is a thtee- to five-day course that offers detailed instruction on a variety of subjects pertaining to semiconductor reliability. This course is designed for every manager, engineer, and technician concerned with reliability in the semiconductor field, using semiconductor components, or supplying tools to the industry.

Participants learn to develop the skills to determine what failure mechanisms might occur, and how to test for them, develop models for them, and eliminate them from the product.

1. **Overview of Reliability and Statistics.** Participants learn the fundamentals of statistics, sample sizes, distributions and their parameters.
2. **Failure Mechanisms.** Participants learn the nature and manifestation of a variety of failure mechanisms that can occur both at the die level and at the package level. These include: time-dependent dielectric breakdown, hot carrier degradation, electromigration, stress-induced voiding, moisture, corrosion, contamination, thermomechanical effects, etc.
3. **Qualification Principles.** Participants learn how test structures can be designed to help test for a particular failure mechanism.
4. **Test Strategies.** Participants learn the basics on how to test test structures, design screening tests, and how to perform burn-in testing effectively.

COURSE OBJECTIVES

1. The seminar will provide participants with an in-depth understanding of the failure mechanisms, test structures, equipment, and testing methods used to achieve today's high reliability components.
2. Participants will be able to gather data, determine how best to plot the data and make inferences from that data.
3. The seminar will identify the major failure mechanisms, explain how they are observed, how they are modeled, and how they are eliminated.
4. The seminar offers a variety of video demonstrations of analysis techniques, so the participants can get an understanding of the types of results they might expect to see with their equipment.
5. Participants will be able to identify basic test structures and how they are used to help quantify reliability on semiconductor devices.
6. Participants will be able to knowledgeably implement screens that are appropriate to assure the reliability of a component.
7. Participants will be able to identify appropriate tools to purchase when starting or expanding a laboratory

INSTRUCTIONAL STRATEGY

By using a combination of instruction by lecture, video, problem solving and question/answer sessions, participants will learn practical approaches to the failure analysis process. From the very first moments of the seminar until the last sentence of the training, the driving instructional factor is **application**. We use instructors who are internationally recognized experts in their fields that have years of experience (both current and relevant) in this field. The handbook offers hundreds of pages of additional reference material the participants can use back at their daily activities.

THE SEMITRACKS ANALYSIS INSTRUCTIONAL VIDEOS™

One unique feature of this workshop is the video segments used to help train the students. Reliability Analysis is a visual discipline. The ability to identify nuances and subtleties in graphical data is critical to locating and understanding the defect. Some tools output video images that must be interpreted by engineers and scientists. No other course of this type uses this medium to help train the participants. These videos allow the analysts to directly compare material they learn in this course with real analysis work they do in their daily activities.

COURSE OUTLINE

Day One (Lecture Time 8 Hours)

1. Introduction to Reliability
   a. Basic Concepts
   b. Definitions
   c. Historical Information
2. Statistics and Distributions
   a. Basic Statistics
   b. Normal Distribution
   c. Lognormal Distribution
   d. Weibull Distribution
   e. Exponential Distribution
   f. Which Distribution Should I Use?
   g. Data Handling

Day Two (Lecture Time 8 Hours)

3. Die-Level Failure Mechanisms
   a. Time Dependent Dielectric Breakdown
   b. Hot Carrier Damage
   c. Negative Bias Temperature Instability
   d. Electromigration
   e. Stress Induced Voiding

Day Three (Lecture Time 8 Hours)

4. Package Level Mechanisms
    a. Ionic Contamination
    b. Moisture/Corrosion
    c. Thermo-Mechanical Stress
    d. Thermal Stress/Cycling
5. Use Condition Mechanisms
    a. Electrical Overstress/ESD
    b. Radiation

Day Four (Lecture Time 8 Hours)

6. Test Structures and Test Equipment
    a. Test Structures
        i. Parametric Test Structures
        ii. Reliability Test Structures
        iii. Self-Stressing Test Structures
    b. Test Equipment
        i. Packaged Part Testing
        ii. Wafer Level Testing
7. Developing Screens, Stress Tests, and Life Tests
    a. Burn-In
    b. Life Testing
    c. HAST
8. Package Attach (Solder) Reliability
9. Board Level Reliability Mechanisms
10. Calculating Chip and System Level Reliability
11. Future Reliability Challenges

IRPS

International Reliability Physics Symposium

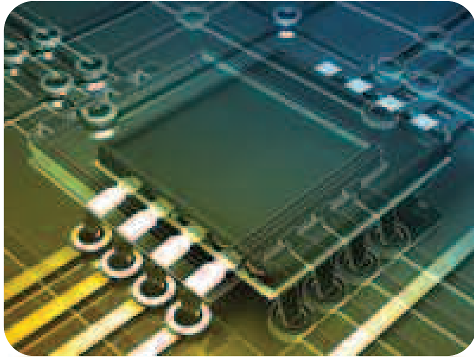
2015 IEEE International Reliability Physics Symposium

April 19-23, 2015
Hyatt Regency Monterey Resort & Spa
Monterey, CA, USA

Registration is available at www.irps.org

Chris Henderson, IRPS Vice General Chair

Chris would be happy to meet with you and discuss any training needs you have. Contact him at henderson@semitracks.com during the symposium!



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We are always looking for ways to enhance our courses and educational materials.

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To post, read, or answer a question, visit our forums.
We look forward to hearing from you!

Upcoming Courses

(Click on each item for details)

Wafer Fab Processing
March 16 – 19, 2015 (Mon – Thur)
San Jose, California, USA

Failure and Yield Analysis
April 27 – 30, 2015 (Mon – Thur)
Munich, Germany

Semiconductor Reliability
May 4 – 6, 2015 (Mon – Wed)
Munich, Germany

EOS, ESD and How to Differentiate
May 7 – 8, 2015 (Thur – Fri)
Munich, Germany