Issue 32 February 2012

InfoTracks

Semitracks Monthly Newsletter

Hi-K/Positive Bias Temperature Instability

By Christopher Henderson

In this section we'll cover the topic of positive bias temperature instability, or PBTI. PBTI primarily affects transistors that use high-k gate dielectrics. It is receiving more attention as leading edge manufacturers implement high-k metal gate transistor processes. We'll begin this section with an overview of the properties of high-k dielectrics. High dielectric constant materials behave somewhat differently than silicon dioxide, so it's important to understand how these differences affect transistor reliability. We'll then discuss positive bias temperature instability and cover the mechanism, how to model its behavior, and methods to mitigate the problem.

To understand why the industry is using high-k dielectrics in the leading edge devices, we need to back up a step. We are running into a fundamental barrier in transistor operation—a silicon dioxide gate dielectric cannot be scaled any further without serious problems. The gate must be scaled down to properly control the transistor channel behavior. By using ultrathin gate dielectrics, the leakage becomes too high. This means that these devices would not be suitable for any application where power is critical, such as portable applications. Even desktop and server applications are sensitive to this leakage as they raise power usage and generate excessive heat. That means we can't use oxide thickness as a method to increase capacitance. The solution is to replace the silicon dioxide with an insulating material that has a higher dielectric constant. This provides a higher capacitance, which in turn improves the transistor performance. Unfortunately hafnium-

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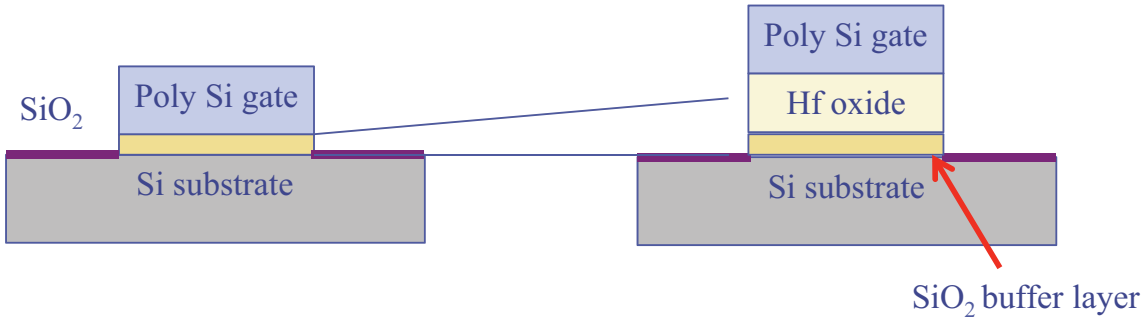
based materials do not bond well to silicon. Therefore we need a buffer layer that bonds both to silicon and to the hafnium oxide dielectric. The best material to do this is silicon dioxide, like we show here.

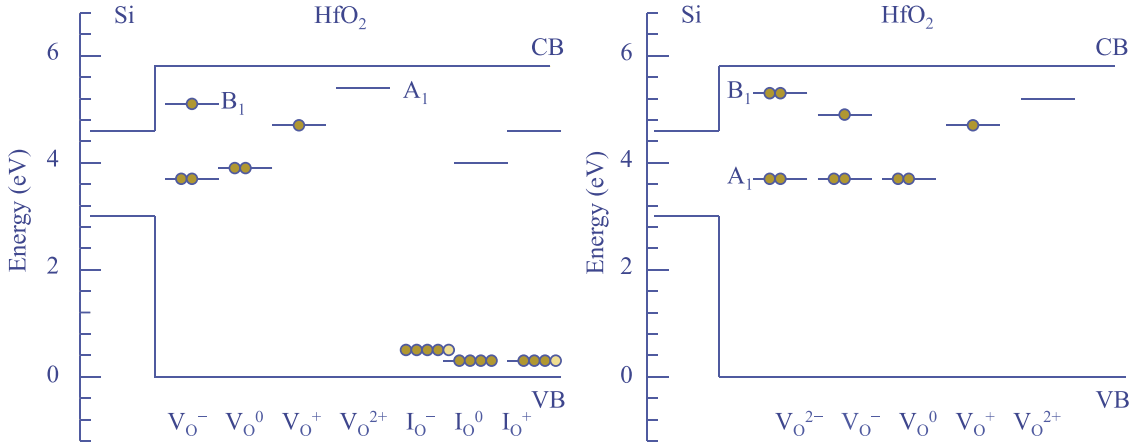


As of this writing, high-k dielectrics are relatively new in production and still not completely understood. This can be seen in the research studies involving high-k dielectric breakdown. In one model, researchers assume that traps are generated in the high-k layer. Breakdown of the high-k layer then triggers a breakdown of the entire dielectric stack. This model is supported by researchers who have observed what they thought to be trap generation in the high-k material, or at least assumed that was the case. In another model, researchers assume that traps are generated in the interface layer. Therefore, a breakdown of the interface layer triggers the stack breakdown. Researchers who have not observed trap generation in the high-k layer support this model. There are some additional factors that make it difficult for researchers. For instance the stack asymmetry will increase the problem complexity. The silicon dioxide is only on one side of the high-k dielectric, so the response will be different for positive and negative bias. Manufacturers use different materials for their high-k dielectrics, including non-hafnium oxides like aluminum oxide, zirconium oxide, and lanthanum oxide. They also use different deposition techniques like atomic layer deposition, metallorganic chemical vapor deposition, and plasma enhanced chemical vapor deposition. Furthermore, even high-k dielectrics deposited the same way can be different due to slight differences in pressure, temperature, and material crystallization processes. So far, companies have only had a few learning cycles to optimize their high-k processes. Since all of these layers being studied by researchers are different, why wouldn't their reliability be different as well?

Several manufacturers introduced hafnium-based high-k dielectrics at the 45-nanometer CMOS technology node as a way to reduce gate leakage while maintaining an aggressive electrical oxide thickness or EOT. The penalty for doing this is that there are defects intrinsic to the high-k material, which leads to undesired transport through the dielectric and trapping-induced instability. These fast, reversible charge trapping processes are active in high-k, never observed before in silicon dioxide. This means that threshold voltage instability occurs even at time-zero. Researchers refer to this behavior as hysteresis. There is charge trapping during conventional DC measurements that prevents evaluation of intrinsic films. It also means that there is a need for fast measurement techniques. The complex nature of a multi-layer gate stack dielectric makes understanding phenomena more challenging. For example, is a time zero mobility degradation observed through DC characterization due to charge trapping in the high-k layer or driven by interface properties? The scientific community is still rigorously researching the exact physical and chemical nature of electron traps in the hafnium oxide – silicon oxide structure. The results of ab initio calculations and experimental studies based on electron spin resonance, or ESR measurements

have pointed to oxygen vacancies and interstitial oxygen atoms as possible defects controlling the threshold voltage instability. The trap characteristics obtained from time-resolved measurements and defect spectroscopic techniques appear to match O-vacancy defects. Nearby we show data on oxygen vacancies in hafnium oxide materials from two different researchers. These data were obtained through spectroscopic measurements. The oxygen vacancy can have five states (2 minus, 1 minus, neutral, 1 plus, or 2 plus). The Vs represent vacancies, and the Is represent interstitials. The lines represent states, and the dots represent the electrons occupying the state. For the negative states, one can see that an extra level is pulled down from the conduction band. Notice the states near the midgap; these will interfere with Fermi level producing a phenomenon known as Fermi Level pinning.

Oxygen vacancy and interstitials in HfO_2 in various charge states



J. Roberson, Rep. Prog. Phys. Vol. 69, 2006
Tse et. al., Microel. Eng., Vol. 84, (2007), p. 663

With the introduction of high-k dielectrics, the phenomenon of positive bias temperature instability has surfaced. Researchers have observed electron trapping and detrapping. This action is quite fast, and has an impact on reliability assessment. There is also instability in the threshold voltage with respect to time. The effect appears to be logarithmic and follows the Power Law. It also appears to have a saturation effect, but researchers are not in complete agreement on these characteristics. Researchers also disagree as to whether there are pre-existing traps, stress-induced traps, or other defects that generate this positive bias. Researchers also disagree about the role of the interface layer, as well as the stress scheme for accurate lifetime projection at use conditions.

Let's move on and discuss models for Positive Bias Temperature Instability. Accurate PBTI lifetime projections require time, voltage, and temperature dependencies of the threshold voltage shift to be accurately determined. Let's begin with the time dependence.

$$\Delta V_T \approx t^n$$

The Power Law has been extensively used for modeling NBTI induced threshold voltage instability and has also been found to fit PBTI data in high-k stacks for long-term stress. An accurate extraction of the time power exponent is critical for End-Of-Life projections and requires use of fast threshold voltage measurement methods. The exponential law has also been proposed for modeling PBTI time dependency and predicts a saturation level of the shift, or ΔV_{max}, for long stress times.

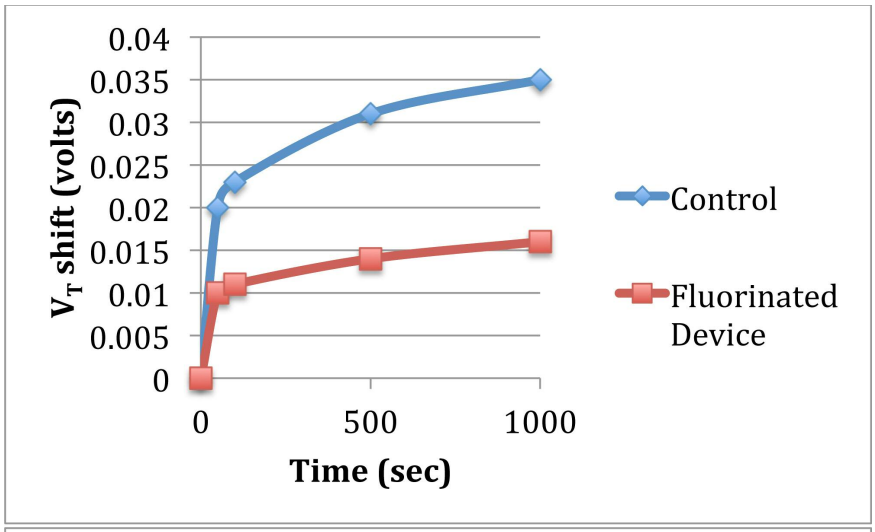
$$\Delta V_T \approx \Delta V_{\max} \approx \left(1 - e^{\frac{-t}{\tau}\beta}\right)$$

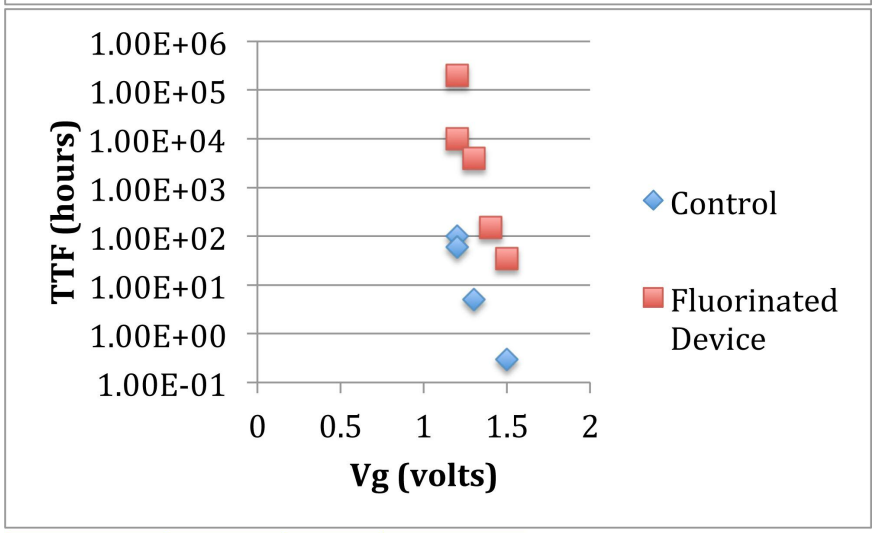
The exponential law may be an optimum modeling choice if electron trapping is the only mechanism determining VT instability and no new traps are created during stress. Caution needs to be exercised to ensure that VT shift saturation levels are not an artifact of relaxation phenomena due to "slow" VT measurements.

There are some techniques to mitigate the effects of PBTI. To first order, PBTI is reduced as the thickness of the high-k layer is reduced. Several researchers have confirmed this behavior. This is because the number of electron traps is reduced for a physically thinner stack. Chad Young was able to verify that the threshold voltage shift is reduced if trapping occurs within the bulk of the high-k dielectric. Scientists at TI postulated that a change in the physical structure, thought to be suppressed crystallization, for thinner gate stacks results in reduced trap densities leading to reduced instability. Engineers have also demonstrated effective ways of minimizing PBTI through process optimization. These improvements have been demonstrated although exact physics behind these effects are still not clear. For instance, in hafnium oxide versus hafnium silicate films, the threshold voltage instability is significantly reduced in hafnium silicate stacks compared to that observed in hafnium oxide stacks. Also, PBTI significantly increases as the hafnium content in the high-k increases. In the case of metal gate versus poly gate, process engineers observe a smaller instability in metal gate based high-k dielectrics like titanium nitride compared to polysilicon gates.

Another interesting effect is that of nitrogen on PBTI. Process engineers have found that the threshold voltage instability improves with increasing content of nitrogen in the stack, and the improvement is more significant when nitrogen is placed further away from silicon substrate. Researchers theorize that the incorporation of nitrogen passivates the oxygen vacancies. Researchers are now looking for further evidence that oxygen vacancies constitute the origin of instability. Fluorine also has an effect on PBTI — theoretical calculations have suggested that fluorine potentially passivates oxygen vacancies most efficiently. Researchers have also demonstrated that fluorination of hafnium based dielectric results in significant improvement of PBTI lifetime and SILC effect reduction. Here is some data from Tseng showing the improvement in PBTI by incorporating fluorine. The details for the control and fluorinated device are shown in the table at the upper right. Notice in the graph on the upper left that the threshold

voltage shift is significantly reduced for the fluorinated device. Also in the lower left, the time to failure for a given device is much longer with the fluorinated device. This gives orders of magnitude lifetime improvement for the fluorinated gate stack.





Device	EOT (A)	V_{tn} (V)	SSn (mV/dec)
Control	12.4	0.23	74
Fluorinated Device	12.6	0.24	63

In conclusion, positive bias temperature instability is a challenging reliability issue for high-k dielectrics in CMOS devices. A variety of techniques are used to characterize PBTI in today's circuits. It is important to use fast measurement techniques to help determine the slope as electrons move in and out of some traps quite quickly. There are rudimentary PBTI models, but these models need improvement. This is especially true with regards to long term instability and defect generation mechanisms. Finally, an improved understanding of PBTI should lead to improvements process optimization techniques for minimizing this reliability problem.

Technical Tidbit

Multi-Level Cells in Non-volatile Memories

A technique for increasing Flash memory density is multi-level cells. If one can accurately control the amount of charge on the floating gate, it can be parsed into four or more levels, rather than the standard two levels. In NOR flash memories, channel hot electron programming, under proper conditions, gives a linear relationship with unit slope between programming gate voltage (V_{GP}) and the threshold voltage variation, independent of cell parameters. Figure 1 shows ΔV_T as a function of the programming voltage for three different channel lengths. One can also plot very similar data in which the number of pulses is used in lieu of the programming voltage. In theory, one could place any given amount of charge on a gate to produce a large amount of possible states, but the current through the cell transistor would be increasingly difficult to distinguish between another.

Given this linear relationship, one can devise a series of gate programming voltages to program the cells with different amounts of charge to yield distinct levels within the cell. Figure 2 shows an example of the control-gate voltage pulses. An alternative approach is to use multiple pulses to program the level. While this simplifies the high voltage circuitry, it requires longer writing such a device, as multiple pulses must be used.

The cell current, obtained in reading conditions, can be compared with several currents provided by suitable reference cells. In Figure 3 we show three reference cells. The comparison values are converted to a binary code, whose content can be 11, 01, 10, or 00, due to the multilevel format of the memory. MSB is the most significant bit, and LSB is the least significant bit.

Figure 4 shows the threshold voltage distribution for 2-bit per cell device as compared to the standard 1-bit per cell device. Notice that there is significant margin in the 1-bit per cell device. In the 2-bit per cell device, there is considerably less margin. Notice also that the 11, 10, and 01 cell distributions give rise to different current distributions, measured at fixed read voltage, while the 00 cell distribution does not drain current as well as the programmed level of a standard 1-bit per cell device.

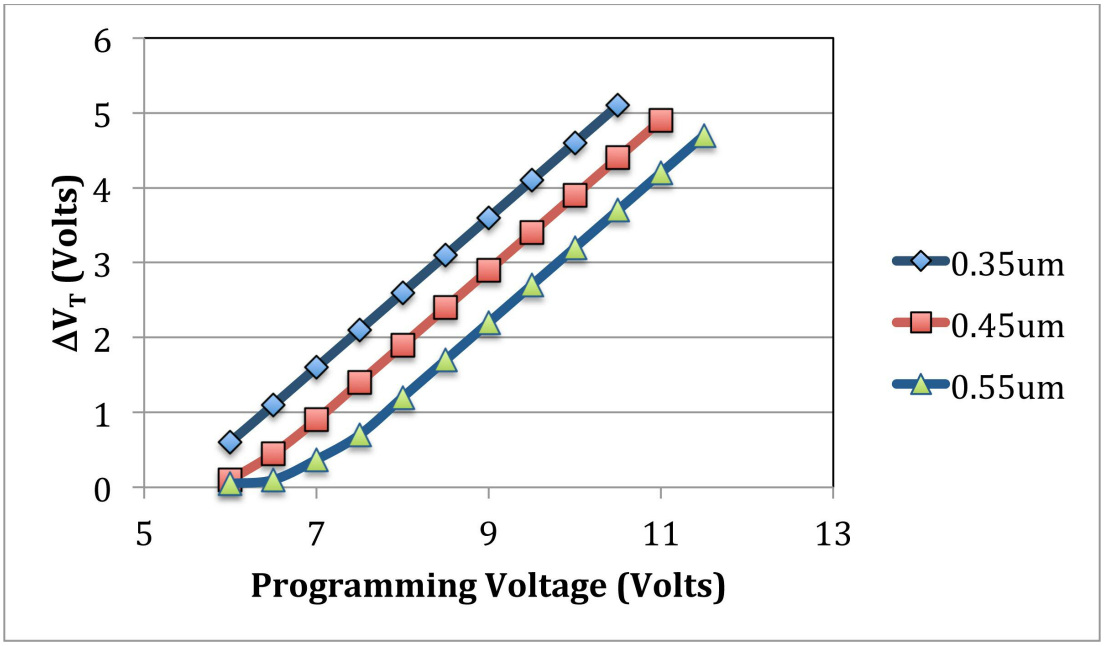


Fig. 1. Showing the linear relationship between programming voltage and cell threshold voltage, given a fixed drain voltage and pulse duration.

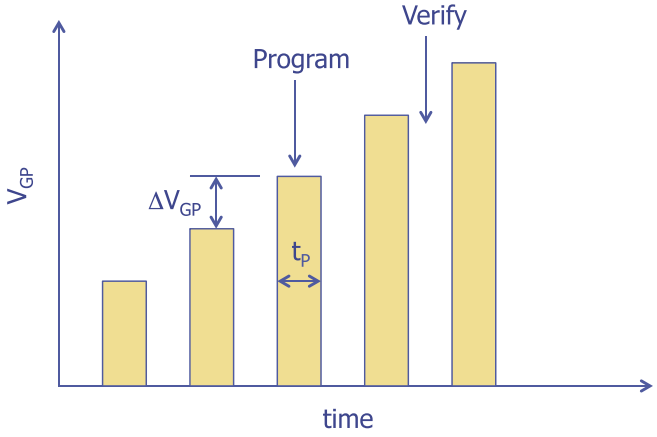


Fig. 2. Programming pulses for an MLC non-volatile memory.

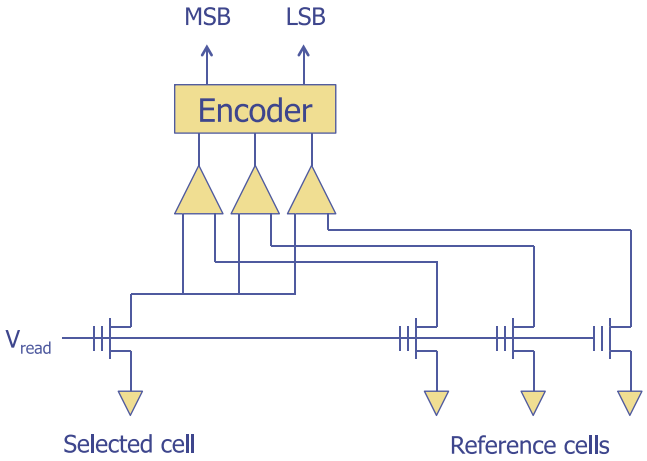


Fig. 3. Parallel sensing architecture for an MLC non-volatile memory.

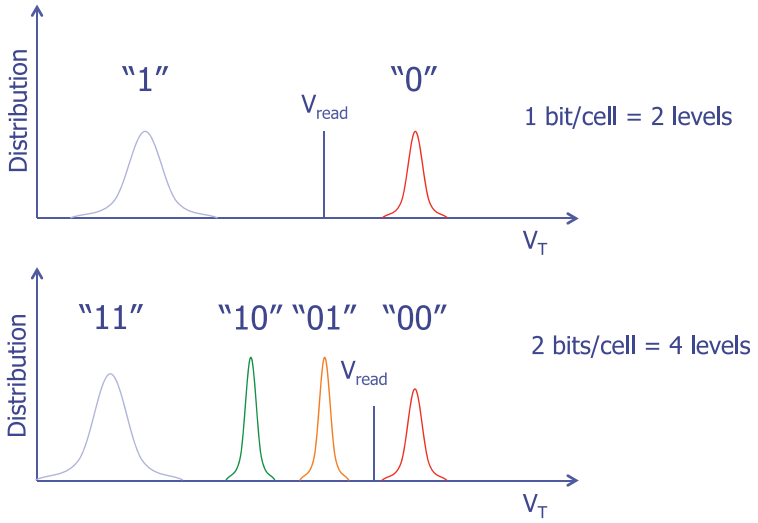
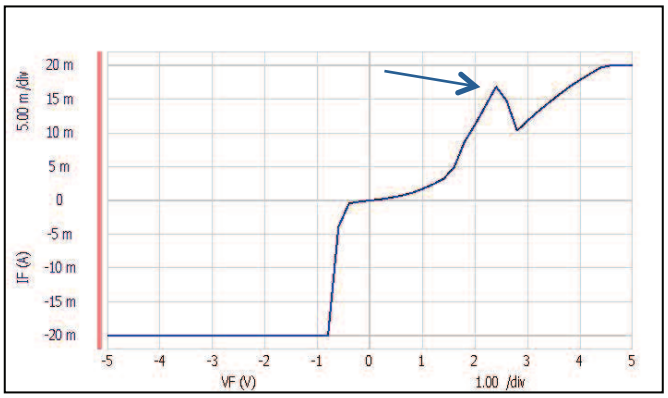


Fig. 4. 1- and 2-bit/cell distributions.

Ask the Experts

Q: I am seeing an I-V curve for an IC between VDD and GND that looks like this (see figure below). What creates the momentary drop in the upper right?



A: Several things might cause this behavior. One item you might want to check is to see if you have good continuity. Intermittent continuity could create this type of curve. A second possibility (more likely) is that you are attempting to power up a device without properly tying the input pins to either ground or VDD. You should tie all floating inputs to either ground or VDD to prevent unstable leakage during power-up. A third possibility is that the IC is experiencing some type of internal bus contention at lower voltages. One side of a bus may power up into a state opposite the other side of the bus, causing increased current. This can then resolve itself as the voltage increases on the internal components.

Spotlight on our Courses: Semiconductor Die/Wafer Level Reliability

One of our most popular courses, Semiconductor Reliability, is coming up in a few weeks in San Jose (March 12 – 14). Many people ask what we cover in the course, so we thought it would be appropriate to give our readers a more in-depth look at the outline and goals of the course. Keep reading for the details.

OVERVIEW

Semiconductor reliability is at a crossroads. In the past, reliability meant discovering, characterizing and modeling failure mechanisms and determining their impact on the reliability of the circuit. Today, reliability can involve tradeoffs between performance and reliability, assessing the impact of new materials, dealing with limited margins, etc. Analysis and experimentation is now performed at the wafer level instead of the packaging level. This requires knowledge of subjects like design of experiments, testing, technology, processing, materials science, chemistry, and customer expectations. While reliability levels are at an all-time high level in the industry, rapid changes may quickly cause reliability to deteriorate. Your company needs competent engineers and scientists to help solve these problems. Semiconductor Die/Wafer Level Reliability is a 3-day course that offers detailed instruction on a variety of subjects pertaining to semiconductor reliability. This course is designed for every manager, engineer, and technician concerned with reliability in the semiconductor field, using semiconductor components, or supplying tools to the industry.

Participants learn to develop the skills to determine what failure mechanisms might occur, and how to test for them, develop models for them, and eliminate them from the product.

1. **Overview of Reliability and Statistics.** Participants learn the fundamentals of statistics, sample sizes, distributions and their parameters.
2. **Failure Mechanisms.** Participants learn the nature and manifestation of a variety of failure mechanisms that can occur both at the die level and at the package level. These include time-dependent dielectric breakdown, hot carrier degradation, NBTI, PBTI, electromigration, stress-induced voiding, contamination, retention, charge loss, etc.
3. **Test Structures.** Participants learn how test structures can be designed to help test for a particular failure mechanism.
4. **Test Strategies.** Participants learn the basics on how to test test-structures, design screening tests, and how to perform wafer level testing effectively.
5. **Design for Reliability.** Participants learn the developments occurring in DFR at the transistor, gate, block, and chip level.

COURSE OBJECTIVES

1. The seminar will provide participants with an in-depth understanding of the failure mechanisms, test structures, equipment, and testing methods used to achieve today's high reliability components.

2. Participants will be able to gather data, determine how best to plot the data and make inferences from that data.
3. The seminar will identify the major failure mechanisms, explain how they are observed, how they are modeled, and how they are eliminated.
4. The seminar offers a variety of video demonstrations of analysis techniques, so the participants can get an understanding of the types of results they might expect to see with their equipment.
5. Participants will be able to identify basic test structures and how they are used to help quantify reliability on semiconductor devices.
6. Participants will be able to understand and communicate design-for-reliability needs and goals to the designers and customers.
7. Participants will be able to identify appropriate tools to purchase when starting or expanding a laboratory.

INSTRUCTIONAL STRATEGY

By using a combination of instruction by lecture, video, problem solving and question/answer sessions, participants will learn practical approaches to the failure analysis process. From the very first moments of the seminar until the last sentence of the training, the driving instructional factor is **application**. We use instructors who are internationally recognized experts in their fields that have years of experience (both current and relevant) in this field. The handbook offers hundreds of pages of additional reference material the participants can use back at their daily activities.

THE SEMITRACKS ANALYSIS INSTRUCTIONAL VIDEOS™

One unique feature of this workshop is the video segments used to help train the students. Reliability Analysis is a visual discipline. The ability to identify nuances and subtleties in graphical data is critical to locating and understanding the defect. Some tools output video images that must be interpreted by engineers and scientists. No other course of this type uses this medium to help train the participants. These videos allow the analysts to directly compare material they learn in this course with real analysis work they do in their daily activities.

COURSE OUTLINE

Day One (Lecture Time 8 Hours)

1. Introduction to Reliability
   a. Basic Concepts: Here we identify the goals of reliability studies/qualification and relate it to overall chip quality.
   b. Definitions: We define the top-level terms and definitions used in reliability physics.
   c. Historical Information: We discuss the origins of the study of physics of failure and trace it through the study of physical mechanisms, fundamental materials properties, design for reliability to today's activities in reliability where one must trade off performance, reliability and cost.

2. Statistics and Distributions
   a. Basic Statistics: We identify the basic statistics used for reliability calculations and define the commonly used terms.
   b. Distributions: We discuss the major distributions used in semiconductor reliability and in which situations to use them.
      i. Normal Distribution
      ii. Lognormal Distribution
      iii. Weibull Distribution
      iv. Exponential Distribution
   c. Which Distribution Should I Use?: We identify areas where choosing the correction distribution is important and how to do so.
   d. Data Handling: We discuss how to take data in such way as to maximize the odds of success.
   e. Acceleration: We show how to make determinations of failure rates based on acceleration parameters and stress conditions.
   f. Sample Size: We discuss the formula for calculating sample sizes need to demonstrate intended reliability levels.

Day Two (Lecture Time 8 Hours)

3. Failure Mechanisms
   a. Time Dependent Dielectric Breakdown
      i. Fundamental Parameters: We discuss the fundamental parameters and issues regarding making TDDB measurements.
      ii. Models (area, activation energies): We discuss the most widely used models in the industry and their advantages and disadvantages.
      iii. Soft Breakdown: We show how today's ICs fail more from soft breakdown and the challenges that causes in making reliability predictions.
      iv. Methods to improve TDDB: We discuss methods to improve TDDB ranging from process-related improvements to design techniques.
      v. BEOL TDDB: We discuss the mechanism of BEOL dielectric failure and the models to quantify its impact.
      vi. Exercises: We work some exercises to calculate TDDB reliability.
   b. Hot Carrier Damage
      i. Fundamental Parameters: We discuss the history and fundamental parameters associated with hot carriers.
      ii. Models: We cover the models used to calculate reliability for hot carrier degradation.
      iii. Effects in Modern ICs (stress liners, SiGe channel, HKMG): We discuss the impact of stress liners, High-K metal gate, and silicon-germanium channels on hot carriers.
      iv. AC effects: We describe the differences between DC and AC hot carrier lifetimes and how AC is more important to monitor.
   c. Negative Bias Temperature Instability
      i. Models: We discuss the Reaction-Diffusion model and how it can be used to calculate reliability.

ii. Recovery effect: We describe the recovery effect that occurs with NBTI and how it can change the outcome of the reliability analysis.
iii. Methods to reduce NBTI: We discuss both process and design techniques for reducing NBTI.
iv. Measurement techniques: We briefly introduce ultrafast or "on the fly" measurement techniques for NBTI.

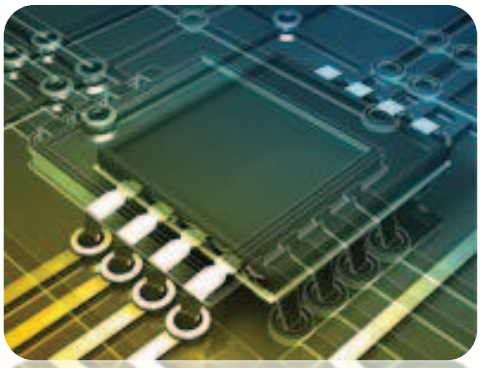
d. Positive Bias Temperature Instability
   i. Models: We describe the model development occurring for this mechanism.
   ii. Recovery effect: PBTI and NBTI both exhibit a recovery effect. We discuss how they are similar and how they are different.
   iii. Properties associated with HKMG: We discuss the High-K metal gate interface with itself and the silicon and how that affects the behavior of PBTI.
   iv. Methods to reduce PBTI: We describe process and design techniques for reducing PBTI.
   v. Exercises: We work several exercises for both NBTI and PBTI reliability calculations.
e. Retention/Charge Loss Mechanisms: We briefly cover memory-specific failure mechanisms like retention and charge loss.
f. Electromigration
   i. Mechanism: We describe the basic mechanism and the conditions that affect electromigration
      1. Atomic Flux
      2. Stress Gradients
      3. Surface Tension
   ii. Materials: We show the problems that occur both with aluminum and copper metallization. We show how the metal properties, along with the surrounding layers and dielectrics, affect its behavior.
      1. Aluminum and Copper effects
      2. Grain size
      3. Barrier and seed layers
      4. Surrounding dielectric effects
   iii. Exercises: We work some exercises to calculate electromigration lifetime.
g. Stress Induced Voiding: We discuss the mechanism of stress voiding, its origin, basic models for the mechanism, and how to minimize its effect.
h. Compound Semiconductor Mechanisms: We briefly cover compound semiconductor-specific mechanisms like gate diffusion, contact diffusion, and hydrogen-related issues.

Day Three (Lecture Time 8 Hours)

4. Design for Reliability
   a. Transistor Level: We discuss compact models, SPICE and other approaches to assess transistor reliability in the context of a larger design.
   b. Library Level: We discuss approaches to create models that can be used for gate-level reliability simulations.
      i. Digital Gates

   ii. Analog Gates
   iii. SRAM
c. Macro/Block Level: We discuss approaches to minimize reliability problems at the block level like signal probability analysis and input vector control.
d. Core/Chip Level: We discuss top-level techniques to improve reliability like adaptive VDD and adaptive body bias.
e. Exercises: We work an exercise to show how to implement design for reliability techniques effectively.

5. Single Event Upset: We discuss Single Event Upset, its origins, and techniques for minimizing the effects of SEU on circuit operation.
6. Test Structures and Test Equipment
   a. Test Structures: We describe how the various test structures can be used not only to evaluate yield, but also how they can be used to evaluate reliability. We also describe test structures designed specifically for reliability stress tests.
      i. Parametric Test Structures
      ii. Reliability Test Structures
      iii. Self-Stressing Test Structures
   b. Test Equipment: We briefly describe the major pieces of equipment used for reliability testing.
      i. Wafer Level Testing
7. Wafer Level Testing Activities: We discuss the types of tests performed and the issues regarding test.
8. Future Reliability Challenges: We conclude the course by taking a look forward to determine what types of reliability challenges lie ahead in the future.



Feedback

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To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered in the next newsletter, please contact Jeremy Henderson by Email (jeremy.henderson@semitracks.com).

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To post, read, or answer a question, visit our forums.
We look forward to hearing from you!

Upcoming Courses

(Click on each item for details)

Semiconductor Reliability
March 12 – 14, 2012 (Mon. – Wed.)
San Jose, CA, USA

Wafer Fab Processing
March 12 – 15, 2012 (Mon. – Thurs.)
San Jose, CA, USA

Failure and Yield Analysis
April 9 – 11, 2012 (Tues. – Fri.)
Singapore

EOS, ESD and How to Differentiate
April 12 – 13, 2012 (Thurs. – Fri.)
Malaysia

ESD Design and Technology
April 22 – 24, 2012 (Sun. – Tues.)
Tel Aviv, Israel

Failure and Yield Analysis
April 22 – 25, 2012 (Sun. – Wed.)
Tel Aviv, Israel

Failure and Yield Analysis
May 7 – 10, 2012 (Mon. – Thurs.)
Munich, Germany

Copper Wire Bonding
May 7 – 8, 2012 (Mon. – Tues.)
Munich, Germany

Semiconductor Reliability
May 14 – 16, 2012 (Mon. – Wed.)
Munich, Germany