Issue 150 December 2021

InfoTracks

Semitracks Monthly Newsletter

Thermal Detection Techniques

By Christopher Henderson

This month, we will continue our series of Feature Articles by discussing Liquid Crystal Thermography. Liquid Crystal Thermography is the most popular thermal detection technique used in failure analysis laboratories. Liquid crystals are inexpensive to purchase and use, and have higher spatial resolution than infrared thermography. The main drawback to Liquid Crystal Thermography is that the technique requires putting liquid crystal material on the die surface. While it is not difficult to apply or remove, it does add additional steps to the failure analysis process.

First, a bit of history on liquid crystals. Liquid crystal research began in the 1950s. Soon after the semiconductor industry started, engineers began applying liquid crystals for analysis purposes. One of the first liquid crystal compounds to be used by failure analysts was a cholesteric liquid crystal called Merck T74. This particular liquid crystal shows color changes with temperature.

Liquid crystal comes packaged either in a container, like we show in Figure 1 on the left, or in a syringe. Liquid crystal can help generate information to isolate regions of heat dissipation, known as hot spots, like we show in Figure 1 on the right.

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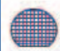

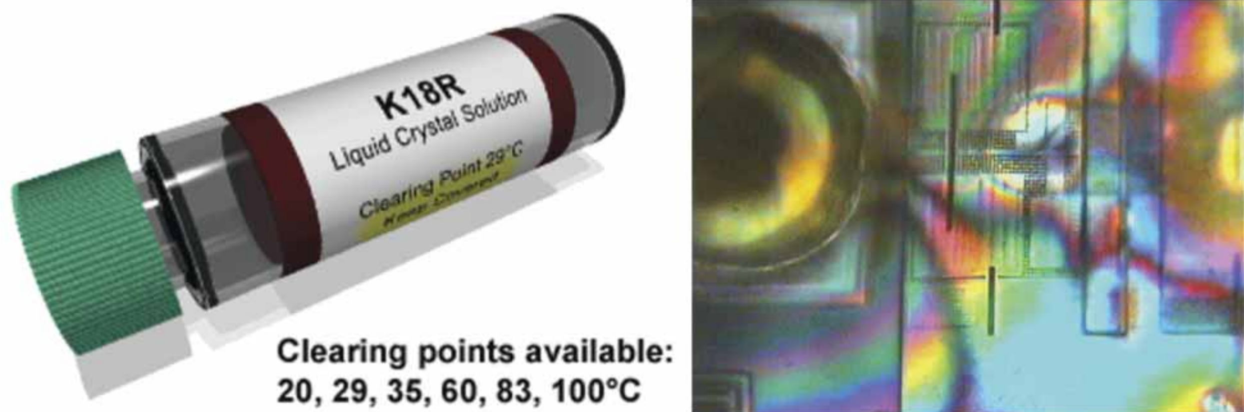

Figure 1. Liquid crystal container (left), and image of hot spot detected with liquid crystal (right).

Figure 2 shows the chemical structures for the more common liquid crystals used for failure analysis purposes. The most commonly used liquid crystals are nematic, or thread, types. K-18, 4-cyano-4-n-hexyl-1, 1'biphenyl, is commercially available and has a state transition temperature of 29.9°C. This works well for applications at approximately room temperature. Another common liquid crystal is K-21, which has a state transition temperature of just under 43°C. There are other liquid crystals available on the market with temperatures ranging from 30°C to 100°C.

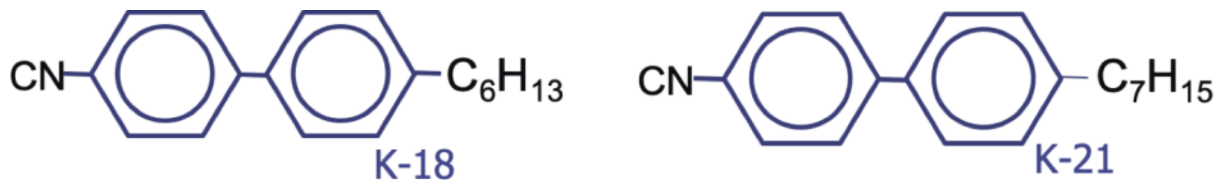

Figure 2. Chemical structures for K-18 and K-21 liquid crystals.

When a liquid crystal is applied to the surface of a semiconductor component, it will alter the behavior of light reflecting off of the sample. In areas where the temperature of the circuit is below the state transition temperature, or clearing point, the light is rotated due to the index of refraction change. This area is said to be in the nematic phase. In areas where the temperature is above the clearing point, the light is not rotated, and is said to be in the isotropic phase, as shown in Figure 3.

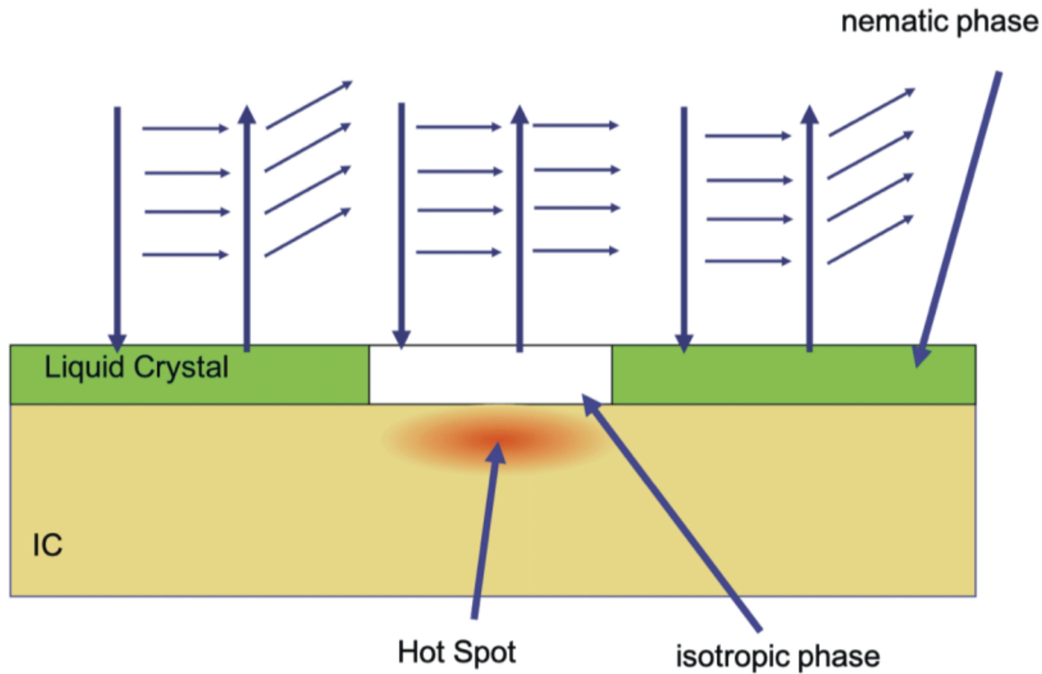

Figure 3. Diagram showing light polarization rotation as a function of the liquid crystal phase.

Figure 4 shows the setup for liquid crystal; note that it is quite simple. One can use a standard light microscope with a polarizer between the light source and the sample, and a second polarizer between the sample and the eyepiece. The first polarizer restricts the light to a certain polarization rotation. The second polarizer can be set to either restrict or allow the light through after it has been rotated by the nematic phase of the liquid crystal. If the light from the nematic phase is allowed to pass, then the area where the liquid crystal is isotropic will appear dark.

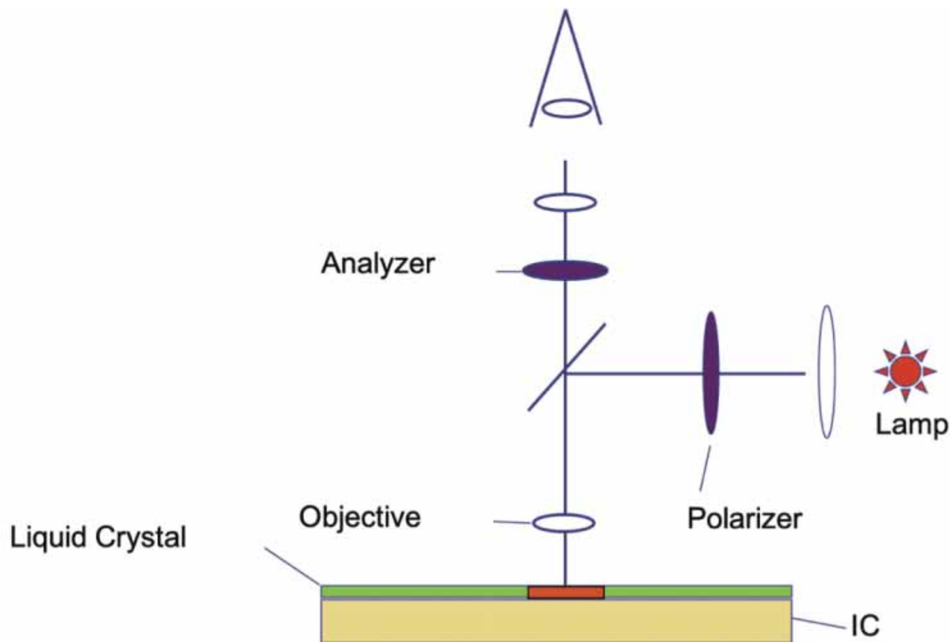

Figure 4. Diagram showing the optical setup for liquid crystal.

It is also easy to prepare liquid crystals for thermography. It is important to note that one must dilute the liquid crystals before use. This can be done using solvents like methanol, freon, or pentane. The goal is to achieve a thin uniform layer on the semiconductor device. The layer should be thick enough to produce the optical effects, but thin enough not to distort the thermal profile. A layer 5 to 7µm thick is ideal for this type of work. A thin layer will also tend to be more temperature sensitive. The correct thickness will yield a multi-color mottled appearance, like we show in Figure 1 above. After the technique has been performed, the liquid crystal should be removed so as to not interfere with subsequent analysis steps. It can be removed using acetone.

Once the liquid crystal has been applied, the device under test will be heated using a thermal stage to just below the state transition temperature of the liquid crystal. The closer one is able to hold the chuck to the state transition temperature, the more sensitive the technique will be. For this reason, it is desirable to protect the sample from air movement, such as that caused by heating or air conditioning. A dark box or plexiglass shield can provide this capability. Heat and cool techniques are also popular. In the heat technique, one heats the sample above the state transition temperature and lets the sample cool back down through it. In the cool technique, the sample is cooled below the state transition temperature and allowed to warm back through it. In either technique, the last area to clear, or the last clear area, depending on the configuration of the polarizers, will define the hot spot.

Figure 5 is an example of liquid crystal thermography in action. The image shows an electromigration test structure with 100mA of current applied to it. Although 100mA sounds like a large current, the power density in the structure is quite low since the resistance of the aluminum is low. The power density is approximately 2100 W/cm^2. Here we are using the K-18 liquid crystal compound. It has a state transition temperature of 29.9°C. The background temperature is around 27°C, and we are using only the heating of the structure itself to produce the effect. The dark areas are areas where the temperature is above 29.9°C and correspond to the aluminum line in the electromigration test structure.

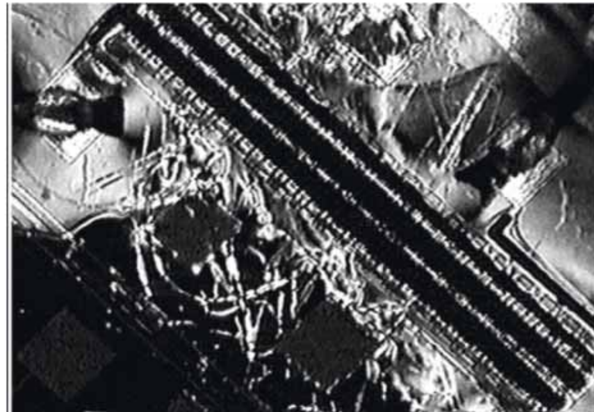

Figure 5. Example showing liquid crystal thermography of an electromigration test structure under stress.

The sequence of images in Figure 6 shows another example of liquid crystal thermography. In this case, we are looking at an input-output buffer that exhibits higher than normal leakage. As we increase current through the leakage site, a small bubble forms at the failure site, as seen in the left image of Figure 6. As the current through the defect increases, the temperature increases, and the bubble associated with leakage site expands, as seen in the center image. Finally, when the leakage is high enough, the clearing

point of the liquid crystal is reached. The polarizer in the optics path blocks the light, causing a dark area in the image that is associated with the isotropic region of the crystal, as seen in the right image of Figure 6.

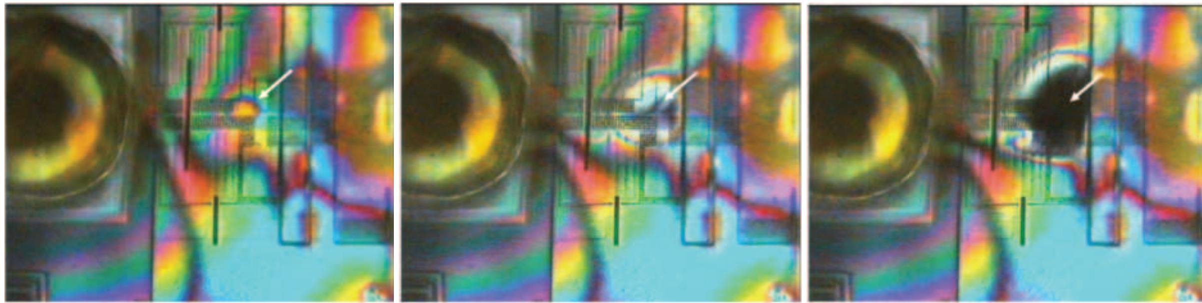

Figure 6. Sequence of liquid crystal images showing a hot spot at successively higher levels of power dissipation.

In summary, liquid crystals have been used for at least 60 years in failure analysis activities. They are quite popular with failure analysts because of their low cost and the ease of use. They provide resolution to approximately the wavelength of the light being used and can provide thermal resolution to about 1°C in normal use. Some engineers have demonstrated increased sensitivity through the use of heating/cooling techniques and precision thermal chucks. Finally, Liquid Crystal Thermography is the only thermal imaging technique that provides real time imaging.

In next month's Feature Article, we will discuss Fluorescent Microthermal Imaging.

Technical Tidbit

Future Transistor Configurations

In this month's Technical Tidbit, we will discuss future transistor configurations.

For many years, the planar MOSFET was the main configuration for transistors in integrated circuits. Then, about 10 years ago, the semiconductor industry began using a different configuration known as the FinFET. Although somewhat more difficult to produce, the FinFET exhibits superior gate control to the planar MOSFET, providing better current drive compared to equivalent-sized planar transistors. However, the FinFET does have some notable disadvantages as one scales down the size of the transistors. The FinFET only provides control on 3 sides of the transistor channel. Also, to scale down the FinFET, one must increase the height of the fins, which increases the challenges in manufacturing the fin, and increases the variability of the fin behavior. Furthermore, the bottom of the fin is subject to unwanted effects, like punch-through. This requires implants to suppress the effect. The main option is to move to a configuration called the Gate All Around transistor, or GAA. The GAA transistor eliminates these disadvantages: there isn't a fin height with which to be concerned, and there is no bottom of a fin to create unwanted effects. Most importantly, the gate covers fourth side of the structure. There are two options for GAA transistors: nanowires and nanosheets. We will briefly discuss both of these options.

Before we discuss the GAA nanowires and nanosheets, first, let's say a few more words about why the industry is moving from FinFET to GAA transistors. In addition to the logic CMOS scaling push on the processing side, the design side of the semiconductor community made considerable efforts to reduce the dimensions of logic standard cells. One way to do this is to reduce cell height by reducing the number of tracks. As noted in Figure 1, the cell height is defined as the number of metal lines (or tracks) per cell times the metal pitch.

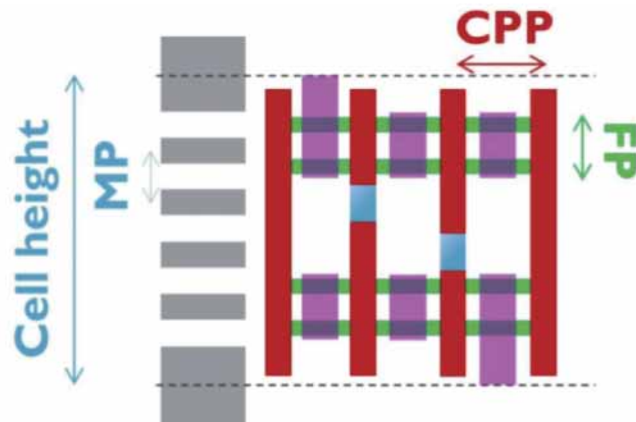

Figure 1. Example of a Standard Cell showing cell height on the left, the Metal Pitch (MP), the Contacted Polysilicon Pitch (CPP), and the Fin Pitch (FP).

For the FinFET, designers, working with process integration engineers, created new generations with ever-smaller cell heights by gradually reducing the number of fins within one standard cell from 3 to 2. This has enabled 7.5 track or 7.5T and 6 tracks or 6T, standard cells, respectively. With 6T, for example, we mean that 6 metal lines fit in the range of the cell height. Eventually, this trend continued to 1 fin, enabling 5T standard cells. We show the evolution in the scaling of standard cell designs in Figure 2. This evolution, however, came at the expense of drive current and variability. To compensate for the degradation of drive current and variability, process integration engineers made the fins taller. However, further enhancing the drive current of 5T FinFET-based single-fin device architectures is extremely challenging.

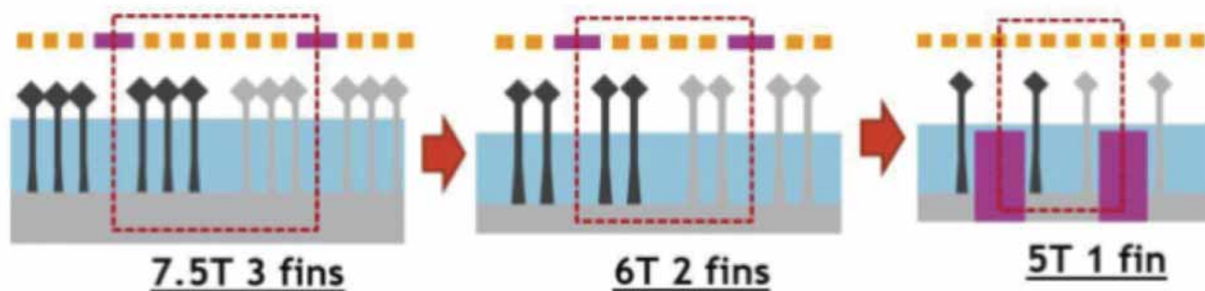

Figure 2. Scaling path for FinFETs from 3-fin structures (left) to 2-fin structures (center) to 1-fin structures (right).

This is where GAA nanosheet and nanowire transistors enter the picture. An important advantage of a GAA transistor over a FinFET transistor is its gate-all-around structure. As the conduction channel is now completely surrounded by the high-k/metal gate, improved gate control over the channel is achieved for shorter channel lengths. Furthermore, by vertically stacking nanosheet or nanowire-shaped conduction channels in standard cells where only one fin is allowed, a larger effective channel width can be realized. This way, GAA transistors can provide larger drive current per footprint than fins — a key benefit for further CMOS scaling. The GAA configuration also allows for a variable device width, which enables some flexibility in design. Designers can now trade off enhanced drive current for reduced area and capacitance, since a smaller channel width tends to reduce parasitic capacitance between the sheets.

The set of images in Figure 3 show the basic process flow for nanowires and nanosheets. First, engineers deposit a series of alternating silicon and silicon-germanium nanosheet layers. Next, they pattern the nanosheet shape into a fin-like structure and then etch to create the structure, along with the Shallow Trench Isolation, or STI. Next, they deposit oxide into the trenches, and etch back to leave the nanowire or nanosheet fin structure above the oxide. Next, they pattern for the dummy gate structure. They then create the space and inner spacer structures. They then follow this step by depositing a dual source-drain epitaxial layer. For the p-channel FET, this is silicon-germanium with boron incorporated into the material, and for the n-channel FET, this is silicon-carbon with phosphorus incorporated into the material. Next, they perform the channel release to remove the silicon from the nanowire or nanosheet stack. They then deposit the replacement metal gate, followed by the creation of an air spacer to lower the dielectric constant which reduces the capacitance between the transistors. They then form a wrap-around contact, and then proceed to the Middle Of Line, and Back End Of Line processing to create the interconnect and wiring between the transistors.

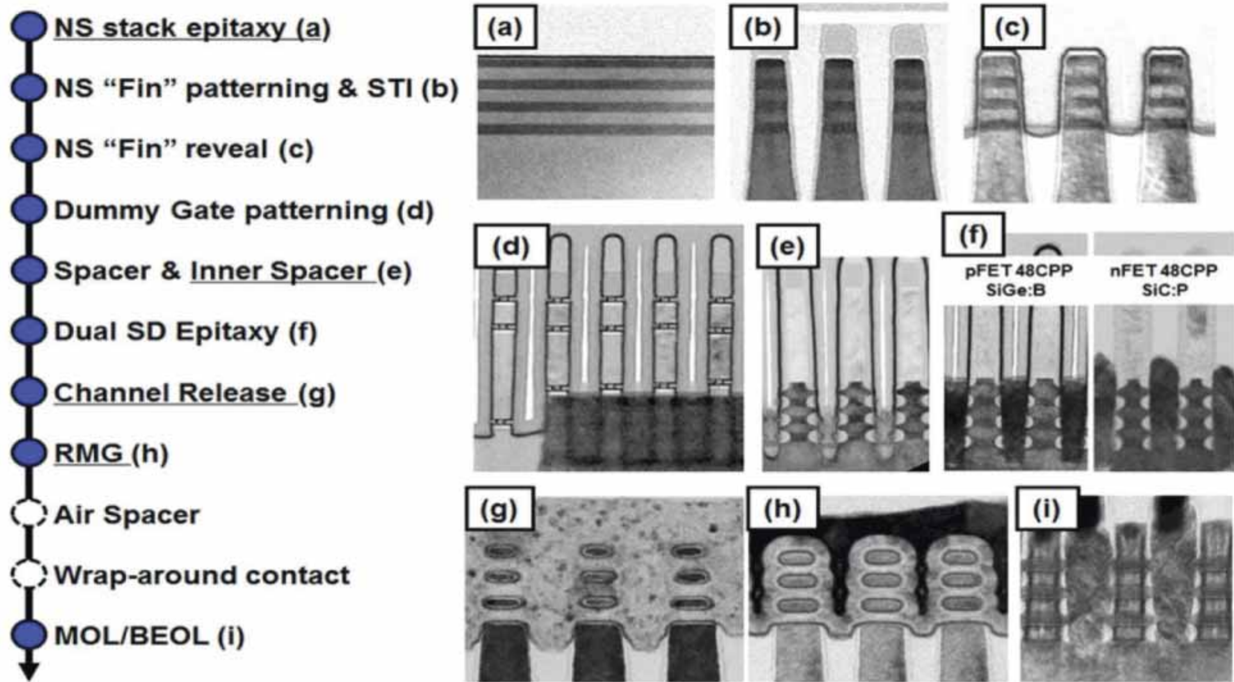

Figure 3. Basic process flow for nanowires and nanosheets.

The first option for GAA transistors is the nanowire configuration. We show an example of this in the transmission electron microscope (TEM) cross-section on the left of Figure 4. On the right of Figure 4, we show a graphical depiction of the transistor using a three-dimensional perspective. This was an early configuration for the GAA transistor.

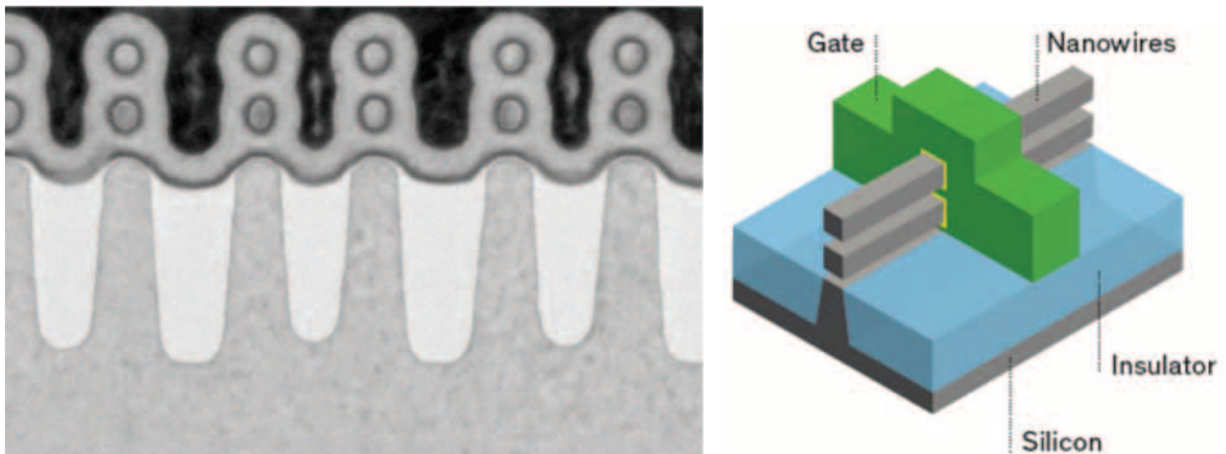

Figure 4 Nanowire configuration for GAA transistors. TEM cross-section (left), graphical depiction (right).

The second, and more common option, for GAA transistors is the nanosheet configuration. In Figure 5, we show an example of stacked nanosheet GAA transistors from Intel. In this configuration, the n-channel and p-channel transistors are stacked on top of each other.

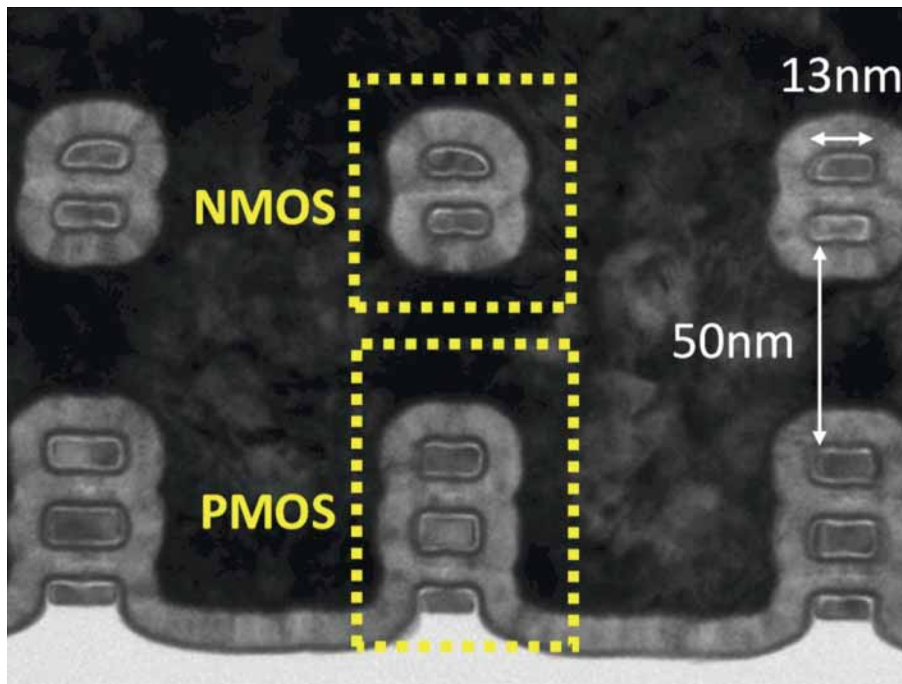

Figure 5. Stacked nanosheet transistors manufactured by Intel.

The image on the left in Figure 6 is an example of nanosheet transistors from TSMC. The air gap structure helps to lower this capacitance. The graph on the right in Figure 6 shows the capacitance as a function of the supply voltage.

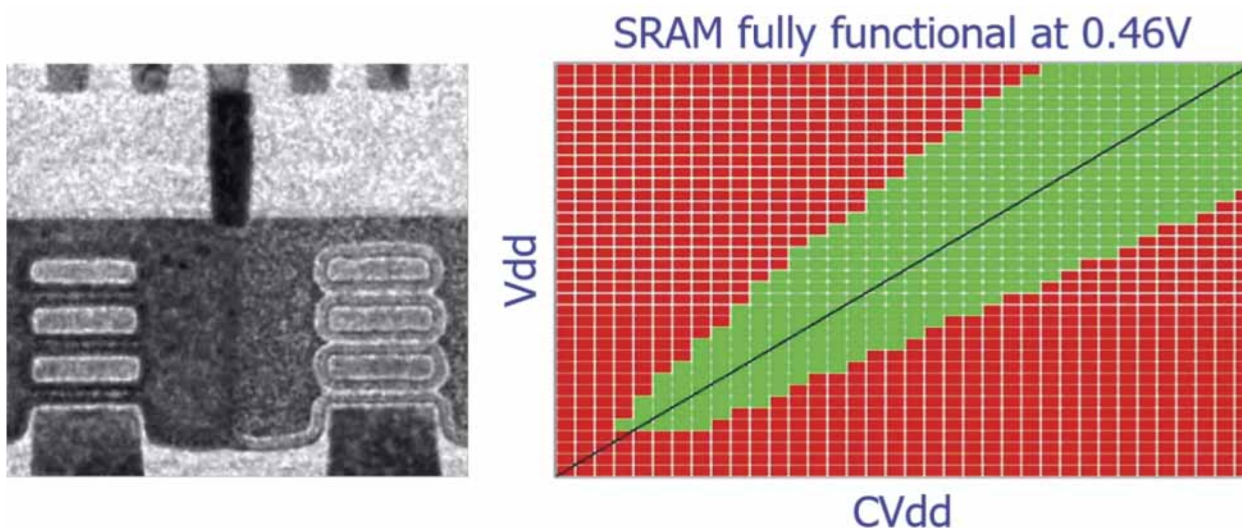

Figure 6. Stacked nanosheet transistors manufactured by TSMC (left).
Capacitance as a function of supply voltage in a TSMC Static Random Access Memory (SRAM) (right).

Another company developing nanosheet transistors for state-of-the-art integrated circuits is Samsung. The TEM image in Figure 7 shows an example of nanosheet transistors from Samsung.

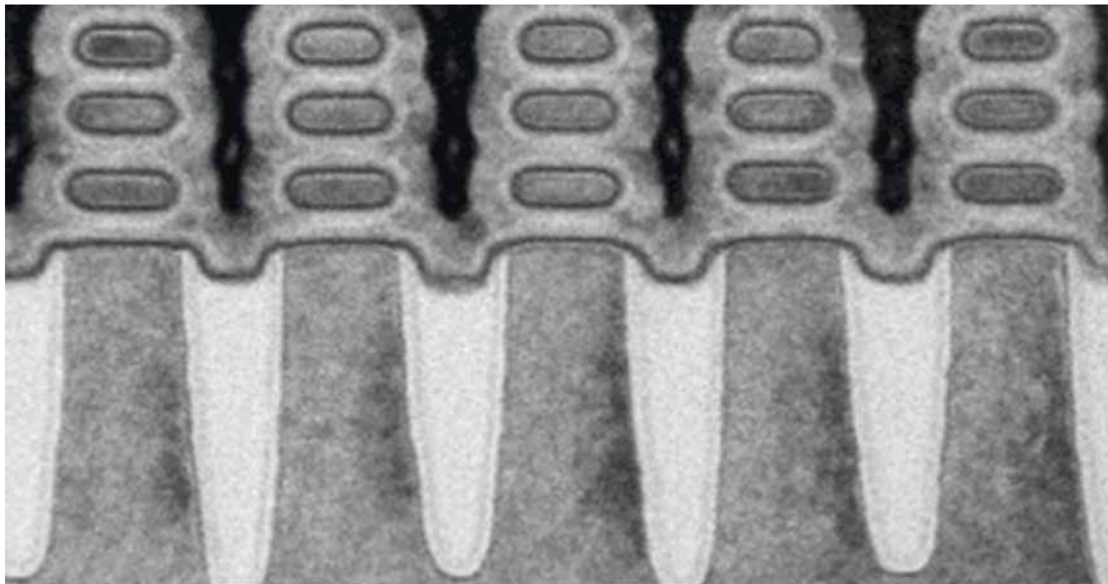

Figure 7. Stacked nanosheet transistors manufactured by Samsung.

One group that has published extensively on GAA transistor development is IBM Research. Figure 8 shows an example set of cross-sectioned nanosheet transistors from IBM. IBM, as well as the rest of the semiconductor industry, has determined for now, that nanosheet transistors provide better power-performance design due to better electrostatic control as well as a higher transistor density. Compared to the latest and greatest 7nm FinFET technology now available in the industry, nanosheet technology offers more than 25 percent performance improvement at the same power, or more than 50 percent power saving at the same performance. Nanosheet configurations also allow for variable sheet width with more streamlined design. It is worth noting that nanosheet technology is a better device architecture for computer products in the age of Artificial Intelligence and 5th Generation cellular technology due to its variable sheet width. This is enabled by Extreme Ultraviolet Lithography (EUVL), and allows for a far more versatile device design, as nanosheet devices with different channel widths can be co-integrated in the same chip for improved power-performance optimization. Finally, nanosheets offer improved channel thickness control. Growing the nanosheet stack's channel layers can create an atomic-level control for channel formation. Such precise channel thickness control is not possible for FinFETs as it is defined by lithography in conjunction with Reactive Ion Etching, where local and global process variations are much higher than the epitaxial thickness variation.

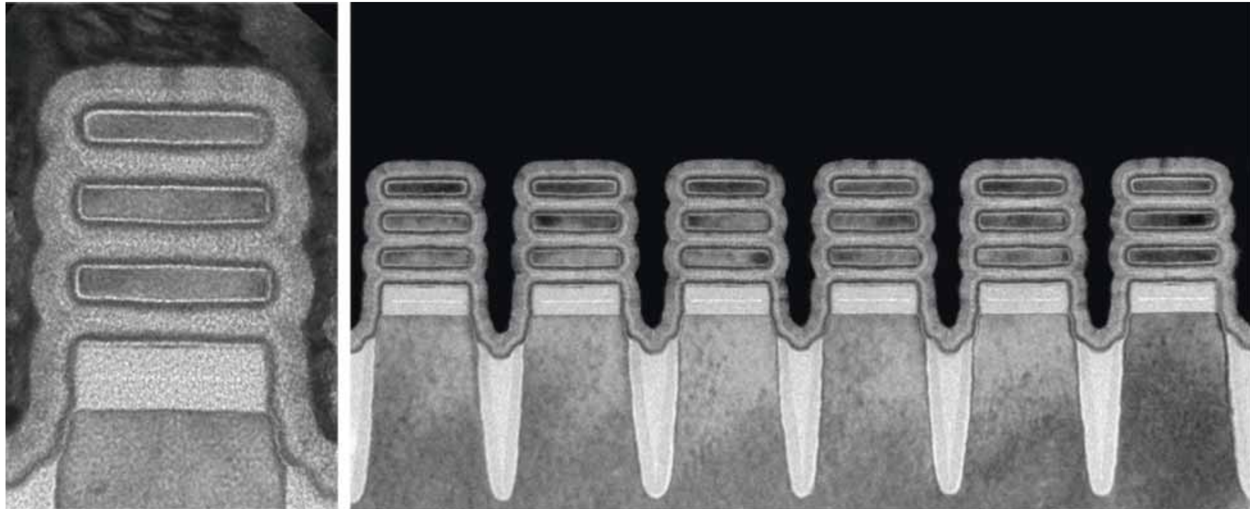

Figure 8. Stacked nanosheet transistors manufactured by IBM.

There are considerable process integration challenges involved with manufacturing GAA transistors. We will briefly mention three challenges. The first challenge is to create a full bottom dielectric isolation to enable the stacked nanosheet transistor configuration. IBM Researcher Jingyun Zhang and her colleagues developed a full bottom dielectric isolation scheme by inserting a dielectric layer underneath both the source/drain and gate regions that eliminates sub-channel leakage for scaled gate lengths. In addition, this feature reduces parasitic capacitance and provides additional power-performance improvement for GAA nanosheet technology. The second is the need to create multiple threshold voltage solutions for nanosheet transistors that can be used for high performance and low power applications. Ruqiang Bao and his colleagues invented novel processes and an integration scheme to implement multiple dipole thicknesses to achieve multiple transistor threshold voltages without changing the volume the transistor occupies. Additionally, they were able to invent a process to control the metal gate boundary during patterning in wide sheets, solving a fundamental issue in nanosheet technology. The third is to develop a dry selective etch of the Silicon/Germanium layers. Nicolas Loubet and his fellow researchers developed a novel isotropic dry etch technique to precisely control the lateral silicon germanium etch with very high selectivity to silicon (>150:1) and dielectrics (>1000:1). Additionally, this etch process can be used during the channel release process, delivering very low channel thickness variability with electrostatics and resistance variation, which is critical for power/performance optimization of high-performance computing stacked nanosheet devices. For further information on these techniques, one can consult the papers that were presented at IEDM 2019.

Finally, let's discuss a variant of the nanosheet structure called the forked nanosheet structure. We show an example of the forked nanosheet transistor from IMEC in Figure 9. The most elegant way to further increase DC performance is by enlarging the effective width of the channels, but in conventional nanosheet architectures, this becomes very difficult. The main problem is the large space margin that is needed in between n- and p-channel transistors, which makes a large effective nanosheet width difficult in scaled cell heights. This space is consumed by a lateral over-etch that arises during the work function metal patterning step. The architecture of the forked nanosheet device, sometimes referred to as a forksheet device, can address this challenge. The forksheet was for the first time publicly proposed by IMEC for SRAM scaling in 2017 (IEDM 2017), and later on as a logic standard cell scaling enabler (IEDM

2019). In this architecture, smaller n-p separation is enabled by introducing a dielectric wall in between n- and pMOS devices before gate patterning. This dielectric wall now serves as an etch stop layer for patterning the work function metal, allowing a much tighter n-to-p spacing. Consequently, the effective width of the channels – and hence, the drive current (DC performance) – can be further enhanced. Instead of maximizing the effective channel width, the smaller n-to-p space can alternatively be exploited to further scale the track height of the standard cell from 5T to 4T. This evolution needs to be complemented by innovations in the back-end and middle-of-line, and by introducing scaling boosters (such as buried power rails or self-aligned gate contacts).

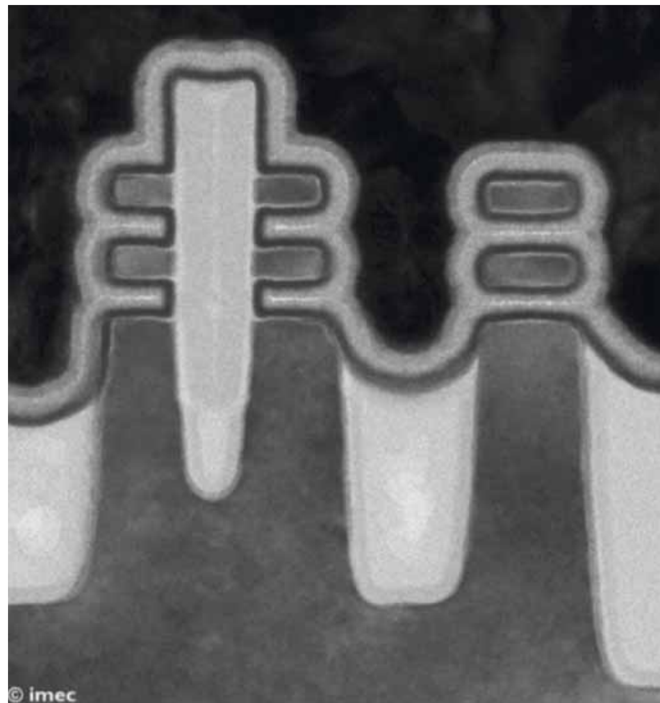

Figure 9. TEM cross-section image of a Forked nanosheet transistor (also known as the "Forksheet" transistor) from imec.

From a processing perspective, the forksheet architecture naturally evolves from the 'basic' nanosheet architecture. Key differentiators are the dielectric wall formation, modified inner spacer, source/drain epitaxy and replacement metal gate steps. At VLSI 2021, IMEC presented electrical data on forksheet field-effect devices that were successfully integrated using a 300mm wafer forksheet process flow. Dual work function metal gates can be integrated at 17nm spacing between the n- and pFETs – highlighting the key benefit of the forksheet architecture.

In conclusion, we introduced the main future transistor configuration – the Gate All Around, or GAA transistor. GAA transistors remove several major disadvantages associated with FinFETs related to channel control, drive strength, and design options. GAA transistors can either be fabricated as nanowires, or more commonly, as nanosheets. The nanosheet transistor configuration provides more versatility for chip designs, and provides improved performance compared to nanowire transistors. One emerging variant of the nanosheet configuration is the forked nanosheet transistor configuration, or forksheet. The GAA transistor is still undergoing rapid evolution, so one should expect to see significant changes and improvements to this architecture in the coming years.

Ask the Experts

Q: Do you know why some companies use 156°C/85% RH as their HAST condition?

A: The normal JEDEC HAST conditions specify either 130°C/85% RH, or 110°C/85% RH, depending on the packaging materials, for qualification tests. However, some companies might use 156°C/85% RH in a HAST chamber to further accelerate heat humidity degradation. This might be performed during package development or the development of new materials for packaging.

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Spotlight: Semiconductor Reliability and Product Qualification

OVERVIEW

Package reliability and product qualification continues to evolve with the electronics industry. New electronics applications require new approaches to reliability and qualification. In the past, reliability meant discovering, characterizing and modeling failure mechanisms and determining their impact on the reliability of the circuit. Today, reliability can involve tradeoffs between performance and reliability, assessing the impact of new materials, dealing with limited margins, etc. in particular, the proliferation of new package types. This requires information on subjects like: statistics, testing, technology, processing, materials science, chemistry, and customer expectations. While customers expect high reliability levels, incorrect testing, calculations, and qualification procedures can severely impact reliability. Your company needs competent engineers and scientists to help solve these problems. ***Semiconductor Reliability and Qualification*** is a four-day course that offers detailed instruction on a variety of subjects pertaining to semiconductor reliability and qualification. This course is designed for every manager, engineer, and technician concerned with reliability in the semiconductor field, qualifying semiconductor components, or supplying tools to the industry.

What Will I Learn By Taking This Class?

Participants learn to develop the skills to determine what failure mechanisms might occur, and how to test for them, develop models for them, and eliminate them from the product.

1. **Overview of Reliability and Statistics.** Participants learn the fundamentals of statistics, sample sizes, distributions and their parameters.
2. **Failure Mechanisms.** Participants learn the nature and manifestation of a variety of failure mechanisms that can occur both at the die and at the package level. These include: time-dependent dielectric breakdown, hot carrier degradation, electromigration, stress-induced voiding, moisture, corrosion, contamination, thermomechanical effects, interfacial fatigue, etc.
3. **Qualification Principles.** Participants learn how test structures can be designed to help test for a particular failure mechanism.
4. **Test Strategies.** Participants learn about the JEDEC test standards, how to design screening tests, and how to perform burn-in testing effectively.

COURSE OBJECTIVES

1. The seminar will provide participants with an in-depth understanding of the failure mechanisms, test structures, equipment, and testing methods used to achieve today's high reliability components.
2. Participants will be able to gather data, determine how best to plot the data and make inferences from that data.
3. The seminar will identify the major failure mechanisms, explain how they are observed, how they are modeled, and how they are eliminated.
4. The seminar offers a variety of video demonstrations of analysis techniques, so the participants can get an understanding of the types of results they might expect to see with their equipment.

5. Participants will be able to identify the steps and create a basic qualification process for semiconductor devices.
6. Participants will be able to knowledgeably implement screens that are appropriate to assure the reliability of a component.
7. Participants will be able to identify appropriate tools to purchase when starting or expanding a laboratory.

COURSE OUTLINE

Day 1 (Lecture Time 8 Hours)

1. Introduction to Reliability
    1. Basic Concepts
    2. Definitions
    3. Historical Information
2. Statistics and Distributions
    1. Basic Statistics
    2. Distributions (Normal, Lognormal, Exponent, Weibull)
    3. Which Distribution Should I Use?
    4. Acceleration
    5. Number of Failures

Day 2 (Lecture Time 8 Hours)

1. Overview of Die-Level Failure Mechanisms
    1. Time Dependent Dielectric Breakdown
    2. Hot Carrier Damage
    3. Negative Bias Temperature Instability
    4. Electromigration
    5. Stress Induced Voiding
2. Package Level Mechanisms
    1. Ionic Contamination
    2. Moisture/Corrosion
        1. Failure Mechanisms
        2. Models for Humidity
        3. Tja Considerations
        4. Static and Periodic stresses
        5. Exercises
    3. Thermo-Mechanical Stress
        1. Models
        2. Failure Mechanisms
    4. Interfacial Fatigue
        1. Low-K fracture
    5. Thermal Degradation/Oxidation

Day 3 (Lecture Time 8 Hours)

1. Package Attach (Solder) Reliability
    1. Creep/Sheer/Strain
    2. Lead-Free Issues
    3. Electromigration/Thermomigration
    4. MSL Testing
    5. Exercises
2. TSV Reliability Overview
3. Board Level Reliability Mechanisms
    1. Interposer
    2. Substrate
4. Electrical Overstress/ESD
5. Test Structures and Test Equipment
6. Developing Screens, Stress Tests, and Life Tests
    1. Burn-In
    2. Life Testing
    3. HAST
    4. JEDEC-based Tests
    5. Exercises

Day 4 (Lecture Time 8 Hours)

1. Calculating Chip and System Level Reliability
2. Developing a Qualification Program
    1. Process
    2. Standards-Based Qualification
    3. Knowledge-Based Qualification
    4. MIL-STD Qualification
    5. JEDEC Documents (JESD47H, JESD94, JEP148)
    6. AEC-Q100 Qualification
    7. When do I deviate? How do I handle additional requirements?
    8. Exercises and Discussion

INSTRUCTIONAL STRATEGY

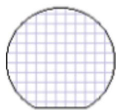
By using a combination of instruction by lecture, video, problem solving and question/answer sessions, participants will learn practical approaches to the failure analysis process. From the very first moments of the seminar until the last sentence of the training, the driving instructional factor is **application**. We use instructors who are internationally recognized experts in their fields that have years of experience (both current and relevant) in this field. The handbook offers hundreds of pages of additional reference material the participants can use back at their daily activities.

The Semitracks Analysis Instructional Videos™

One unique feature of this workshop is the video segments used to help train the students. Reliability Analysis is a visual discipline. The ability to identify nuances and subtleties in graphical data is critical to locating and understanding the defect. Some tools output video images that must be interpreted by engineers and scientists. No other course of this type uses this medium to help train the participants. These videos allow the analysts to directly compare material they learn in this course with real analysis work they do in their daily activities.

You may want to stress some aspects more than others or conduct a simple one-day overview course. Many of our clients seek ongoing just-in-time training that builds in-depth, advanced levels of reliability expertise. We'll work with you to determine the best course of action and create a statement of work that emulates the very best practices of semiconductor reliability analysis.

Our instructors are active in the field and they practice the disciplines daily. Please give us a call (505) 858-0454 or drop us an e-mail (info@semitracks.com).



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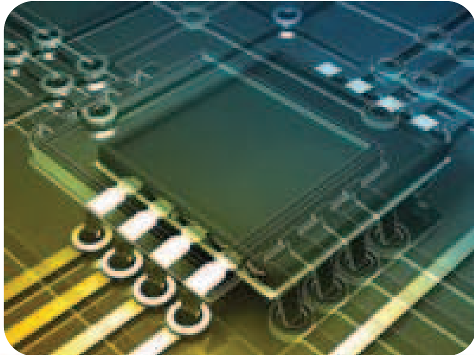

Feedback

If you have a suggestion or a comment regarding our courses, online training, discussion forums, or reference materials, or if you wish to suggest a new course or location, please call us at 1-505-858-0454 or Email us (info@semitracks.com).

To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered in the next newsletter, please contact Jeremy Henderson by Email (jeremy.henderson@semitracks.com).

We are always looking for ways to enhance our courses and educational materials.

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For more information on Semitracks online training or public courses, visit our web site!

http://www.semitracks.com

To post, read, or answer a question, visit our forums.
We look forward to hearing from you!

Upcoming Webinars

(Click on each item for details)

Wafer Fab Processing

4 sessions of 4 hours each
US: February 28 – March 3, 2022
(Mon – Thur), 11:00 A.M. – 3:00 P.M. EST;
8:00 A.M. – 12:00 noon PST

Semiconductor Reliability / Product Qualification

4 sessions of 4 hours each
US: March 7 – 10, 2022 (Mon – Thur),
11:00 A.M. – 3:00 P.M. EST;
8:00 A.M. – 12:00 noon PST