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Qualification Process Part 2

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In this section, we will continue to discuss the qualification process. Qualification takes into account the design, package and customer use conditions, so this is a very significant and important topic, especially from the customer's perspective.

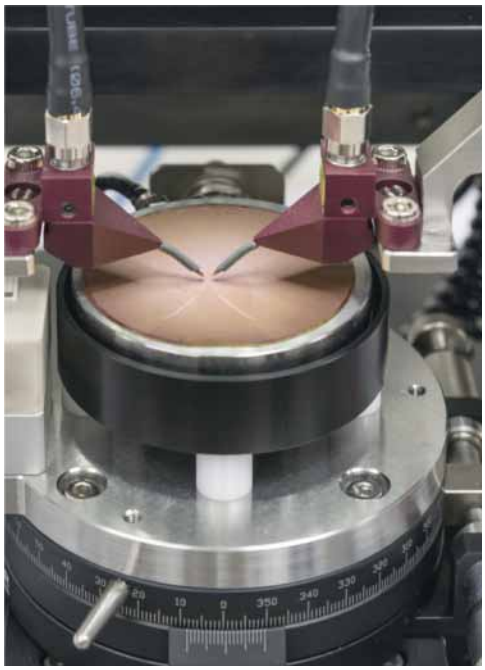


Figure 3.

In this Issue:

SEMITRACKS, INC.
Semiconductor, Microelectronics, Microsystems, and Nanotechnology Training

One important aspect of technology qualification is wafer level reliability testing. Wafer Level Reliability, or WLR, is a stress to failure. We use elevated voltages and temperatures. WLR is typically performed on test structures, and we use the process to evaluate wear-out failure mechanisms. One of the biggest challenges however with using test structures, is mapping the results to a real product. While stressing and understanding the failure mechanisms are much easier with test structures, they do not accurately represent what will happen with a product die.

WLR is typically part of the initial technology development cycle. When performed during technology development, we sometimes refer to this activity as Intrinsic Reliability Monitoring or IRM. Engineers normally look at major failure mechanisms like gate oxide integrity, negative bias temperature instability, hot carrier degradation, electromigration, and dielectric breakdown strength. IRM would normally be completed during qualification. WLR also involves set up tests to monitor the reliability on an on-going basis. This includes monitoring scribe line test structures and monitoring for shifts during bakes. The initial round of testing would typically be completed during qualification and ramping to volume production. Once the process is stable we then use WLR to monitor the process, and to assess major changes, should they be needed. WLR would typically be performed on a periodic basis to ensure that the reliability of the product from the fab continues to be at an acceptable level. Quite often, these periodic tests are maintained as trend charts in fabs or foundries.

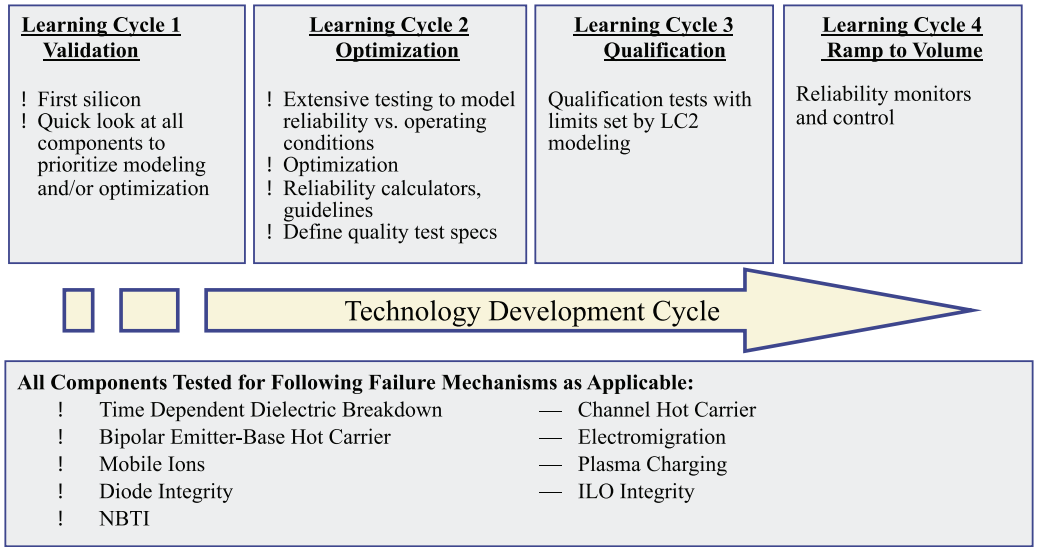


Figure 4.

WLR is often performed as a series of cycles. In learning cycle 1, we validate the silicon. We take a quick look at the important parameters to prioritize our reliability efforts. In learning cycle 2, we optimize the process. We perform more extensive modeling to check reliability vs. operating conditions.

We also create guidelines, calculators, and define the quality test specifications. In learning cycle 3, we perform the qualification tests themselves, using the limits we established during learning cycle 2. Finally, in learning cycle 4, we ramp to volume, and use WLR to monitor and control the process. One would typically monitor major failure mechanisms that apply to the technology, like we show here in Figure 4.

These are some common types of qualification used in the semiconductor industry. They include MIL-STD 883 for military and space applications, JEDEC JESD47 for stress driven qualification, and the Automotive Electronics Council, or AEC, standard. AEC released its failure mechanism-based stress test qualification for packaged ICs known as AEC-Q100 back in 2007. It is used widely in automotive applications. We will cover these standards in more detail below.

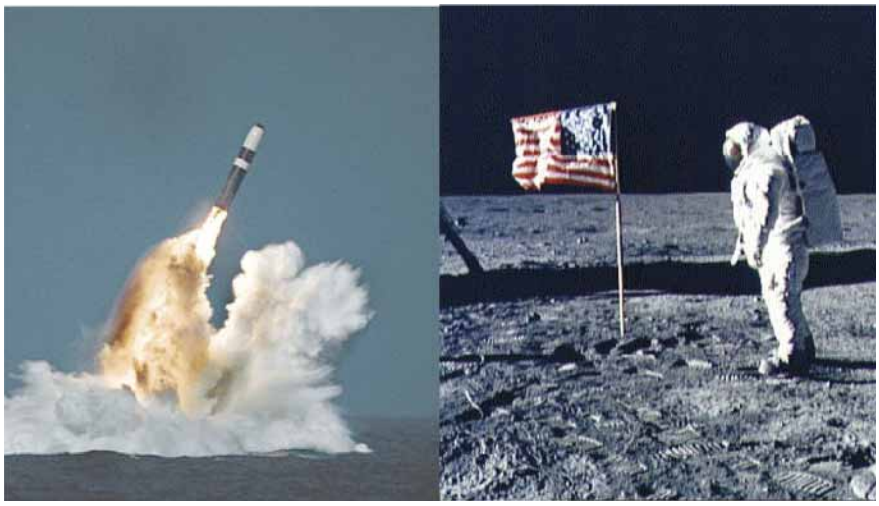


Figure 5.

We'll begin with some background on the military standard qualification procedures. Shortly after the invention of the transistor and the integrated circuit, the United States military became interested in using these solid-state devices in critical applications like weapons systems. Of course, assembly problems occurred where components failed. The US government became interested in these problems as they pushed for higher reliability levels, and as such, they began to fund studies and develop tests to characterize these problems. The first physics of failure conference was held in 1962 in the Los Angeles area so that the local defense contractors could discuss these problems and share their data. Several years later, the US government published a standard known as MIL-STD 883 to document the tests need to characterize these devices. This document was used for programs like the Trident II and Apollo programs. It was not intended as a qualification document per se, but developed into a body of knowledge used for qualification tests. This document now contains well over 50 tests.

To summarize, MIL STD 883 is an important document. It was the first document to codify test procedures for semiconductor devices and integrated circuits. However, the document is primarily written for military components. There is an emphasis on hermetically-sealed components, military temperature ranges, radiation effects, and 100% screening, since lot sizes are typically quite small. As such, many of these tests are not applicable to commercial integrated circuits packaged in plastic

packages. Furthermore, many of these test methods are out-of-date and reflect procedures that were used in the past, not in a modern fabrication environment where defect levels are quite low, product shipment sizes are large, and product lifecycles are extremely short.

JEDEC Standard 47 (JESD47) is the most common product qualification method used in the industry. JESD47 covers standardized tests that engineers can use to qualify semiconductor components. The standard allows for qualification of new products, families of products, and products where the process has changed. The standard is meant for normal operating environments rather than extreme operating environments. Therefore, it is not appropriate for applications like military use, high temperature use, or certain aspects of automotive use. The standard points out that one should defer to the use conditions for the user, if they're available. The standard also points out that the customer's requirements come first, and need to be met over and above the requirements of the standard. In summary, this document is not something to simply take at face value. You always want to incorporate the latest information, mechanisms, use conditions, and issues into your testing and qualification plans.

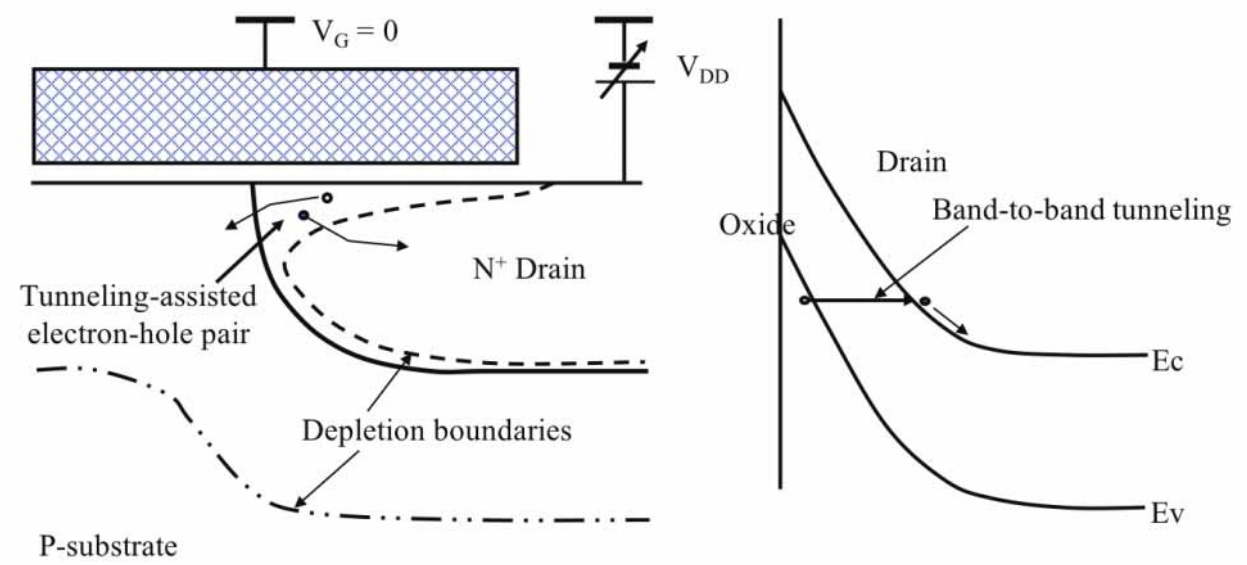
Let's now discuss the Automotive Electronics Council (AEC) standard, AEC-Q100. AEC-Q100 qualification allows a supplier who successfully completes the process for a component or components to claim the circuit is AEC-Q100 qualified. However, approval for use in an automotive system is beyond the scope of this document and instead based on the contractual agreements between the customer and the supplier. The document defines four different part operating temperature grades, ranging from Grade 0 which covers the largest temperature range, to Grade 3 which covers the least temperature range. Grade 0 is obviously the most difficult to achieve.

Technical Tidbit

Gate Induced Drain Leakage (GIDL)

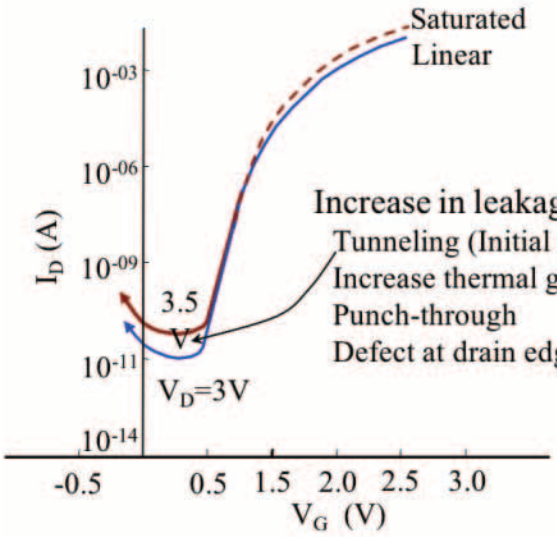
An important leakage component in today's transistors is gate induced drain leakage, or GIDL. In this technical tidbit, we will briefly explain the phenomenon.

GIDL is increased leakage observed at high drain voltages and low gate voltages. GIDL is attributable to band-to-band tunneling within the drain, like we show on the right. It creates tunneling-assisted electron-hole pairs in the drain region. In order for tunneling to occur, the band-bending must be at least that of the silicon bandgap.



GIDL is easiest to detect and creates the biggest impact on subthreshold current. However, it can be difficult to separate from other effects like increased thermal generation, punch through, defects, or ESD. This equation gives an estimate of the electric field in the silicon, so it is apparent that the amplitude of the band bending needs to exceed 1.2 volts in order for tunneling to occur. The GIDL current can be estimated by this equation: where A is a constant that depends on the effective mass of the electron, the bandgap, and the extent of the phonon scattering, for silicon B is approximately 21 megavolts per centimeter.

GIDL can be reduced by optimizing the junction profile under the gate near the drain, or by reducing the field, or reducing the drain to gate voltage.



Increase in leakage can be due to
- Tunneling (Initial GIDL definition)
- Increase thermal generation
- Punch-through
- Defect at drain edge

Estimate of electric field in silicon

$$E_{Si} \cong \frac{|V_{DG}|-1.2}{\frac{\varepsilon_{Si}}{\varepsilon_{ox}} t_{ox}} \approx \frac{|V_{DG}|-1.2}{3t_{ox}}$$

Band bending of at least Eg/q ≈ 1.2V needed for tunneling to occur

Estimate of GIDL current

$$I_D \cong AE_{Si} e^{-B/E_{Si}}$$

- A is a pre-exponential constant that depends on m*, Eg, and phonon scattering (extracted from data)
- B ≈ 21 MV/cm

*4

Ask the Experts

Q: I am having trouble etching platinum. What can I do?

A: It is essential to remove the Pt surface passivation caused by exposure to the atmosphere. This can be achieved by exposing the platinum layer to a pure Ar-plasma immediately prior to starting the Pt etch.

For reproducible results you can use Aqua Regia (3:1 mixture of HCl and HNO_3). It should be prepared shortly before use and then heated to around 60°C for the etching process. This process works best if you go directly from the Ar-plasma to the Aqua Regia etch to avoid re-growth of the passivation layer.

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Spotlight: CMOS, BiCMOS, and Bipolar Process Integration

OVERVIEW

Semiconductor and integrated circuit developments continue to proceed at an incredible pace. For example, today's mixed-signal chips perform a wide range of applications unheard of a few years ago, including wireless applications, high speed communications, and signal processing. These challenges have been accomplished because of the integrated circuit industry's ability to track something known as Moore's Law. A corollary to Moore's Law is that frequencies on mixed-signal devices continue to rise. This has been accomplished by making devices smaller and smaller. The question looming in everyone's mind is "How far into the future can this continue?" ***CMOS, BiCMOS, and Bipolar Process Integration*** is a 3-day course that offers detailed instruction on the physics behind the operation of a modern mixed-signal integrated circuit, and the processing technologies required to make them. We place special emphasis on current issues related to designing and manufacturing the next generation devices. This course is a must for every manager, engineer and technician working in the semiconductor industry, using semiconductor components or supplying tools to the industry.

By focusing on the fundamentals of transistor operation and performance, participants will learn why advances in the industry are occurring along certain lines and not others. Our instructors work hard to explain how semiconductor devices work without delving too heavily into the complex physics and mathematical expressions that normally accompany this discipline.

Participants learn basic but powerful aspects about the semiconductor industry. This skill-building series is divided into three segments:

1. **Basic Device Operation.** Participants learn the fundamentals of transistor operation. They learn why BiCMOS devices dominate the mixed-signal industry today.
2. **Fabrication Technologies.** Participants learn the fundamental manufacturing technologies that are used to make modern integrated circuits. They learn the typical CMOS, Bipolar and BiCMOS process flows used in integrated circuit fabrication.
3. **Current Issues in Process Integration.** Participants learn how device operation is increasingly constrained by three parameters. They also learn about the impact of using new materials in the fabrication process and how those materials may create problems for the manufacturers in the future.
4. **An Overview of Issues Related to Process Integration.** Participants learn about the image of new materials, yield, reliability and scaling on technology and process integration. They receive an overview of the major reliability mechanisms that affect silicon ICs today.

COURSE OBJECTIVES

1. The seminar will provide participants with an in-depth understanding of the semiconductor industry and its technical issues.
2. Participants will understand the basic concepts behind transistor operation and performance.
3. The seminar will identify the key issues related to the continued growth of the semiconductor industry.

4. The seminar offers a wide variety of sample problems that participants work to help them gain knowledge of the fundamentals of device operation and manufacturing.
5. Participants will be able to identify basic and advanced technology features on semiconductor devices. This includes features like silicon-germanium, emitter islands, copper, and low-k dielectrics.
6. Participants will understand how reliability, power consumption and device performance are interrelated.
7. Participants will be able to make decisions about how to construct and evaluate new CMOS, BiCMOS, and bipolar technologies.

INSTRUCTIONAL STRATEGY

By using a combination of instruction by lecture, classroom exercises, and question/answer sessions, participants will learn practical information on semiconductor devices and the operation of this industry. From the very first moments of the seminar until the last sentence of the training, the driving instructional factor is **application**. We use instructors who are internationally recognized experts in their fields that have years of experience (both current and relevant) in this field. The handbook offers hundreds of pages of additional reference material the participants can use back at their daily activities.

COURSE OUTLINE

Day 1

1. Introduction
2. Basic Semiconductor Concepts
   a. Diffusion/Drift
   b. PN Junction Diodes
   c. Bipolar Junction Transistor
   d. MOS Transistor
   e. Additional Concepts
      i. Avalanche Breakdown
      ii. Zener Breakdown
      iii. Tunneling
      iv. Schottky Barriers
3. General Scaling Issues
   a. Constant Field Scaling/Constant Voltage Scaling
   b. Process Integration Issues
      i. Transistors (Ion vs Ioff, Mobility Enhancement, short channel effects, etc.)
      ii. Interconnect (RC delay, power dissipation, etc.)
   c. Limitations to Scaling

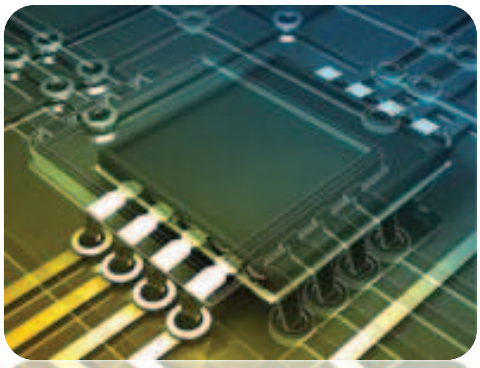
Day 2

4. Conventional CMOS
   a. Well/Substrate Engineering
   b. Device Isolation
   c. Gate Stack
   d. Contacts/Silicide
   e. Scaling Issues
   f. Basic CMOS Flow Presentation
5. Conventional BiCMOS
   a. Bipolar Transistor Fundamentals
   b. BiCMOS Process Overview
   c. Scaling and Limitations
   d. Basic BiCMOS Flow Presentation
6. Bipolar Enhancement Techniques
   a. SiGe
   b. SiGe:C
7. Power Technologies
   a. LDMOS
   b. DECMOS
   c. BCD
8. Additional Analog Circuit Elements
   a. Resistors
   b. Capacitors
   c. JFETs

Day 3

9. Interconnects
   a. Aluminum Interconnects, Issues
   b. Copper Interconnects, Issues
   c. Low-k Dielectrics
10. CMOS/Bipolar/BiCMOS Reliability Considerations
    a. Electrostatic Discharge
    b. Electromigration and Stress Migration
    c. Soft Errors, Plasma Damage
    d. Dielectric Reliability
    e. Bias Temperature Instabilities
    f. Hot Carrier Reliability
    g. Burn-In

11. Yield Considerations
    a. Yield Detractors
    b. Models
    c. Monitors
12. Conclusion/Wrap Up



Feedback

If you have a suggestion or a comment regarding our courses, online training, discussion forums, or reference materials, or if you wish to suggest a new course or location, please call us at 1-505-858-0454 or Email us (info@semitracks.com).

To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered in the next newsletter, please contact Jeremy Henderson by Email (jeremy.henderson@semitracks.com).

We are always looking for ways to enhance our courses and educational materials.

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http://www.semitracks.com

To post, read, or answer a question, visit our forums.
We look forward to hearing from you!

Upcoming Courses

(Click on each item for details)

CMOS, BiCMOS and Bipolar Process Integration
February 18 – 20, 2019 (Mon – Wed)
Singapore

Failure and Yield Analysis
April 23 – 26, 2019 (Tue – Fri)
Munich, Germany

Wafer Fab Processing
April 23 – 26, 2019 (Tue – Fri)
Munich, Germany

EOS, ESD and How to Differentiate
April 29 – 30, 2019 (Mon – Tue)
Munich, Germany

Semiconductor Reliability / Product Qualification
May 6 – 9, 2019 (Mon – Thur)
Munich, Germany

Semiconductor Reliability / Product Qualification
May 13 – 16, 2019 (Mon – Thur)
Tel Aviv, Israel

Introduction to Processing
June 3 – 4, 2019 (Mon – Tue)
San Jose, California, USA

Advanced CMOS/FinFET Fabrication
June 5, 2019 (Wed)
San Jose, California, USA

Interconnect Process Integration
June 6, 2019 (Thur)
San Jose, California, USA