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Voltage Contrast Part 2

By Christopher Henderson

The next variation of voltage contrast is biased voltage contrast. Biased voltage contrast is the imaging of voltages on a device with a bias applied to one or more connections. For instance, a CMOS integrated circuit can be observed using biased voltage contrast by connecting VDD to power and VSS to ground. The mechanism is the same as that of passive voltage contrast. The secondary electrons are sensitive to the local electrical potentials on the conductors. A conductor at ground emits more secondary electrons, resulting in a light contrast. A conductor at a positive voltage emits fewer electrons, resulting in a dark contrast. Biased voltage contrast can be used to isolate failure sites to a logic block or even down to a metal trace.

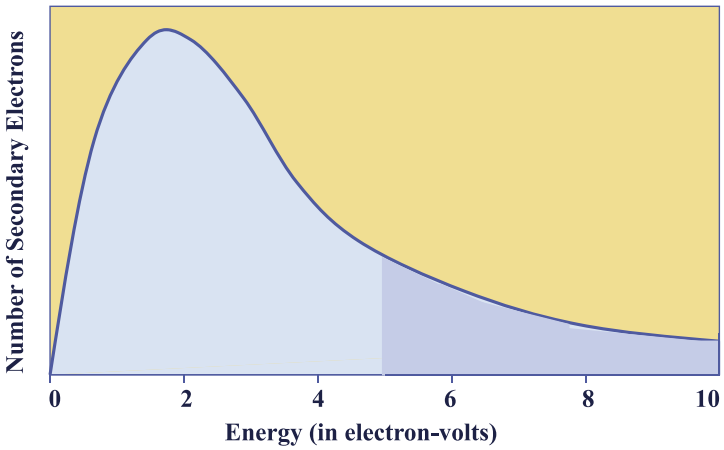

Figure 8. Secondary electron energy spectrum.

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The graph in Figure 8 shows the energies of emitted secondary electrons. The number of secondary electrons peaks at around 2 electron volts. A long tail extends out beyond 10 electron volts. If an interconnect is biased at zero volts, then secondary electrons with any particular energy can escape the conductor and be collected by the secondary electron detector. If a line is biased at 5 volts, then only secondary electrons with energies greater than 5 volts can escape. Fewer electrons escape than the total number above 0 volts. A large number of secondary electrons escaping creates a bright image, while a small number escaping creates a dark image. Also, notice from the shape of the curve that it will be difficult to detect the difference between 3 volts and 3.1 volts. The slight increase in the number of secondary electrons creates little discernable difference in contrast. This fact will be important later when we discuss electron beam probing.

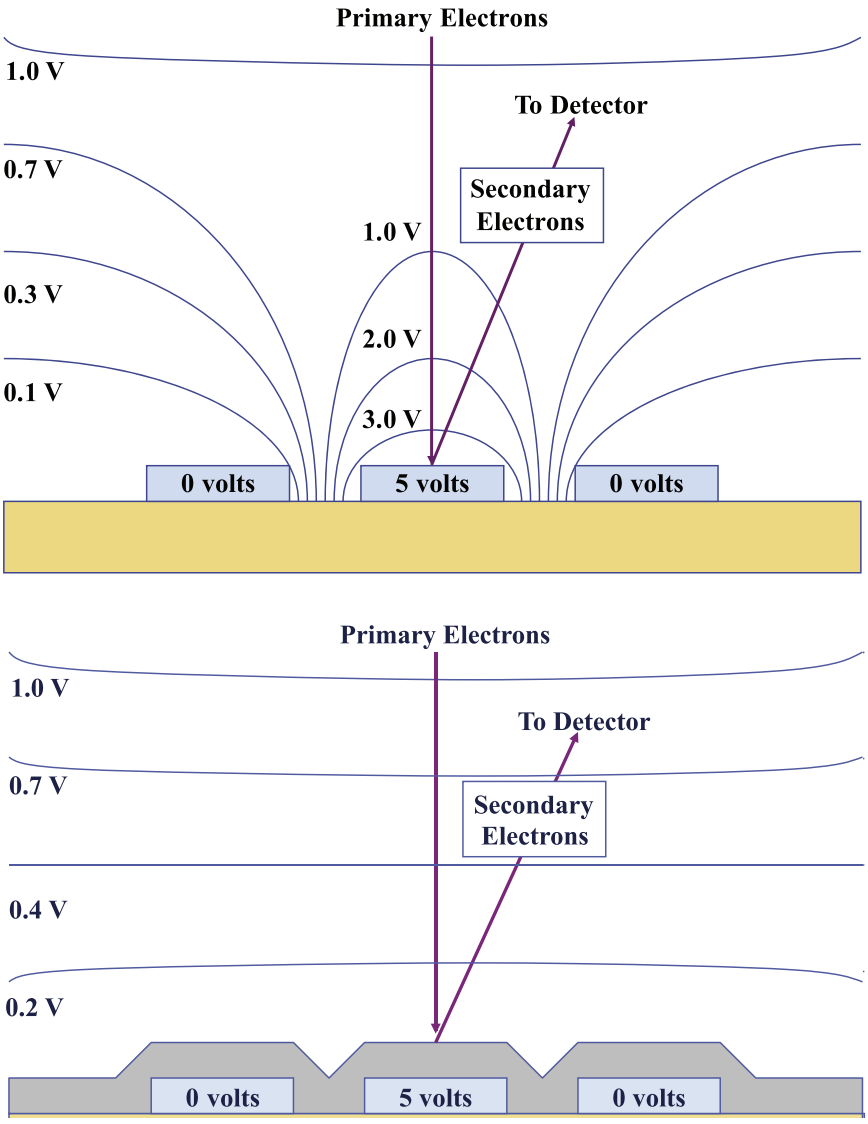


Figure 9. Principle behind biased voltage contrast, unpassivated (top) and passivated (bottom).

As the primary electrons interact with the device, secondary electrons are given off. The number of secondary electrons that make it to the detector will be a function of their energies—as we discussed in

the paragraph—a function of the position of the detector, and a function of the location where the primary electron beam strikes the sample (Figure 9 top). One should also be aware that this is for a condition where the metal conductors are exposed. If the conductors are covered by a dielectric layer, the secondary emission will be quite different. Instead of being determined by an electric field that is based on the voltages at the conductors, the secondary emission is determined by the potential on the surface of the dielectric due to charging (Figure 9 bottom). The initial opposite polarity image charge from the voltages on the conductors is replaced by a slight positive charge from the electron beam surface interaction. As a result, the voltage contrast image fades while an area is imaged.

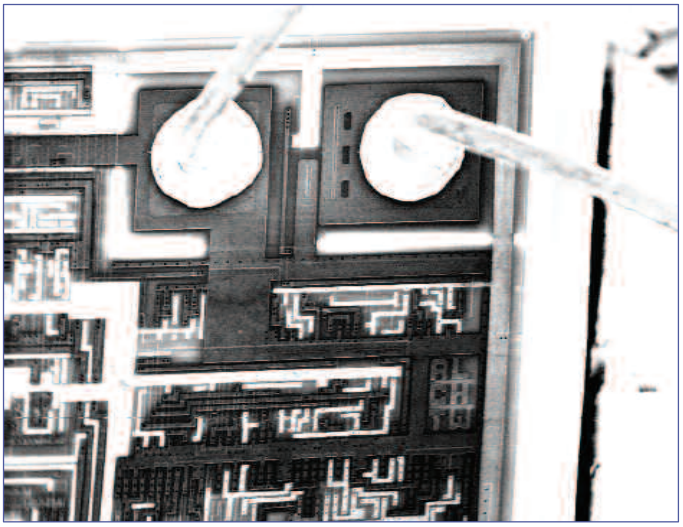


Figure 10. Biased voltage contrast—state 1.

Figure 10 shows an example image demonstrating biased voltage contrast. In this image one can see a portion of a circuit and two bond wires. The top layer of dielectric has been removed so that the voltage contrast is permanently visible. The bond wires are bright, indicating a ground potential. A portion of the interconnect is bright and a portion is dark. The bright interconnect is at ground, while the dark interconnect is at 5 volts.

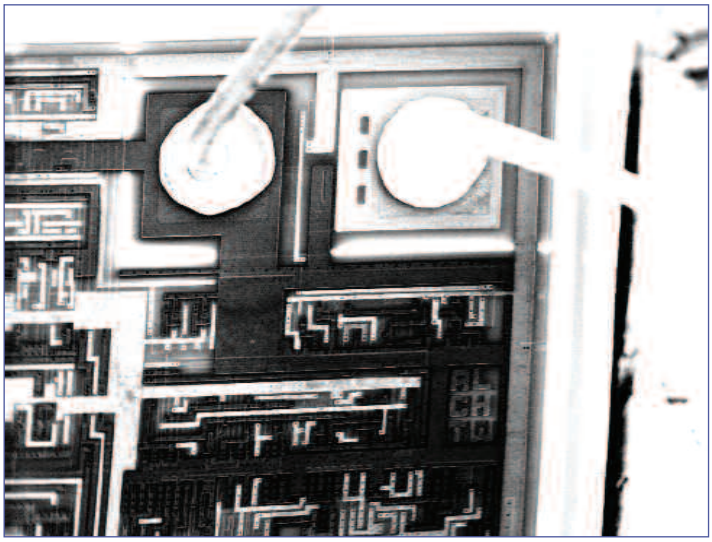


Figure 11. Biased voltage contrast—state 2.

Figure 11 is the same circuit and the same field of view with a different set of conditions applied to the pins. Note that some lines have toggled bright, while others have toggled dark.

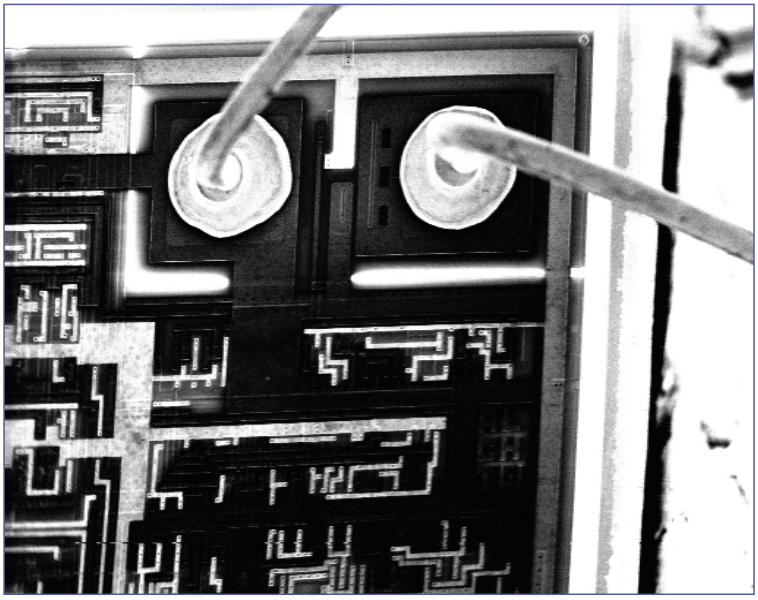


Figure 12. Biased voltage contrast—state 3.

Figure 12 is a third set of input conditions. Notice that still other lines have changed from bright to dark—or zero to 5 volts—and others have changed from dark to bright, or 5 volts to ground.

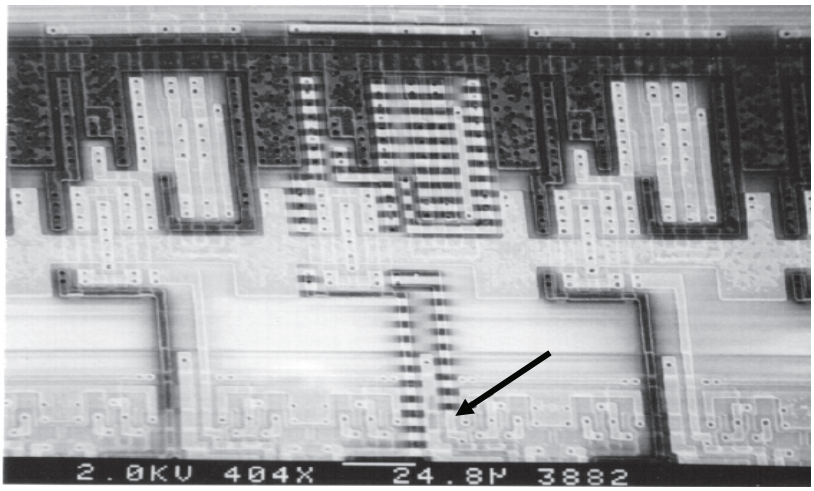


Figure 13. Biased voltage contrast—open metal line.

One technique frequently used with voltage contrast is to switch one or more inputs and then look for discontinuities in the interconnect. To perform this method, hook a function generator up to a single input pin—as shown in Figure 13—or hook a pattern generator to a group of inputs and drive a pattern design to look for defects. The interaction of the function generator with the scan rate creates the bright and dark stripes seen in the image. Some analysts refer to the phenomenon as "barber poling." The size of the

stripes can be altered by changing the frequency of the input pattern. In the image, the arrow indicates the location of the open circuit: the place where the "barber poling" stops, but the interconnect continues.

Another form of voltage contrast is capacitive coupling voltage contrast. The technique is sometimes abbreviated CCVC or called stroboscopic voltage contrast. CCVC permits imaging and measurement of dynamic voltages on structures beneath the overlying dielectric layers. The technique uses the top glass layer as a discharging capacitor. Because of the tendency for the primary beam to charge the top dielectric and remove the image charge, one must use fast scan rates and low primary beam currents. One must also create an electrical condition such that the interconnect of interest changes periodically. These requirements create tradeoffs among the signal to noise ratio, timing resolution, and length of the vector loop. We discuss those tradeoffs further in this presentation. One must pay attention to local electric fields; cross talk between adjacent interconnect can distort signals. One must also pay attention to charging and contamination. These problems can degrade or obscure the voltage contrast signals. The best policy is to use a primary electron beam of 1kV or less to avoid charging and damage.

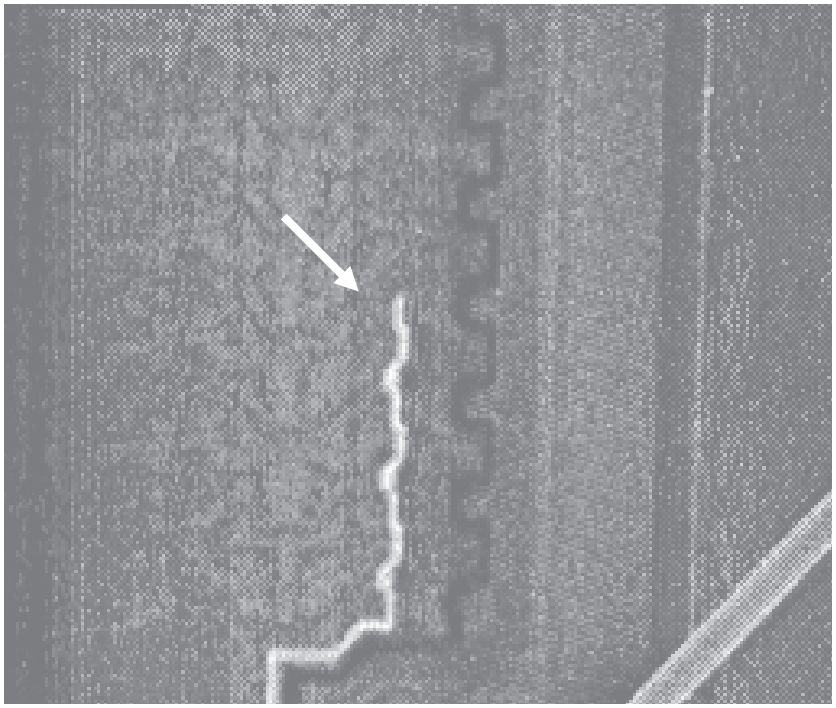


Figure 14. CCVC imaging example.

The image in Figure 14 shows an example of capacitive coupling voltage contrast. The arrow indicates the open in the interconnect line. Capacitive coupling voltage contrast images have less signal to noise than static voltage contrast images because the primary beam current must be kept low to sustain the voltage contrast effect. A low primary beam current yields a poor image at TV frame rates. Secondly, the lower signal to noise occurs because the primary beam voltage is quite low, around 1kV. The resolution of an SEM at 1kV is not as good as it is at 30kV. And three, each CCVC image is a single frame. Since the image is constantly changing, one must capture individual frames to see the image. One can increase the signal to noise ratio somewhat by averaging multiple frames during the same clock cycle in the vector set.

The technique for obtaining clearer capacitive-coupled voltage contrast images is to use a device called a beam blanker. Beam blankers are used on devices that operate at higher frequencies (greater than 1MHz). When on, the device bends the electron beam away from a sample. The beam blanker is then turned off for a particular vector, allowing the electron beam to hit the sample. If one creates a loop of vectors and ties the "off" cycle of the beam blanker to the vector of interest, an image of the circuit in a particular vector state can be created. One can then change the off state of the beam blanker to correspond to a different vector to view the logic state at that particular vector.

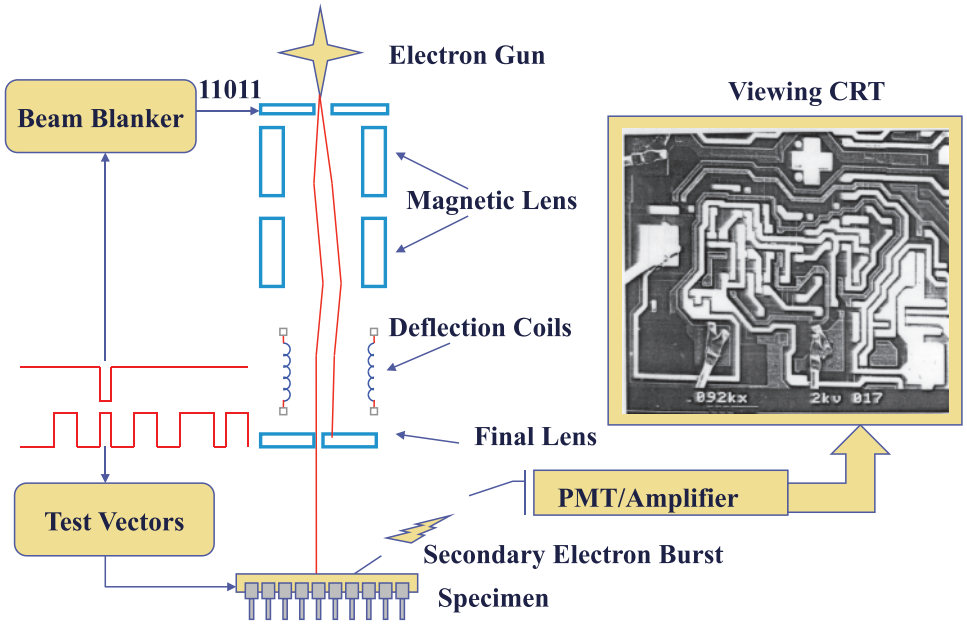


Figure 15. CCVC diagram.

If one uses a beam blanker, a pulse from the test system is used to blank the beam except for the vector of interest (Figure 15). If the beam is being blanked, the voltage in the beam blanking hardware bends the beam to one side, causing it not to go through the final aperture. If the beam blanking hardware is off, the beam travels down through the column through the final aperture, hitting the sample. From there, the secondary electrons will be collected in the photomultiplier tube and amplified to create an image similar to the one seen on the right.

The fourth variant of voltage contrast is the ability to obtain waveforms from the voltage contrast data via an electron beam probing system. Waveform measurement was developed at Cambridge in the early 1980s and incorporated into a system called the Cambridge DVCS-1500. In the mid-1980s, Neil Richardson and Stefano Concina at Schlumberger added computer-aided design navigation features and computer control to create the first modern electron beam probing system, the IDS-5000. The machines were widely used in the 1990s on one, two, and three-level metal ICs before chemical mechanical planarization and flip chip packaging made frontside analysis difficult. Part of the reason for the tools' wide acceptance in the industry is the user-friendly computer interface. Second, they could be driven using the computer-aided design database from the chip. The layout could be locked to the SEM image, which in turn could be locked to the netlist and the schematic. This feature made tracing signals much easier. Before the IDS-5000, the analyst had to trace signals on the chip by hand. The tools were used not only in failure analysis laboratories but also in design debug activities. The ability of the instrument to act

as an oscilloscope inside the chip proved invaluable to designers attempting to debug complex chip designs.

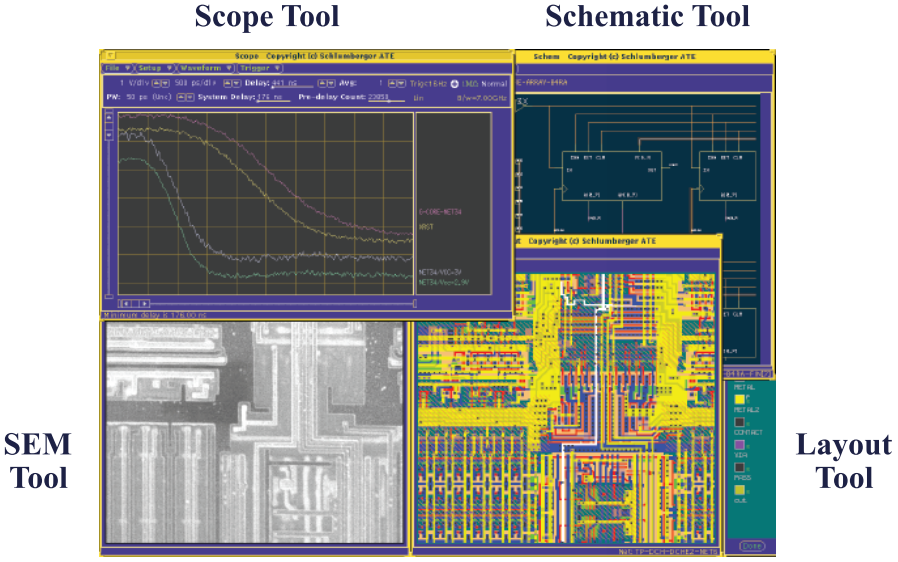


Figure 16. IDS-10k user interface.

Figure 16 is an example of the Schlumberger IDS-10000 user interface. The IDS-10k runs on Unix to take advantage of connections to computer-aided design software. The interface here shows four windows or tools. The SEM tool shows a secondary electron image of the surface of the device. At higher magnifications a spot is present that can be moved around the image and located on an interconnect segment of interest, much like one would touch a scope probe on a board trace of interest. The scope tool is an oscilloscope-like window that shows voltages as a function of time. The waveform corresponds to the location of the spot in the SEM tool window. The schematic tool shows the schematic of the device under test. The layout tool shows a CAD rendition of the area displayed in the SEM Tool.

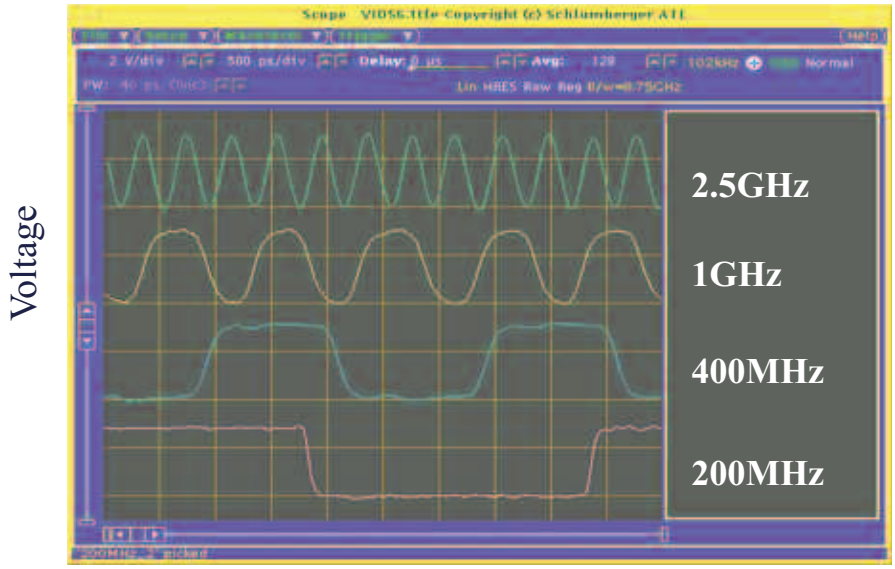


Figure 17. Electron beam waveform measurement.

Figure 17 is an example of the types of waveforms that can be obtained from an electron beam probing system. These represent waveforms under ideal conditions. The instrument is capable of approximately 50 millivolts resolution and 20 picoseconds timing accuracy. The waveforms shown here are a clock signal at 2.5GHz and three signals at 1GHz, 400MHz, and 200MHz respectively. The waveforms have a peak-to-peak voltage of 3.3 volts, the operating voltage of the 0.35µm device on which the signals were obtained.

Figure 18. Electron beam waveform measurement (practical application).

Most signals acquired on an electron beam probe system are not that clean. A number of factors can make the signals worse, including the depth of the buried conductor, probing, the proximity to adjacent conductors, and various settings on the electron beam prober itself. The waveforms shown in Figure 18 are more indicative of the types of waveforms one will see in a practical application. The waveform at the top has some noise in it. This is typical, even for a waveform that has been averaged a number of times. The waveform immediately below is the same signal, but from a line buried more deeply. In this case, the signal came from metal 5 in a six-layer metal device. It can be almost impossible to obtain a waveform from more than two levels below the surface. The green waveform shows the effects of cross talk from an adjacent line. Notice the depressed peaks indicated by the arrows. The signal at the secondary detector is being altered by an adjacent line and its electric fields. Finally, some signals can simply be too degraded to determine the behavior. In the red signal at the bottom, this is caused by a combination of system noise, depth, a long vector loop, and cross talk.

CAD navigation is an important aspect of electron beam probing and many other fault localization techniques. The technique is becoming increasingly important for complex integrated circuits for several reasons. One is that most integrated circuits are now planarized. It can be quite difficult to locate features in an SEM on a planarized IC. Another is that the feature sizes on integrated circuits are quite small.

Optical microscopy cannot resolve features below about 0.25µm. It can also be quite difficult to locate features from the backside due to wavelength limitations and substrate doping. As a result, fault localization without CAD navigation is much like driving around in an unfamiliar city without a map. Generating databases for CAD navigation is not trivial; it requires some planning upfront during the design cycle. This means that the failure analysis and design departments must coordinate the transfer of the appropriate intermediate design files. The design tools must also be compatible with the CAD navigation tools. Most CAD navigation tools use Dracula or some type of layout versus schematic routine to lock the layout to the netlist and schematic. The design department must therefore save the netlist, layout, and schematics in a form that the CAD navigation tools can use.

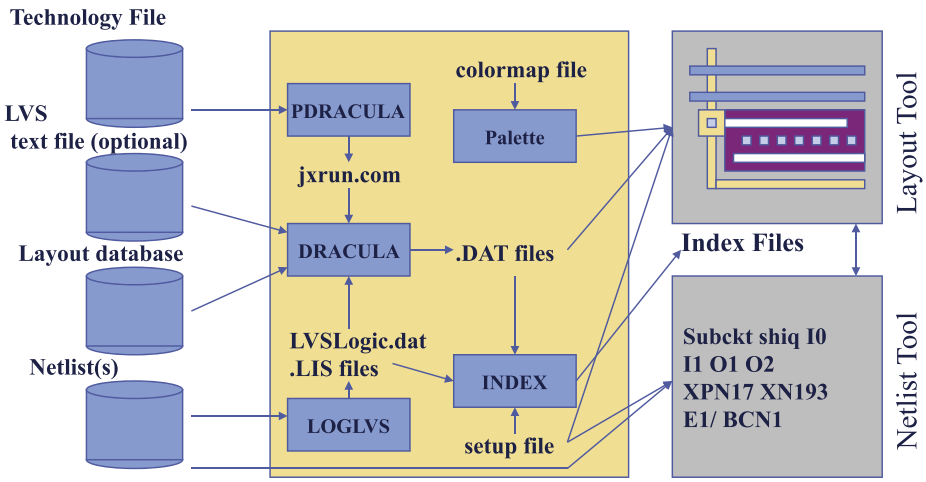


Figure 19. Setup for CAD navigation.

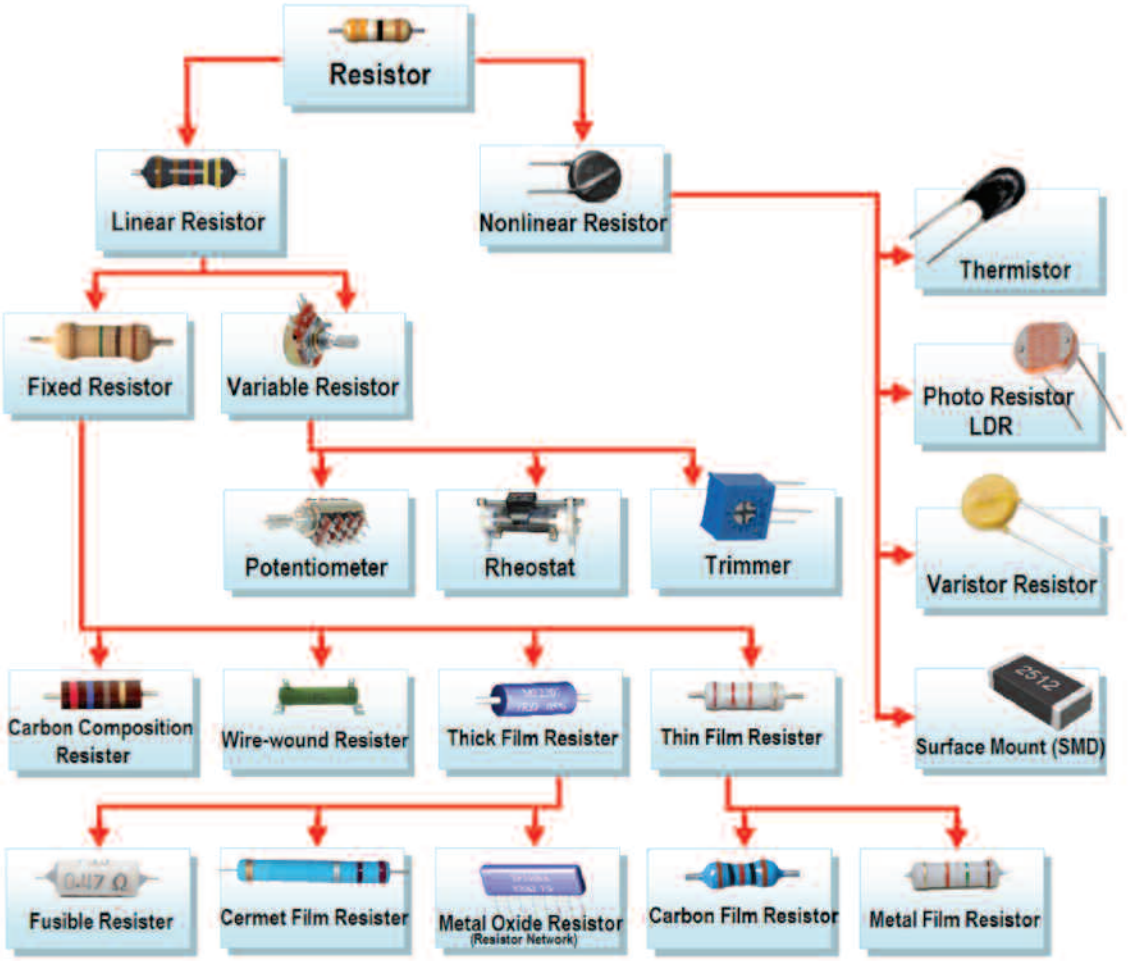
Figure 19 is a pictorial diagram of the setup process for CAD navigation. The design department will need to supply three or four main files for the process: a technology file that defines the layers and connections; an optional layout versus schematic text file that tells the computer what features constitute electrical primitives such as transistors, resistors, and diodes; the layout database that contains the polygon information for each layer; and the netlist, which contains the electrical connectivity of the primitive elements. Ideally, the design department should provide netlists and schematics before the hierarchy has been flattened to a single level to make navigation easier on complex chips. Once the files are available, they are run through a series of batch processes to link features within the layout, netlist, and schematic. The layout is processed with a colormap to make layers easily visible on the screen. Finally, the netlist is processed with an index file to complete the link with the layout.

Technical Tidbit

Resistors

This technical tidbit covers the taxonomy of resistors. Resistors are ubiquitous, even in today's advanced electronics. They play an integral role in signal integrity, protection, and signal formation, and can be used not only at the board level, but also as an element within a packaged integrated circuit.

Component suppliers manufacture resistors in several different formats. They include composition, metal or carbon film, thin film, thick film, and wire wound.



Here we show resistors by their taxonomy. Resistors can be divided into two majoring groupings: linear and non-linear. The non-linear group contains devices such as thermistors, photo-resistors, varistors, and surface mount devices. Linear resistors can be further divided into fixed and variable groupings. Variable resistors include potentiometers, rheostats, and trimmers. The fixed resistor category is the biggest, and includes carbon composition resistors, wire-wound resistors, thick film and thin film resistors. There are other sub-groups beyond what we show on this slide, but these are the major ones.

We can also divide resistors by application type. Some major groupings would include surface mount resistors, leaded resistors, high power resistors, high voltage resistors, current sense and shunt resistors, precision resistors, custom resistors, wirewound resistors, and pulse protection resistors.

Ask the Experts

Q: Is there a relationship between the EFO wand length and the lifetime of the wand?

A: Normally, the wand tip is made from a very high temperature material like iridium oxide. Although the wand length may slowly shorten over time and affect its lifetime, and another factor is the formation of bumps on the tip. This creates an irregular electric field at the tip end, causing fluctuations in the spark gap voltage. One might use the SEM to examine the end of the wand to determine how the bumps develop over time. This might allow the user to better understand the overall lifetime of the wand tip.

Spotlight: Failure and Yield Analysis

OVERVIEW

Failure and Yield Analysis is an increasingly difficult and complex process. Today, engineers are required to locate defects on complex integrated circuits. In many ways, this is akin to locating a needle in a haystack, where the needles get smaller and the haystack gets bigger every year. Engineers are required to understand a variety of disciplines in order to effectively perform failure analysis. This requires knowledge of subjects like: design, testing, technology, processing, materials science, chemistry, and even optics! Failed devices and low yields can lead to customer returns and idle manufacturing lines that can cost a company millions of dollars a day. Your industry needs competent analysts to help solve these problems. ***Advanced Failure and Yield Analysis*** is a four-day course that offers detailed instruction on a variety of effective tools, as well as the overall process flow for locating and characterizing the defect responsible for the failure. This course is designed for every manager, engineer, and technician working in the semiconductor field, using semiconductor components or supplying tools to the industry.

By focusing on a ***Do It Right the First Time*** approach to the analysis, participants will learn the appropriate methodology to successfully locate defects, characterize them, and determine the root cause of failure.

Participants learn to develop the skills to determine what tools and techniques should be applied, and when they should be applied. This skill-building series is divided into three segments:

1. **The Process of Failure and Yield Analysis.**Participants learn to recognize correct philosophical principles that lead to a successful analysis. This includes concepts like destructive vs. non-destructive techniques, fast techniques vs. brute force techniques, and correct verification.
2. **The Tools and Techniques.** Participants learn the strengths and weaknesses of a variety of tools used for analysis, including electrical testing techniques, package analysis tools, light emission, electron beam tools, optical beam tools, decapping and sample preparation, and surface science tools.
3. **Case Histories.** Participants identify how to use their knowledge through the case histories. They learn to identify key pieces of information that allow them to determine the possible cause of failure and how to proceed.

COURSE OBJECTIVES

1. The seminar will provide participants with an in-depth understanding of the tools, techniques and processes used in failure and yield analysis.
2. Participants will be able to determine how to proceed with a submitted request for analysis, ensuring that the analysis is done with the greatest probability of success.
3. The seminar will identify the advantages and disadvantages of a wide variety of tools and techniques that are used for failure and yield analysis.
4. The seminar offers a wide variety of video demonstrations of analysis techniques, so the analyst can get an understanding of the types of results they might expect to see with their equipment.
5. Participants will be able to identify basic technology features on semiconductor devices.
6. Participants will be able to identify a variety of different failure mechanisms and how they manifest themselves.
7. Participants will be able to identify appropriate tools to purchase when starting or expanding a laboratory.

INSTRUCTIONAL STRATEGY

By using a combination of instruction by lecture, video, and question/answer sessions, participants will learn practical approaches to the failure analysis process. From the very first moments of the seminar until the last sentence of the training, the driving instructional factor is **application**. We use instructors who are internationally recognized experts in their fields that have years of experience (both current and relevant) in this field. The handbook offers hundreds of pages of additional reference material the participants can use back at their daily activities.

THE SEMITRACKS ANALYSIS INSTRUCTIONAL VIDEOS™

One unique feature of this workshop is the video segments used to help train the students. Failure and Yield Analysis is a visual discipline. The ability to identify nuances and subtleties in images is critical to locating and understanding the defect. Many tools output video images that must be interpreted by analysts. No other course of this type uses this medium to help train the participants. These videos allow the analysts to directly compare material they learn in this course with real analysis work they do in their daily activities.

COURSE OUTLINE

1. Introduction
2. Failure Analysis Principles/Procedures
    a. Philosophy of Failure Analysis
    b. Flowcharts
3. Gathering Information
4. Package Level Testing
    a. Optical Microscopy
    b. Acoustic Microscopy
    c. X-Ray Radiography
    d. Hermetic Seal Testing
    e. Residual Gas Analysis
5. Electrical Testing
    a. Basics of Circuit Operation
    b. Curve Tracer/Parameter Analyzer Operation
    c. Quiescent Power Supply Current
    d. Parametric Tests (Input Leakage, Output voltage levels, Output current levels, etc.)
    e. Timing Tests (Propagation Delay, Rise/Fall Times, etc.)
    f. Automatic Test Equipment
    g. Basics of Digital Circuit Troubleshooting
    h. Basics of Analog Circuit Troubleshooting
6. Decapsulation/Backside Sample Preparation
    a. Mechanical Delidding Techniques
    b. Chemical Delidding Techniques
    c. Backside Sample Preparation Techniques

7. Die Inspection
    a. Optical Microscopy
    b. Scanning Electron Microscopy
8. Photon Emission Microscopy
    a. Mechanisms for Photon Emission
    b. Instrumentation
    c. Frontside
    d. Backside
    e. Interpretation
9. Electron Beam Tools
    a. Voltage Contrast
        i. Passive Voltage Contrast
        ii. Static Voltage Contrast
        iii. Capacitive Coupled Voltage Contrast
        iv. Introduction to Electron Beam Probing
    b. Electron Beam Induced Current
    c. Resistive Contrast Imaging
    d. Charge-Induced Voltage Alteration
10. Optical Beam Tools
    a. Optical Beam Induced Current
    b. Light-Induced Voltage Alteration
    c. Thermally-Induced Voltage Alteration
    d. Seebeck Effect Imaging
    e. Electro-optical Probing
11. Thermal Detection Techniques
    a. Infrared Thermal Imaging
    b. Liquid Crystal Hot Spot Detection
    c. Fluorescent Microthermal Imaging
12. Chemical Unlayering
    a. Wet Chemical Etching
    b. Reactive Ion Etching
    c. Parallel Polishing
13. Analytical Techniques
    a. TEM
    b. SIMS
    c. Auger
    d. ESCA/XPS
14. Focused Ion Beam Technology
    a. Physics of Operation
    b. Instrumentation
    c. Examples
    d. Gas-Assisted Etching
    e. Insulator Deposition
    f. Electrical Circuit Effects
15. Case Histories

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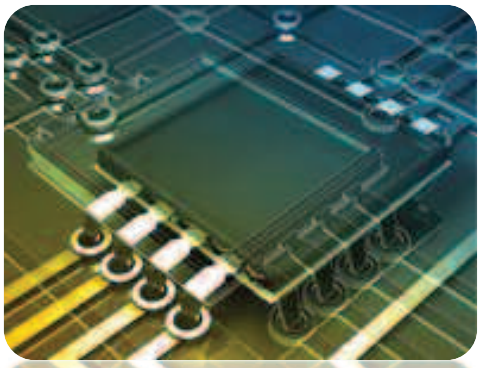
Chris Henderson

Chris would be happy to meet with you and discuss any training needs you have. Contact him at henderson@semitracks.com during the forum!



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Portland, Oregon, USA

Advanced CMOS/FinFET Fabrication
Feb 6, 2017 (Mon)
Portland, Oregon, USA

Semiconductor Statistics
Feb 7 – 8, 2017 (Tue – Wed)
Portland, Oregon, USA

Semiconductor Reliability
Mar 13 – 15, 2017 (Mon – Thur)
Singapore/Malaysia

Defect Based Testing
May 3 – 4, 2017 (Wed – Thur)
Munich, Germany

Failure and Yield Analysis
May 8 – 11, 2017 (Mon – Thur)
Munich, Germany

Semiconductor Reliability and Qualification
May 15 – 18, 2017 (Mon – Thur)
Munich, Germany

Semiconductor Statistics
May 22 – 23, 2017 (Mon – Tue)
Munich, Germany