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Leadframes—Part II

By Christopher Henderson

This article is a continuation of last month's article on leadframes.

Today, we mainly use plated leadframes. Plated leadframes can help improve adhesion of the die attach, wire bonds, and mold compound, and improve the solderability of the leadframe. The plating materials need to meet environmental regulations associated with the Removal of Hazardous Substances (RoHS) (pronounced "row-hos"), and they need to be inexpensive. RoHS requirements eliminate the possibility of lead, so that means we must use other plating materials. Figure 1 (below) shows an example of a leadframe plating system. In order to reduce costs, some companies plate the leadrame prior to stamping. This is called a pre-plated leadframe.

Figure 1. Leadframe plating system.

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Many companies use tin as a leadframe plating. The leadframe supplier deposits a plating layer between 7 and 20 microns thick. This improves solderability. However, copper-tin intermetallics can form and interfere with the reliability of the solder joint, and can aid in the growth of tin whiskers, another reliability problem. Some companies will anneal or fuse the tin plating to reduce this problem. Some companies will also use silver plating. The silver plating is on the order of 2.5 to 8 microns thick, and the assembly site deposits this after mold on the exposed portion of the leads. Some companies use a nickel-palladium-gold plating to prevent the intermetallic growth. The nickel-palladium-gold layer is quite thin, with the nickel between 0.5 and 2 microns thick, the palladium between 10 and 100 nanometers thick, and the gold only 3 to 9 nanometers thick, to reduce costs. This process is done by the leadframe supplier.

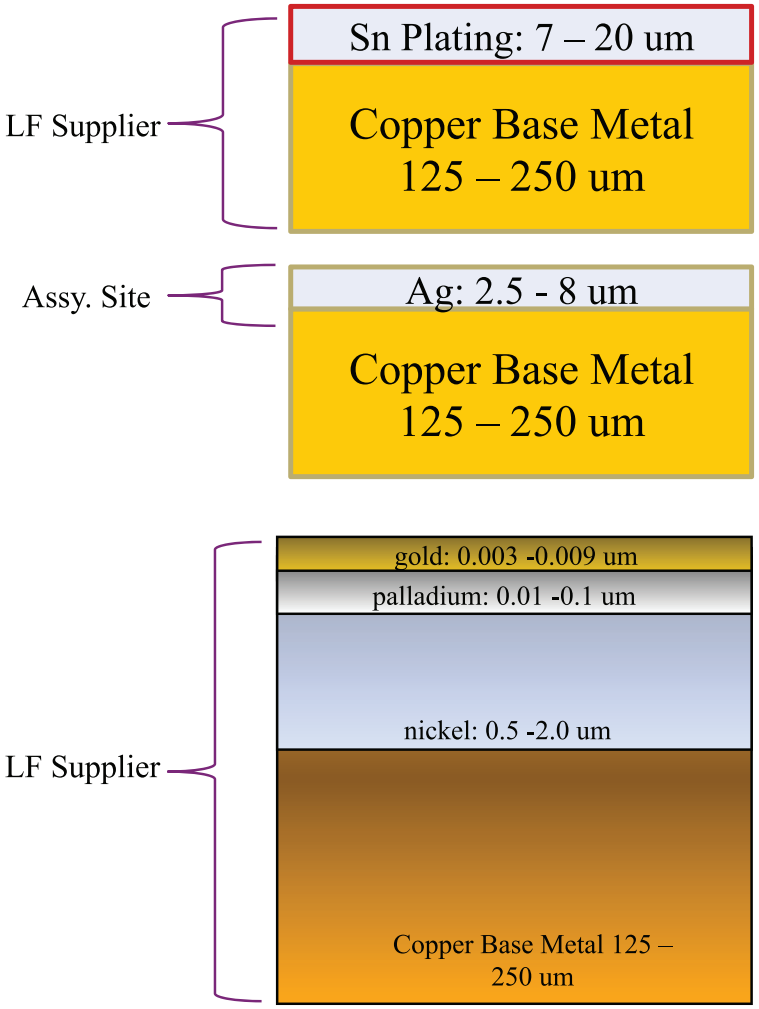


Figure 2. Drawing showing various leadframes and plating options.

One technique to improve adhesion is to change the plating finish. One can roughen the nickel layer through a chemical etch before depositing the palladium. This improves adhesion, and is particularly effective with downbonds. This is also important with copper wire since it has lower fatigue strength. However, a rough leadframe costs 15 – 30% more.

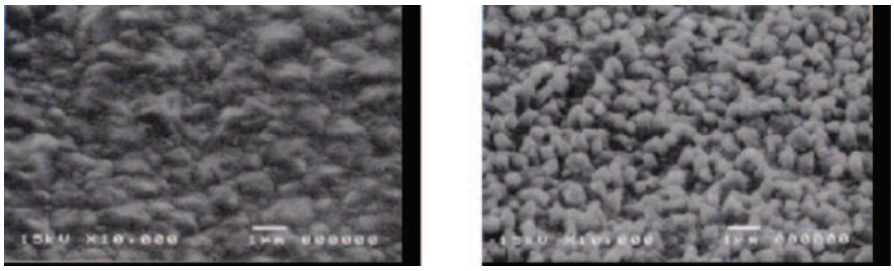


Figure 3. Standard and rough nickel-palladium-gold (NiPdAu) plating.

Rough leadframes help control mold and die attach delamination. The rough leadframe keeps the stress low on the ball and stitch bonds to prevent lifted ball and broken stitch bonds. It also protects the thermal path. Figure 4 below helps to illustrate this. The upper drawing shows a schematic cross section of the nickel-palladium-gold pre-plated leadframe, and the lower figures show scanning electron microscope (SEM) images of the standard and rough leadframes.

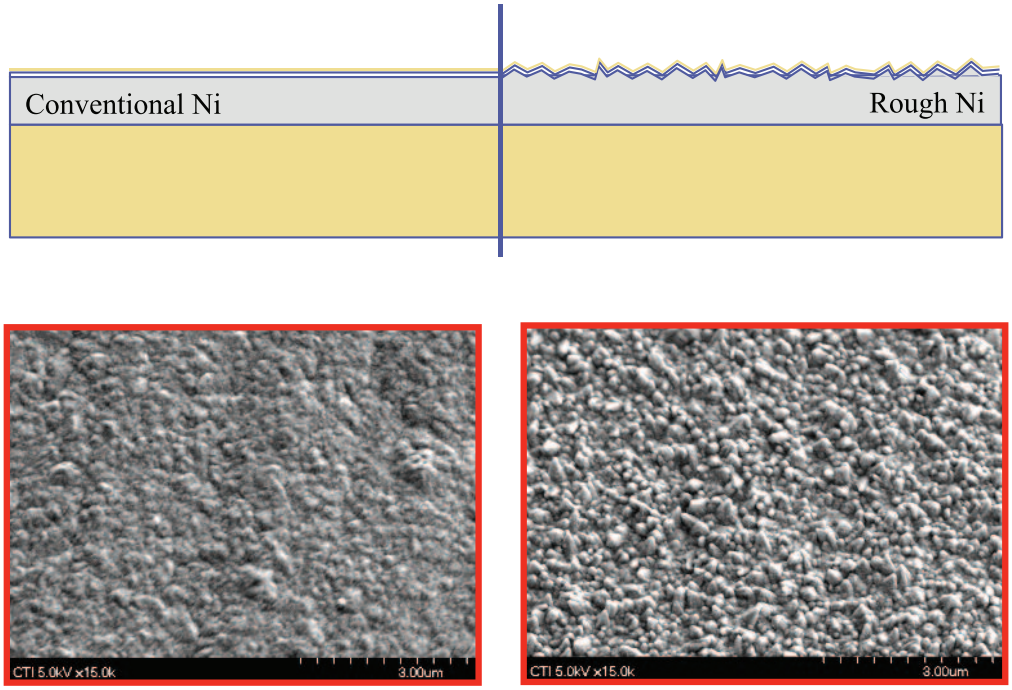
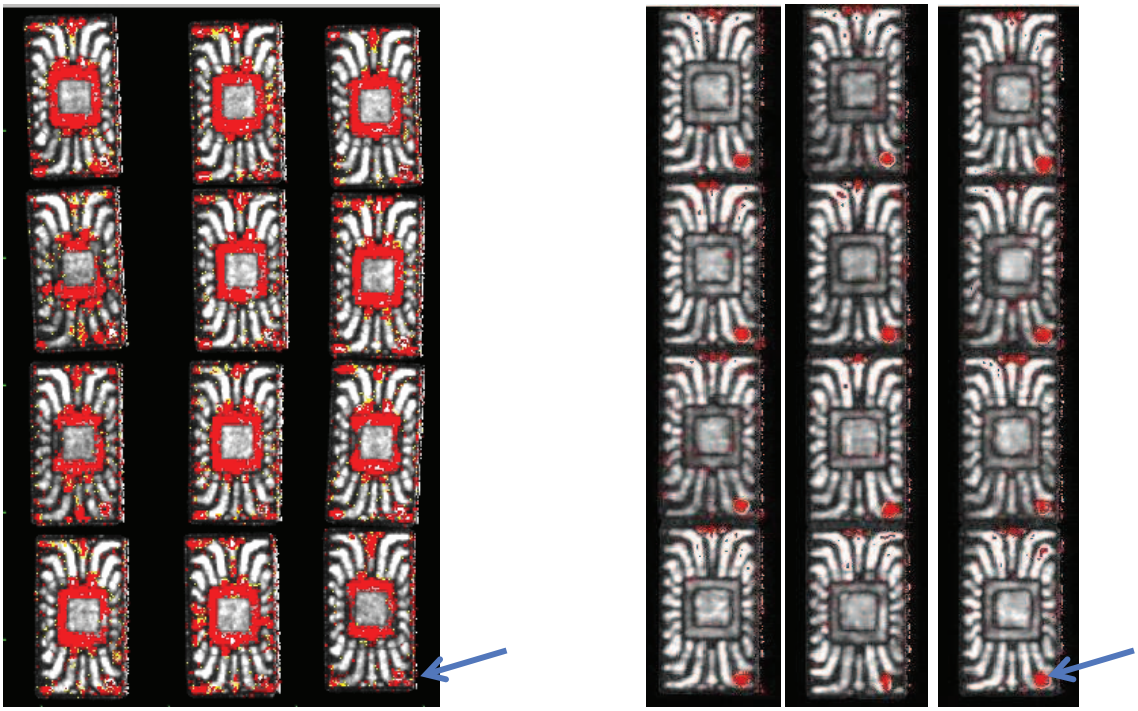


Figure 4. Drawing showing cross-section (top) and SEM images of standard and rough leadframe platings (bottom).

The scanning acoustic microscope images in Fig. 5 show how a rough leadframe can improve adhesion. The samples on the left show significant areas of red after undergoing the JEDEC Level 3 Moisture Sensitivity Stress Test. The red indicates delamination has occurred. The samples on the right show very

little delamination. The red mark on each package in the lower right corner is an artifact of the mold release process, and is not associated with leadframe delamination.



MSL3, post stress, Standard Plating MSL3, post stress, Rough NiPdAu

Figure 5. Scanning acoustic microscope images after moisture sensitivity stress on standard plating (left) and rough plating (right).

In conclusion, we briefly discussed the different types of leadframes used in packaging semiconductor devices. We learned that the industry primarily uses copper and copper alloys because of their lower resistance. We also discussed several types of platings, including tin, silver, and nickel-palladium-gold coatings, and their advantages and disadvantages. Leadframe technology is an older technology that is mature, but it is still widely used in the industry. We still make billions of devices per year with leadframes, and will continue to do so for the foreseeable future.

Technical Tidbit

IDDQ Behavior and the Curve Tracer

Quiescent Power Supply Current (IDDQ) is a powerful way to examine a component during a failure analysis effort. Many types of defects can be identified from the IDDQ signature. We won't go into why this is so here, as there is more information on this topic on our Online Training site. However, we will discuss the nature of the IDDQ measurement and what it tells us.

First, let's discuss how to make a Quiescent Power Supply Current (IDDQ) measurement on a bench setup. To perform this test, one needs a curve tracer or a parameter analyzer, a switchbox capable of connecting to the curve tracer and the device, and the device to be tested. The analyst should then place the IC in a non-contention state. A non-contention state is one where there are no transistor outputs trying to drive a logical high and a low at the same time on the same node. In order to remove the contention, it may be necessary to clock the IC or input a few vectors to the appropriate inputs. The analyst should tie all of the inputs to either V_{DD} or V_{SS}, float all of the outputs, and sweep the voltage on the V_{DD} side from the maximum rated supply voltage down to zero. This will yield a curve similar to the curve shown in the lower left portion of this slide.

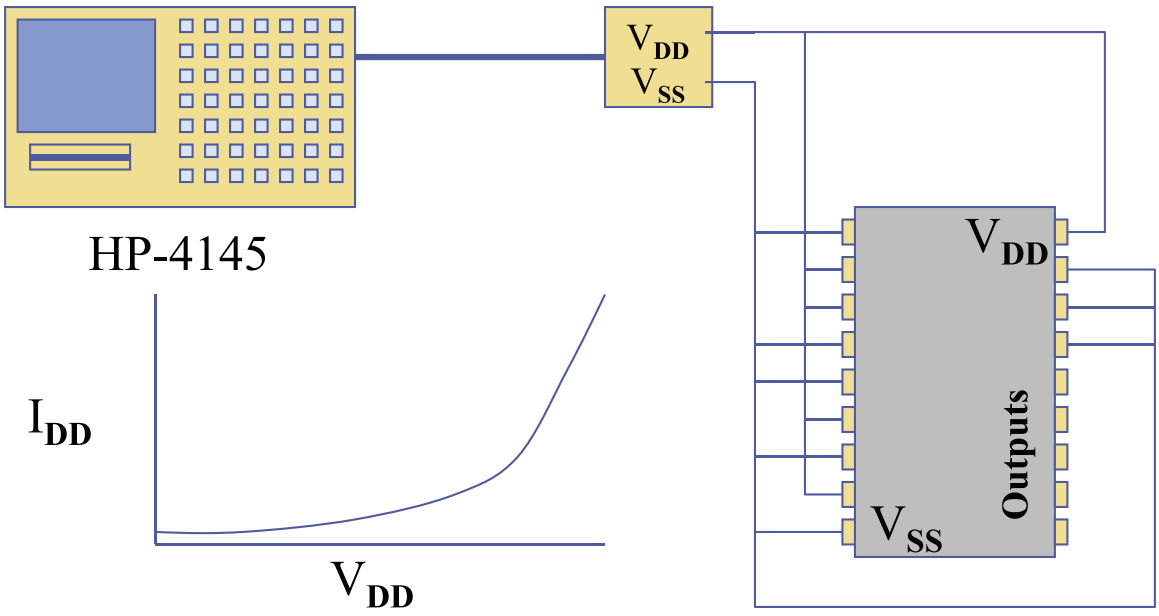


Figure 1. Basic setup for IDDQ on a curve tracer.

Figure 2 shows some actual examples of I_{DD}-V_{DD} curves. These are all taken from microprocessor analysis work done several years ago. The microprocessors are 0.5µm CMOS circuits with approximately 800,000 transistors. The curve on the upper left has an obvious parabolic shape to it. Subsequent failure analysis localized the problem to a gate oxide short in an n-channel transistor within the random logic. The curve on the upper right shows a linear shape. In this case, the defect was localized to a high

resistance short between V_{DD} and V_{SS} In the example in the lower left, the I_{DD}-V_{DD} curve exhibits an exponential characteristic. The current is well within the specified limits at 3.3 volts and 5.0 volts, but it increases rapidly at about 5.5 volts, somewhat sooner than a defect-free circuit. This leakage is due to a soft pn junction, and possibly attributable to electrostatic discharge damage. The I_{DD}-V_{DD} curve on the lower right has an erratic shape to it. We created the I_{DD}-V_{DD} curve by sweeping from the supply voltage down to zero. Notice that the current starts at a low value, then jumps high. It then meanders erratically downward until about 1 volt, where it then drops to a low value. An erratic, time-varying current is indicative of an open circuit defect.

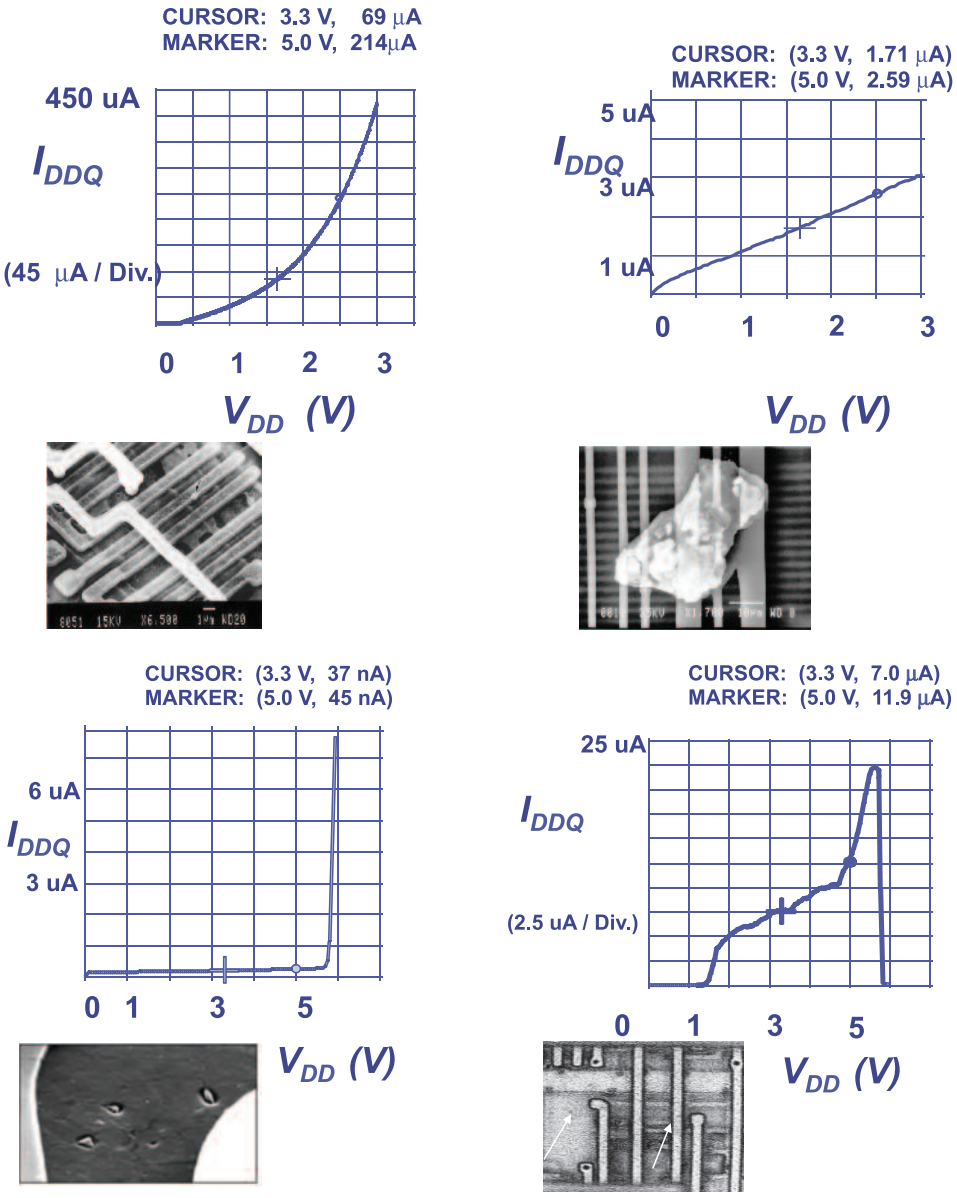


Figure 2. IDD-VDD curves associated with various defects. Gate oxide short (upper left), VDD-VSS bridging short (upper right), ESD damage causing soft breakdown (lower left), and open vias (lower right).

Ask the Experts

Q: How accurate is an IDDQ vs. VDD curve trace in determining the actual defect on an IC?

A: We actually discuss this test and defects in this month's Technical Tidbit. IDDQ vs. VDD can help the analyst separate opens from shorts, and identify various types of shorts, but the accuracy level is only around 85% or so. Although IDDQ is a great test for establishing the direction of an analysis, it is even less accurate by itself in determining what the actual defect will be. One will need further analysis to identify the actual defect.

Spotlight: Process Integration Short Course

OVERVIEW

Semiconductor and integrated circuit developments continue to proceed at an incredible pace. For example, today's microprocessor chips have one thousand times the processing power of those a decade ago. These challenges have been accomplished because of the integrated circuit industry's ability to track something known as Moore's Law. Moore's Law states that an integrated circuit's processing power will double every two years. This has been accomplished by making devices smaller and smaller. The question looming in everyone's mind is "How far into the future can this continue?" ***CMOS and BiCMOS Process Integration*** is a five-day course that offers detailed instruction on the physics behind the operation of a modern integrated circuit, and the processing technologies required to make them. We place special emphasis on current issues related to designing and manufacturing the next generation devices. This course is a must for every manager, engineer and technician working in the semiconductor industry, using semiconductor components or supplying tools to the industry.

By focusing on the fundamentals of transistor operation and interconnect performance, participants will learn why advances in the industry are occurring along certain lines and not others. Our instructors work hard to explain how semiconductor devices work without delving heavily into the complex physics and mathematical expressions that normally accompany this discipline.

Participants learn basic but powerful aspects about the semiconductor industry. This skill-building series is divided into four segments:

1. **Basic Device Operation.** Participants learn the fundamentals of transistor operation. They learn why CMOS (Complimentary Metal Oxide Semiconductor) devices dominate the industry today
2. **Fabrication Technologies.** Participants learn the fundamental manufacturing technologies that are used to make modern integrated circuits. They learn the typical CMOS and BiCMOS process flows used in integrated circuit fabrication.
3. **Current Issues in Process Integration.** Participants learn how device operation is increasingly constrained by three parameters. They also learn about the impact of using new materials in the fabrication process and how those materials may create problems for the manufacturers in the future.
4. **An Overview of Issues Related to Process Integration.** Participants learn about the image of new materials, yield, reliability and scaling on technology and process integration. They receive an overview of the major reliability mechanisms that affect silicon ICs today.

COURSE OBJECTIVES

1. The seminar will provide participants with an in-depth understanding of the semiconductor industry and its technical issues.
2. Participants will understand the basic concepts behind transistor operation and performance.
3. The seminar will identify the key issues related to the continued growth of the semiconductor industry.

4. The seminar offers a wide variety of sample problems that participants work to help them gain knowledge of the fundamentals of device operation and manufacturing.
5. Participants will be able to identify basic and advanced technology features on semiconductor devices. This includes features like silicon-germanium, strained silicon, copper, and low-k dielectrics.
6. Participants will understand how reliability, power consumption and device performance are interrelated.
7. Participants will be able to make decisions about how to construct and evaluate new CMOS, BiCMOS, and bipolar technologies.

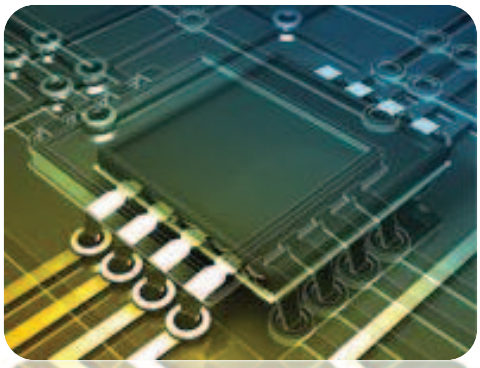
INSTRUCTIONAL STRATEGY

By using a combination of instruction by lecture, classroom exercises, and question/answer sessions, participants will learn practical information on semiconductor devices and the operation of this industry. From the very first moments of the seminar until the last sentence of the training, the driving instructional factor is **application**. We use instructors who are internationally recognized experts in their fields that have years of experience (both current and relevant) in this field. The handbook offers hundreds of pages of additional reference material the participants can use back at their daily activities.

COURSE OUTLINE

1. Introduction
2. Conventional CMOS
   a. Key Components and Parameters
   b. Process Overview and Integration Issues
   c. Scaling and Limitations
3. Mobility Enhancement Techniques
   a. Strained Silicon
   b. Crystal Orientation
4. Gate Stacks, High-k Dielectrics
   a. Gate Conductor Materials and Properties
   b. High-k Materials and Properties
   c. Gate Stack Integration
5. Options for Source-Drain, Extensions
   a. Elevated Source/Drain
   b. Co-Implantation of Inactive Species
   c. Schottky-Barrier Source-Drain

6. Three-Dimensional Structures
    a. FinFETs, Multi-Gates
7. Interconnects
    a. Aluminum Interconnects, Issues
    b. Copper Interconnects, Issues
    c. Low-k Dielectrics
8. Conventional BiCMOS
    a. Bipolar Transistor Fundamentals
    b. BiCMOS Process Overview
    c. Scaling and Limitations
9. Bipolar Enhancement Techniques
    a. SiGe
    b. SiGe:C
10. CMOS/BiCMOS Reliability Considerations
    a. Electrostatic Discharge
    b. Electromigration and Stress Migration
    c. Soft Errors, Plasma Damage
    d. Dielectric Reliability
    e. Bias Temperature Instabilities
    f. Hot Carrier Reliability
    g. Burn-In
11. Yield Considerations
    a. Yield Detractors
    b. Models
    c. Monitors



Feedback

If you have a suggestion or a comment regarding our courses, online training, discussion forums, or reference materials, or if you wish to suggest a new course or location, please call us at 1-505-858-0454 or Email us (info@semitracks.com).

To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered in the next newsletter, please contact Jeremy Henderson by Email (jeremy.henderson@semitracks.com).

We are always looking for ways to enhance our courses and educational materials.

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For more information on Semitracks online training or public courses, visit our web site!

http://www.semitracks.com

To post, read, or answer a question, visit our forums.
We look forward to hearing from you!

Upcoming Courses

(Click on each item for details)

ESD Design and Technology
February 11 – 13, 2014 (Tue – Thur)
San Jose, California, USA

Semiconductor Reliability
February 11 – 13, 2014 (Tues – Thur)
San Jose, California, USA

Failure and Yield Analysis
February 17 – 20, 2014 (Mon – Thur)
San Jose, California, USA

Wafer Fab Processing
February 18, 2014 (Tue)
San Jose, California, USA

Microelectronic Defect, Fault Isolation and Failure Analysis
February 19 – 21, 2014 (Wed – Fri)
Malaysia

Microelectronic Defect, Fault Isolation and Failure Analysis
February 24 – 26, 2014 (Mon – Wed)
Singapore

CMOS, BICMOS and Bipolar Process Integraion
March 25 – 26, 2014 (Tue – Wed)
Austin, Texas, USA