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InfoTracks

Semitracks Monthly Newsletter

Failure Analysis Procedures – Part II

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This article is a continuation of last month's article. As we discussed last month, sometimes failure analyst's can best understand the FA procedure for a component by thinking about the process in terms of the type of failure. This is a flowchart that describes how to analyze a scan-based failure at the wafer level.

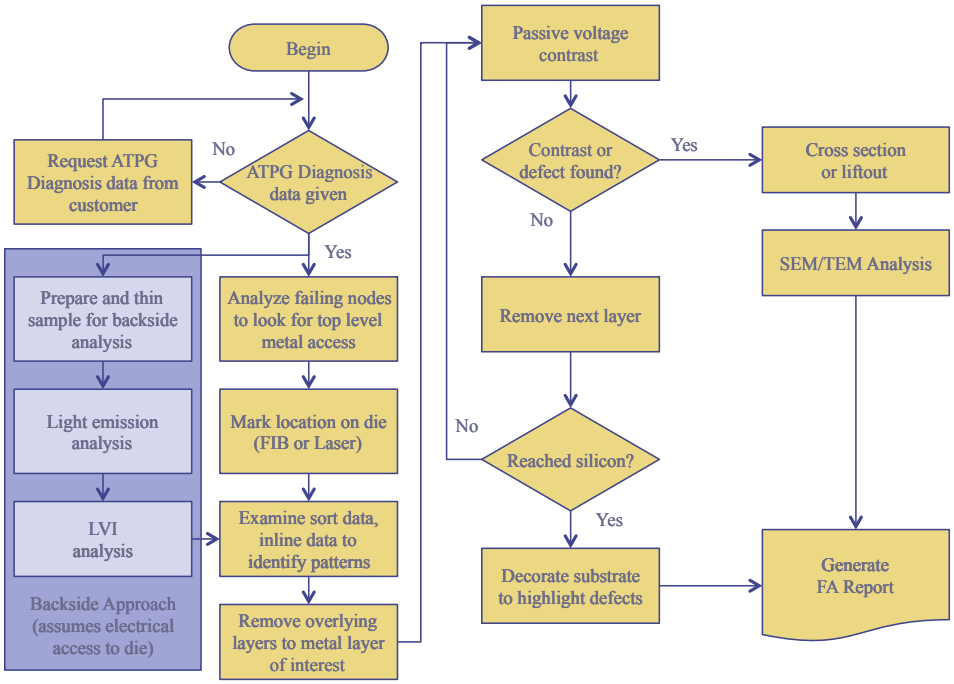


Figure 1. Flowchart for a scan-based failure.

In this Issue:

We begin with the Automatic Test Pattern Generation (ATPG) Diagnosis data. This information comes from EDA tools like TetraMax™ from Synopsys, Encounter Test™ from Cadence, or Mentor Graphics' tool Tessent™. Test engineers will sometimes run these routines on failures to help with the diagnosis process. If this data is not available, one should request it from the customer. Without this information, it can be quite difficult to troubleshoot a scan-based failure. Today's complex components practically require this approach to the analysis. Without assistance from the electrical test data, the analyst must resort to hunting for what amounts to a needle in a haystack. Each year, the needles get smaller and the haystack gets larger!

If we have the data, or once we have the data, we can analyze the failing candidate nodes to see if there is top-level metal access. We can examine the GDSII files for this information. The higher in the metal stack the defective candidate appears, the less parallel polishing we need to perform to access the layer. Once we have identified candidate locations to examine, we can mark the locations on the die with a focused ion beam or laser system. This point in the analysis also provides a good opportunity to examine the sort data, inline data, and other data items for clues as to where the failure might be occurring and why. Next we remove the overlying layers to expose the metal layer of interest. Ideally, this metal layer is the uppermost layer in the defective node. With this metal layer exposed, we can perform passive voltage contrast. Passive voltage contrast can be used to identify opens and shorts. If we don't see incorrect contrast, then we can remove the chip layers down to the next metal layer in the node, or down to the uppermost metal layer in the next candidate. We would continue this process down through the backend of the process, or through the interconnect and dielectric layers. Once we see incorrect contrast or the defect itself, we can determine if we need further analysis. This might involve a cross-section or TEM liftout. We can then examine the defect with the SEM or TEM as appropriate. If we do not see the defect after removing all of the interconnect and dielectric layers, we can decorate the substrate to highlight potential defects in the silicon. At this point, we can write up our findings in a failure analysis report.

The flow shown in the gold flowchart shapes assumes that we do not have electrical access to the die for testing in conjunction with failure analysis techniques. If we were to have access to wafer-level test with failure analysis lab tools, then it may make sense to perform the analysis from the backside. We show this alternate flow in the blue-gray color. We can thin the sample to around 100µm to provide better transmission of the laser signals and light emission. Once we have the sample thinned, we can use techniques like Light Emission and Laser Voltage Imaging to provide additional diagnosis capability. After the Laser Voltage Imaging Analysis, we will need to return to the main flow to expose the defect. Depending on the results of the LVI and Light Emission analysis, we may have identified a metal interconnect segment, via, contact, or transistor to examine further. This might mean we return to the main flow at a different point than shown here in the flowchart.

Although flowcharts provide only a moderate degree of help for specific analysis cases, they do provide a high-level overview of the process. One can construct more specific flowcharts that account for the equipment available for analysis, the circuits to be analyzed, and the importance level of the analysis. High level-flowcharts can also suggest other techniques that might not be available in one's laboratory, but should be considered.

Technical Tidbit

Palladium-Coated Copper Wire for Bonding

In order to improve the manufacturing process with copper wire, some manufacturers are experimenting with and implementing palladium-coated copper wire. One big reason we might consider palladium-coated copper wire is to reduce oxidation. Copper wire oxidizes in an oxygen environment (like an open assembly test area) so one solution is to coat the wire with an element like palladium. The palladium needs to be the thick enough to prevent oxidation, but thin enough to prevent changes in wire behavior, like changes in resistance, flexibility, intermetallic formation, and so on. The big advantage of palladium-coated copper wire is that the shelf life for wire bonding applications is weeks, rather than days for bare copper wire.

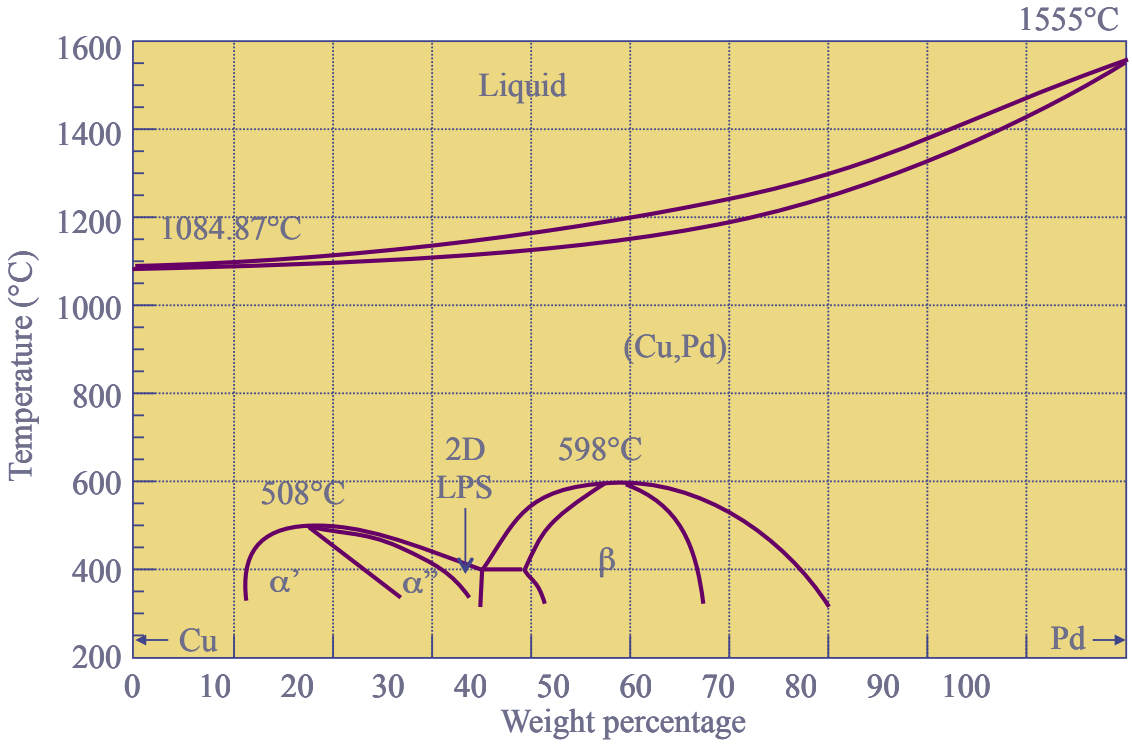
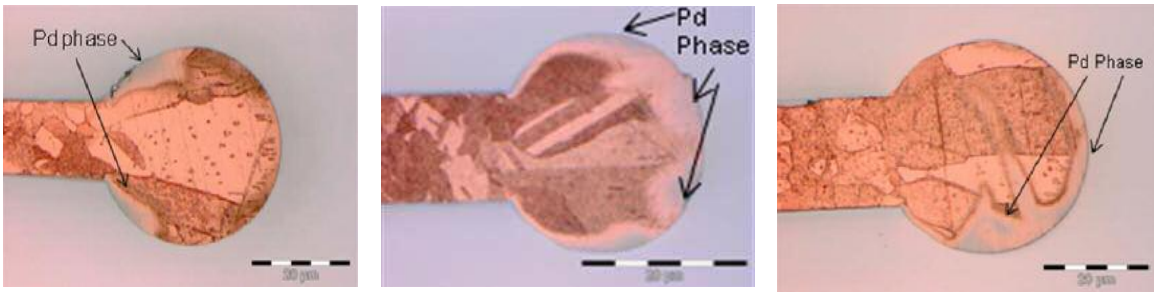


Figure 1. Phase Diagram for Copper-Palladium

If we look at the phase diagram for palladium and copper, we can see why some of the problems exist. Palladium is a substitutional element in the copper lattice. If we have a 25µm diameter wire with a 0.1µm palladium coating, then this translates to a 2.2 percent atomic concentration of palladium in copper. This substitution will raise the Vicker's Hardness Number of the copper by about 5. The solidus and liquidus lines are close to one another. Furthermore, turbulent mixing of the elements occurs during the heating phase. This leads to situations where the two elements can erratically segregate in the free air ball.



30mA 60mA 120mA

Figure 2. Cross-section images of copper-palladium Free Air Balls under various currents (images courtesy Kulicke and Soffa).

Figure 2 shows segregation of the palladium in the free air ball. Notice that we don't form alloys; the copper and palladium exist as separate elements up to the liquid phase. Also notice that at low currents, or less heat, the palladium tends to clump into smaller regions. The grey areas indicate palladium-rich areas. At higher currents, the palladium does mix more randomly and deeper into the free air ball itself. In general, the mixing leads to higher hardness of the ball itself, making bonding more problematic.

The electronic flame off (EFO) procedure needs to be modified for palladium-coated copper. Palladium has a higher melting point than copper, so the palladium doesn't form a solid solution with the copper. Therefore, the free air ball doesn't contain uniformly distributed palladium. Engineers can adjust the profile of the EFO to create a free air ball with palladium on the surface. The properties of the free air ball depend on many factors including the flow rate of oxidation protection gas, the EFO current, the firing time and the gap between the tip of wire and the EFO wand. With a proper EFO, one can improve the corrosion resistance as compared to a bare copper ball. Some researchers have reported that one can form EFO ball in pure nitrogen without requiring forming gas.

There are some consequences to switching to palladium-coated copper. Copper wire is not a ductile as gold wire, so package flexing becomes more of an issue. Package flexing can lead to loss of adhesion and wire fatigue near the stitch bond on the package lead frame.

Although there are some concerns, the palladium coating not only reduces oxidation, but it can also improve corrosion resistance, which can improve packaging reliability in environments where moisture might be a concern.

[1] H. Clauberg, et. al., "Wire Bonding with Pd-Coated Copper Wire," IEEE CPMT Symposium Japan, pp. 1 – 4, 2010.

[2] L. J. Tang, et. al., "Pitfalls and Solutions of Replacing Gold Wire with Palladium Coated Copper Wire in IC Wire Bonding," IEEE ECTC, pp. 1673 – 1678, 2011

Ask the Experts

Q: MM and HBM are common requirements for our products (power amplifiers/low noise amplifiers), but is CDM also a must during qualification?

A: CDM is an important test method when the products you produce will go through a lot of automated assembly and testing. I am not sure if that is the case for your products. You may have to check with your product engineers to determine which markets your parts go into. In general, power amplifiers would not be as sensitive to CDM damage as low noise amplifiers, but most amplifiers have ESD-sensitive inputs.

Spotlight on our Courses: Yield Analysis

Solving Yield Problems is one of the most critical activities facing today's foundries and fabless semiconductor companies. In conjunction with SEMI, we identified this topic as a growing and critical need for the industry. We have revamped the course into a shorter, more focused course for engineers dealing with yield problems within fabless semiconductor companies, and engineers developing yield analysis tools and techniques within the EDA community. If you are interested in attending this course, or if you are interested in having this done as an in-house course for your staff, please feel free to contact us at (505) 858-0454, or at info@semitracks.com.

COURSE OVERVIEW

Yield Analysis is an increasingly difficult and complex process. Today, engineers are required to locate defects on complex integrated circuits. In many ways, this is akin to locating a needle in a haystack, where the needles get smaller and the haystack gets bigger every year. This is made even more complex by the tremendous amount of data produced by fab tools and test systems. Engineers are required to understand a variety of disciplines in order to effectively perform yield analysis. This requires knowledge of subjects like: design, testing, technology, processing, materials science, data mining, and statistics. Low yields on a high volume manufacturing line can cost a company millions of dollars a day. Your industry needs competent analysts to help solve these problems. ***Yield Analysis*** is a 1-day course that offers detailed instruction on a variety of effective tools, as well as the overall process flow for identifying, locating and characterizing the defects responsible for the low yields. This course is designed for every manager, engineer, and technician working in the semiconductor field, using semiconductor components or supplying tools to the industry.

Participants learn to develop the skills to determine what tools and techniques should be applied, and when they should be applied. This skill-building series is divided into three segments:

1. **The Process of Yield Analysis.** Participants learn to recognize correct philosophical principles that lead to a successful analysis. This includes concepts like destructive vs. non-destructive techniques, fast techniques vs. brute force techniques, and correct verification.
2. **Data Mining Techniques.** Participants learn the strengths and weaknesses of data mining tools used for analysis, including electrical testing techniques, defect inspection tools, wafer map data, and correlation techniques.
3. **Case Histories.** Participants identify how to use their knowledge through the case histories. They learn to identify key pieces of information that allow them to determine the possible cause of failure and how to proceed.

COURSE OBJECTIVES

1. The seminar will provide participants with an in-depth understanding of the tools, techniques and processes used in yield analysis.
2. Participants will be able to determine how to proceed with a submitted request for analysis, ensuring that the analysis is done with the greatest probability of success.
3. The seminar will identify the advantages and disadvantages of a wide variety of tools and techniques that are used for yield analysis.
4. The seminar offers a wide variety of video demonstrations of analysis techniques, so the analyst can get an understanding of the types of results they might expect to see with their equipment.
5. Participants will be able to identify basic yield models and equations and their applicability to a variety of semiconductor devices.
6. Participants will be able to identify a variety of different failure mechanisms and how they manifest themselves.
7. Participants will be able to identify appropriate tools to purchase when starting or expanding a laboratory.

INSTRUCTIONAL STRATEGY

By using a combination of instruction by lecture, video, and question/answer sessions, participants will learn practical approaches to the failure analysis process. From the very first moments of the seminar until the last sentence of the training, the driving instructional factor is **application**. We use instructors who are internationally recognized experts in their fields that have years of experience (both current and relevant) in this field. The handbook offers hundreds of pages of additional reference material the participants can use back at their daily activities.

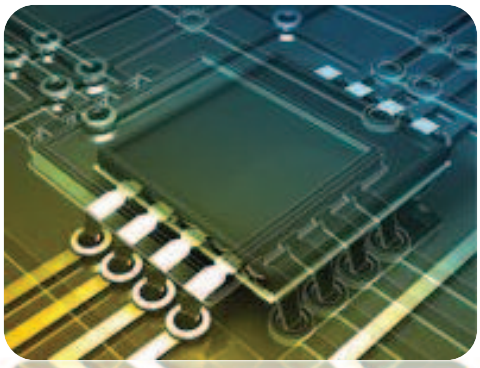
THE SEMITRACKS ANALYSIS INSTRUCTIONAL VIDEOS™

One unique feature of this workshop is the video segments used to help train the students. Yield Analysis is a visual discipline. The ability to identify nuances and subtleties in images is critical to locating and understanding the defect. Many tools output video images that must be interpreted by analysts. No other course of this type uses this medium to help train the participants. These videos allow the analysts to directly compare material they learn in this course with real analysis work they do in their daily activities.

COURSE OUTLINE

(Lecture Time 8 hours)

1. Introduction
2. Yield Analysis Principles/Procedures
   a. Philosophy of Yield Analysis
   b. Flowcharts
3. Models for Yield Prediction
   a. Poisson
   b. Murphy
   c. Seeds
   d. Bose-Einstein
   e. Other treatments
   f. In-class Exercises: Yield Calculations
4. Gathering Information
5. Test Structures
6. Yield Enhancement Techniques
   a. Random Defects
   b. Systematic Defects
7. Defect Analysis and Yield Loss
   a. Defects in Silicon Devices
      i. Front End of the Line
      ii. Back End of the Line
   b. Design/Manufacturing Interactions
   c. Process Variations
   d. Which Defects Cause Yield Loss
   e. Kill Ratio of Defects
8. Data Mining
   a. Electrical Data
   b. Metrology
   c. Wafer Maps/Spatial Data
   d. Correlation Techniques
9. Overview of Electrical Testing
10. Failure Analysis Techniques Overview
    a. Optical/SEM Inspection
    b. Fault Isolation Techniques (Light Emission, TIVA, PVC, EBIC, others)
    c. Analytical Techniques (TEM, AFM, EDS, SIMS, Auger, EELS, others)
11. Root Cause Analysis
12. Case Histories



Feedback

If you have a suggestion or a comment regarding our courses, online training, discussion forums, or reference materials, or if you wish to suggest a new course or location, please call us at 1-505-858-0454 or Email us (info@semitracks.com).

To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered in the next newsletter, please contact Jeremy Henderson by Email (jeremy.henderson@semitracks.com).

We are always looking for ways to enhance our courses and educational materials.

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For more information on Semitracks online training or public courses, visit our web site!

http://www.semitracks.com

To post, read, or answer a question, visit our forums.
We look forward to hearing from you!

Upcoming Courses

(Click on each item for details)

Fault Isolation
January 21 – 23, 2013 (Mon – Wed)
Penang, Malaysia

Semiconductor Reliability
January 23 – 25, 2013 (Wed – Fri)
San Jose, California

Failure and Yield Analysis
January 28 – 31, 2013 (Mon – Thur)
San Jose, California

EOS, ESD and How to Differentiate
February 4 – 5, 2013 (Mon – Tues)
San Jose, California

Polymers in Electronics / FTIR
February 4 – 5, 2013 (Mon – Tues)
San Jose, California

Upcoming Webinars

(Click on each item for details)

An Overview of the Semitracks Online Training System
February 7, 2013 (Thu) • 11:00 A.M. EST