ISSUE #169
August 2023

SEMITRACKS, INC.

INFOTRACKS

YOUR MONTHLY LOOK INSIDE SEMICONDUCTOR TECHNOLOGY

Semiconductor Cleanroom Technology

By Christopher Henderson

In this month's Feature Article, we will continue our discussion of filtration as it applies to Semiconductor Cleanroom Technology. The ability to effectively filter particles from the atmosphere is the hallmark of a cleanroom, so we will discuss the types and specifications of HEPA filters used in semiconductor manufacturing.

Figure 1 shows collection efficiencies for a single fiber. Notice that the collection efficiency for both impaction and interception fall off as the particle size decreases. This is due to the fact that the cross-sectional area of the particles becomes insufficient for the fibers to present a barrier to their movement, or even affect their movement. On the other hand, diffusion collection efficiency increases as the particle size decreases, since the collisions with the air molecules scatter the particulate, increasing their chance of adhering to the fiber mesh.

WHAT'S INSIDE?

Want to take control of your learning? See page 08

Upcoming Courses:

- Product Qualification Overview
- Advanced CMOS/FinFET Fabrication
- IC Packaging Design and Modeling

See page 12 for more details

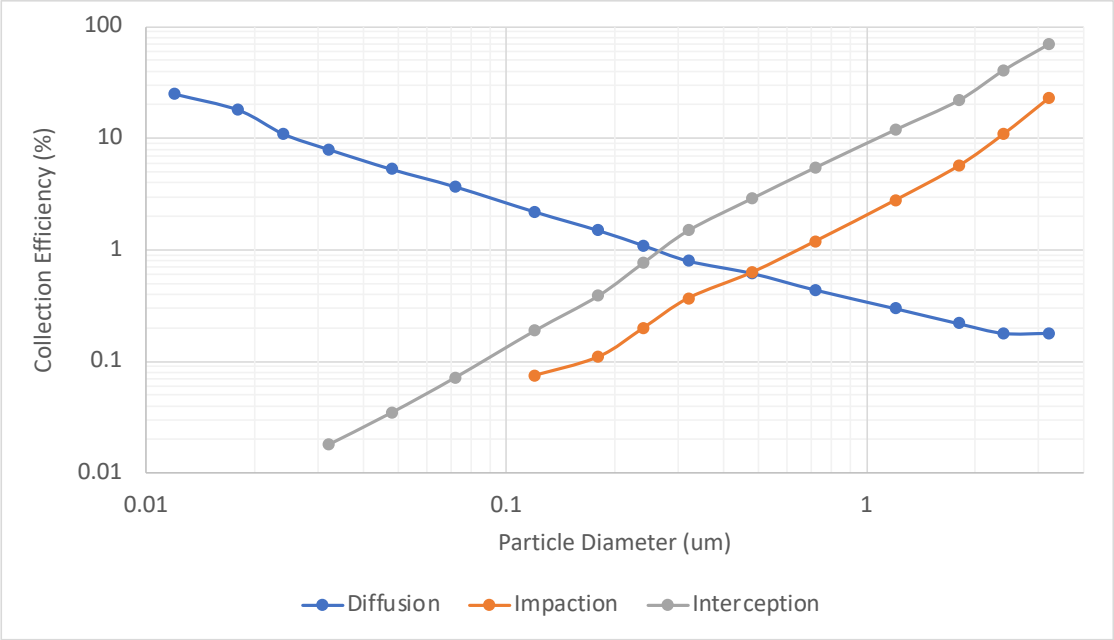


Figure 1- Graph showing the collection efficiency of three of the four filtration mechanisms, as a function of particle diameter.

When one adds the capture mechanisms together, one obtains the following collection efficiency curve, shown in Figure 2. Notice that the collection efficiency is excellent for large particles, and is also fairly good for very small particles. However, at 0.2 to 0.3 μm, the collection efficiency is very poor, around 2%. The reason that 0.2 to 0.3 μm particles are hard to capture is because none of the individual capture mechanisms work well in this regime. As the size of the particles decrease, the impaction mechanism decreases because the particles tend to follow the flow of the air rather than being controlled by their mass. As the size of the particles decrease, the interception mechanism decreases because the van der Waals forces on the particle decrease, lessening the attraction to the fiber. However, the diffusion mechanism is different. As the particles decrease in size, they are more likely to be deflected by the air molecules, which increases their chances of running into the fibers. When the three mechanisms are added together for particles in the range of 0.2 to 0.3 um, the individual collection efficiencies of the mechanisms are quite small. Adding together 3 small numbers for collection efficiencies produces a small overall collection efficiency.

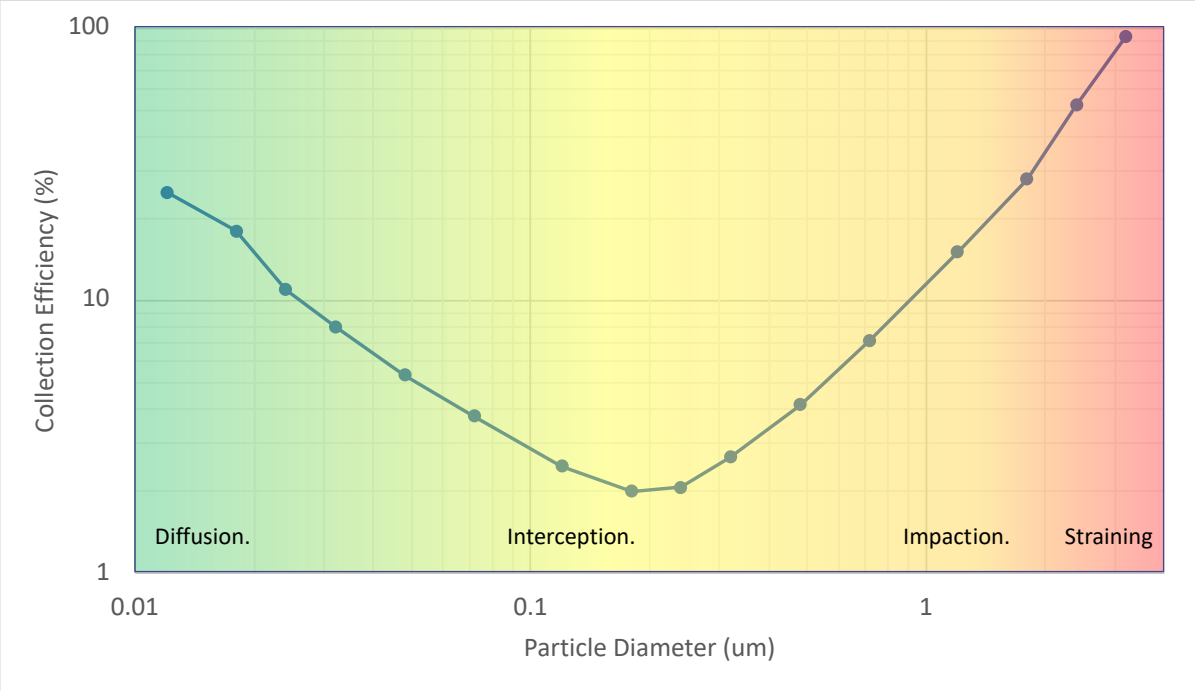
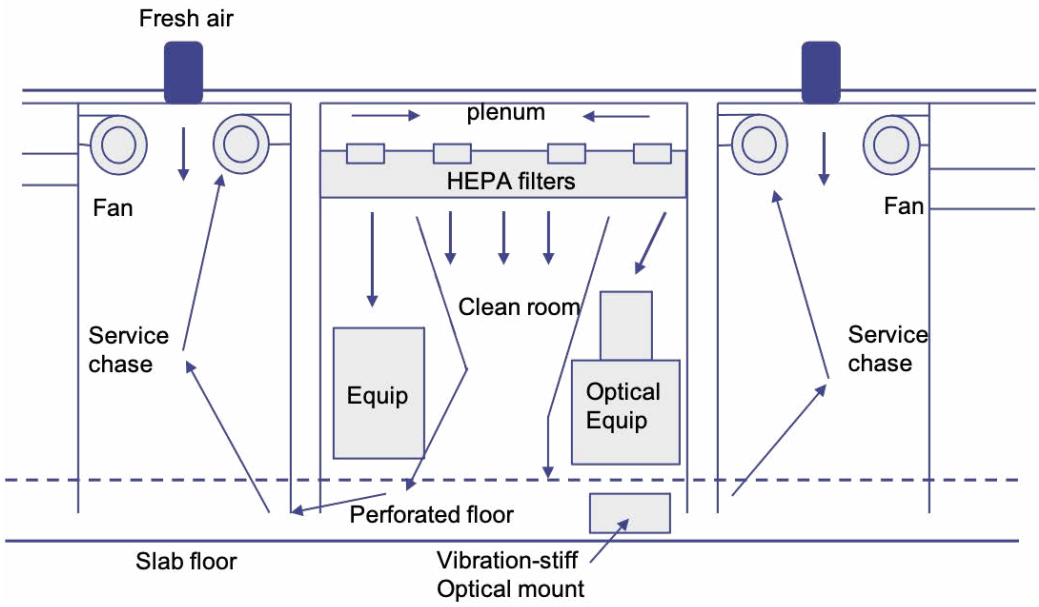


Figure 2- Graph showing the combined collection efficiency for all four filtration mechanisms, as a function of particle diameter.

Next, let's discuss the use of filters in the cleanroom environment. HEPA filters are typically used in two locations. The primary location in a cleanroom would be in the ceiling within the Fan Filter Units, like we show in Figure 3 at the top. The HEPA filters would filter incoming air from the plenum and then exhaust it into the cleanroom itself in the form of laminar flow. A second location for HEPA filters would be in a wafer work station, like we show in Figure 3 at the bottom. The airflow comes in from the top, and a blower forces the air through the HEPA filter and down over the work surface.



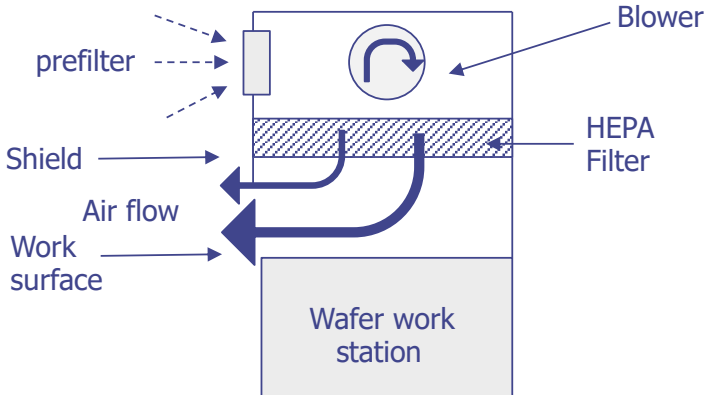


Figure 3- (Top) Laminar flow clean room design showing both the bays and chases. (Bottom) Hood design for wafer work station with vertical laminar flow HEPA filters.

Figure 4 shows the installation of HEPA filters on a larger scale, within a ballroom-style semiconductor cleanroom. Notice that the filters are normally evenly spaced to help provide a more laminar flow of air within the ballroom.

Figure 4- Ballroom-style cleanroom showing placement of HEPA filters in the ceiling.

In next month's Feature Article, we will continue our discussion of filtration for cleanrooms by discussing HEPA filter specifications in more detail.

Technical Tidbit: ATE DC Instrumentation

This month's Technical Tidbit begins a short series on Automated Test Equipment (ATE) Instrumentation. In this month's Tidbit, we will introduce ATE instrumentation and discuss Direct Current (DC) Instrumentation. Test engineers use this type of instrumentation in ATE systems to determine DC voltage and current values in the course of testing integrated circuits.

Let's begin with a brief overview to provide some context. Figure 1 shows a block diagram representation of an ATE system. Most test systems include a Central Processing Unit, which is functions as the brains of the tester; a Digital Signal Processor or Array Processor; a Time Measurement System; Direct Current, or DC Instruments; Alternating Current, or AC Instruments; and a Digital Subsystem for pattern launch and capture.

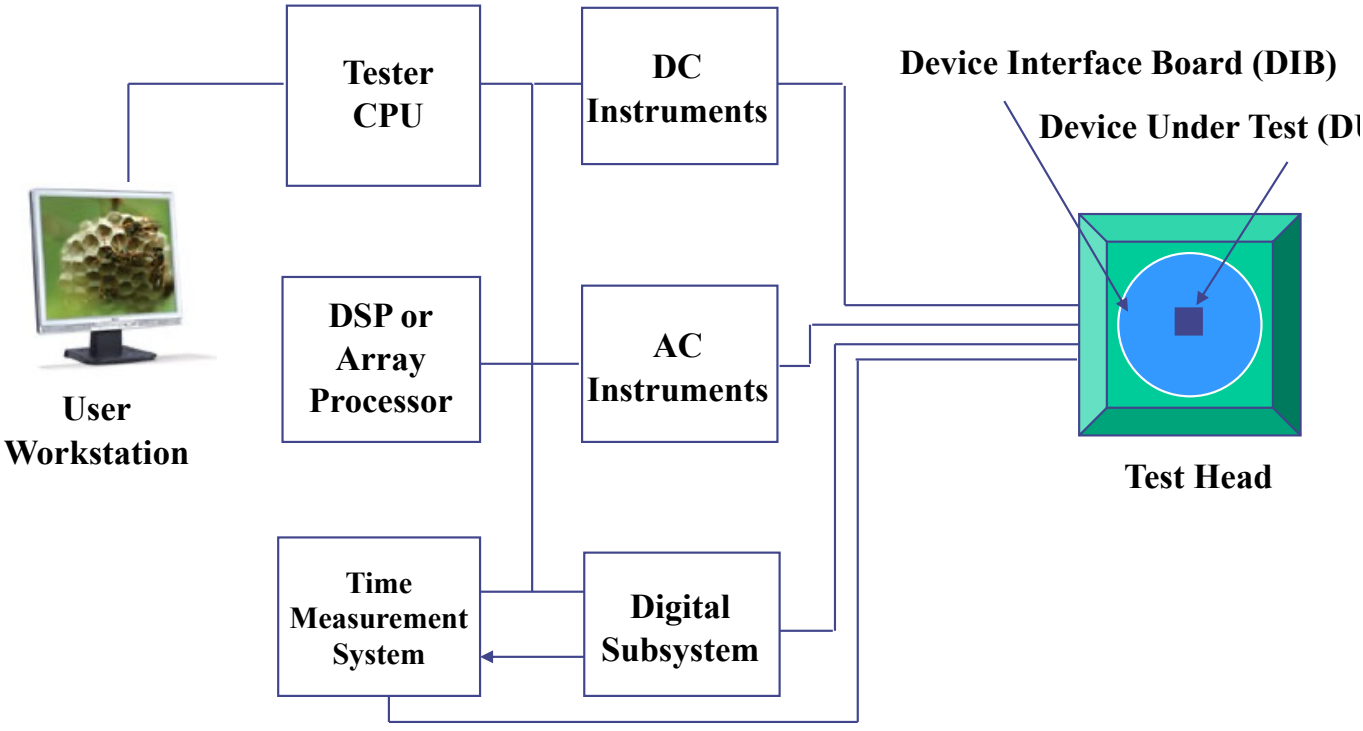


Figure 1- A block diagram depicting the basic architecture of an ATE system.

In the remainder of this Tidbit, we will focus on the "DC Instruments" block. DC instrumentation provides precision voltage-current sources and measurement test capabilities. These integrated instruments source and measure voltage and current for both positive and negative voltages and currents. This is referred to as four quadrant operation. These instruments contain independent voltage-current source and measurement capabilities and differential voltmeters. These instruments also support a large variety of alarms to monitor for programming errors or defective devices.

The schematic in Figure 2 shows an example of a direct current instrument configuration. Starting at the upper left we see the voltage and current Digital-to-Analog Converters, or DACs. These DACs take the digital values from the digital control circuit block and convert them into analog values to present to the Device Under Test, or DUT, which is shown at the right of Figure 2. The output of the DACs goes into summing nodes to detect potential overvoltage errors, undervoltage errors, or excessive current. If an error is detected, error signals are generated by the V/I crossover circuit block and sent back to the digital control as alarm signals. If the signals are in a valid range, the voltage and current signals typically run through an integrator to create a precise, stable value, and then through an overshoot detection circuit, to prevent damage to the DUT. The signals are presented to the DUT through a high impedance connection, shown in the upper right of Figure 2 as the "HiForce" connection. On that same line, voltage signals can be detected as output signals using a high impedance sense connection, shown in the upper right of Figure 2 as the "HiSense" buffer circuit. Current signals can be detected as output signals using the same "HiForce" connection. The detected voltage and current signals then run through a switch, then a low-pass filter, or LPF, and finally through an Analog to Digital converter, and then back to the digital control circuit as a digital representation of analog values. The instrumentation also contains a Device Ground Sensor Buffer circuit, to detect any issues or changes in the ground connection to the DUT.

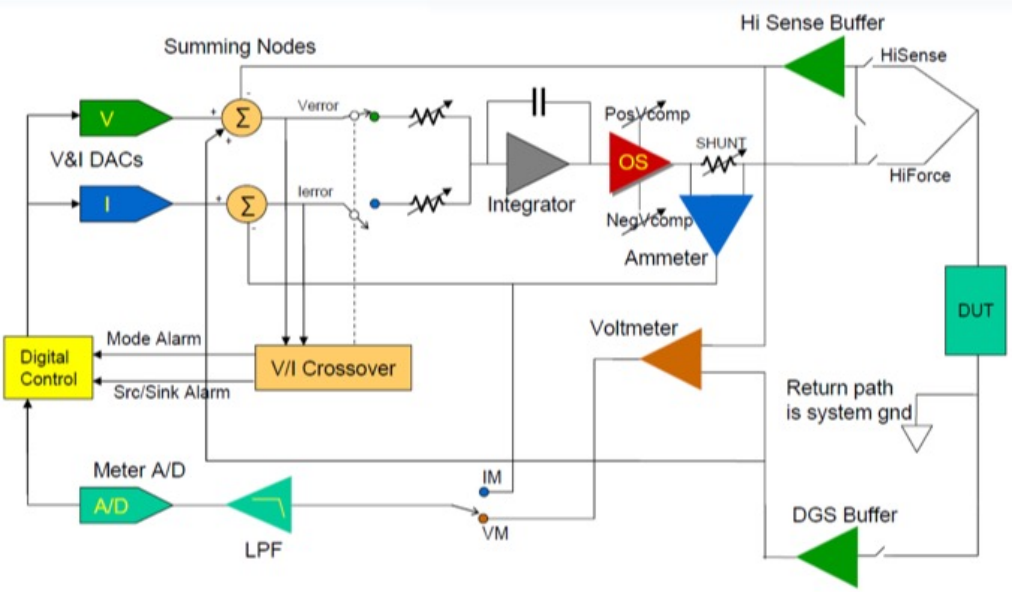


Figure 2- Schematic showing the block diagram of a DC instrumentation module.

In next month's Technical Tidbit, we will discuss the AC portion of the ATE instrumentation.

Ask The Experts

Q: I have a couple of questions regarding field oxidation. My first question involves the location of the oxide. It is my understanding that we pattern the wafer, etch the nitride, and then remove the remaining resist. Next, we deposit more oxide. When the oxide gets deposited, I would expect the oxide to cover everything, not just the open areas between nitride regions. So, shouldn't the oxide cover the top and side surfaces of the nitride as well? My second question involves bird's beak structures. I cannot understand how the bird's beak structure is created. Can you please explain it?

A: Thanks for your questions. Please refer to Figure 1 for more details. During the field oxidation process, the oxide is grown, not deposited. When it is grown, it will only grow in the exposed areas of silicon, not on top of the silicon nitride. This is why this process is known as field oxidation – it is only grown in the "open field" on the silicon.

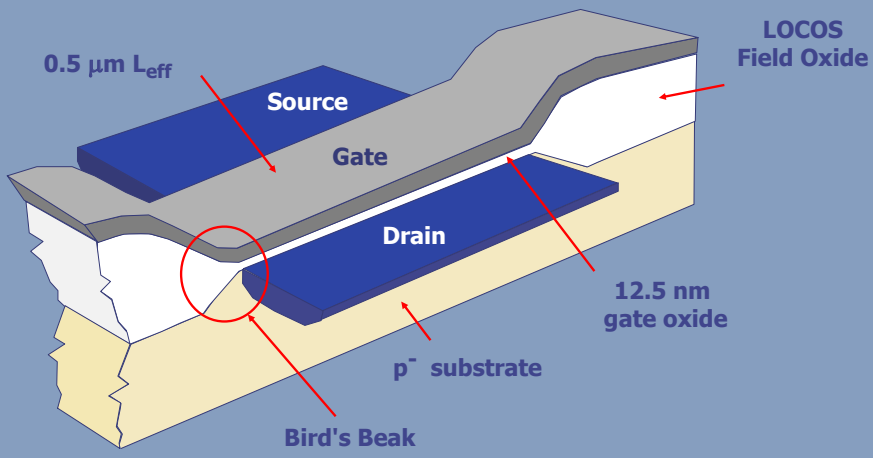


Figure 1- Cutaway view of the field oxide and bird's beak structure.

With regards to the bird's beak structure, the bird's beak shape comes about because the oxygen diffuses into the growing oxide layer from the surface in regions where the silicon is directly exposed, i.e., not covered in silicon nitride. Oxygen diffuses in all directions, both vertically AND horizontally. It is this horizontal diffusion of the oxygen that creates silicon dioxide under the edge of the silicon nitride layer, creating the bird's beak structure.

Course Spotlight:IC PACKAGING DESIGN AND MODELING

OVERVIEW

IC packaging complexity levels are rising year-by-year in lock step with process advances and electrical performance enhancements. Single die packages with leads have given way to multi-chip area array packages, stacked die packages, and stacked packages. Pin-counts have increased from a few handfuls to thousands. Space constraints for consumer products have required shrinking some packages to barely larger than the chip volume, and high-performance applications have required ever increasing levels of power dissipation and higher frequency operation. Pin count increases and wide I/O have driven substrate technologies to include upwards of 20 or 30 interconnect layers. Higher integration levels in automotive applications have motivated higher reliability requirements. At the same time, time-to-market and cost reduction requirements have forced an ever-accelerating product development pace where missing a product launch can spell a company's doom. Trial and error iteration won't work in today's industry.

The only way to meet the interrelated demands of complexity, performance, time-to-market, and reliability is through appropriate package design processes and modeling. This webinar will cover fundamental issues in package design, including the need for appropriate risk analysis, up-front design rules, early look-ahead, and modeling coupled with verification. Compact models that enable transferring phenomenological behavior between die, package, and system level models will be described. Mechanical analysis examples applied to a wide range of reliability issues will be emphasized with a focus on solving issues in advance.

Participants will learn the fundamentals of thermal and electrical analysis for performance characterization. Participants will also learn critical skills required to design a fully functioning IC package that meets competing requirements. Participants will then learn the critical factors that must be implemented to ensure the success of their package designs and products. This skill-building series is divided into four segments:

1. **Packaging Design Overview.** Participants will learn the fundamentals of packaging design. They will learn why modeling has become critical to today's semiconductor packaging, and how important co-design from the chip level through the system level is to product performance.

2. **Mechanical Simulations.** Participants will learn the fundamentals of displacement, strain, stress, and energy, and how to interpret the stresses that can be calculated. They will also learn how to apply fracture mechanics to a problem.

3. **Thermal Simulations.** Participants will learn heat transfer modeling. They will also learn about steady-state, and transient thermal modeling. Reasons for, and the topology of, industry standards and compact thermal models will be described.

4. **Modeling Semiconductor Packages.** Participants will learn about the software used for modeling a variety of aspects of semiconductor packaging. They will see many examples of current modeling tools used by package design experts.

COURSE OBJECTIVES

1. Application spaces for each package family will be covered, including the primary constraints and care-abouts for the product spaces.

2. A thorough listing of interrelated factors will be detailed to enable participants to understand what factors throughout the entire package design chain must be considered when making modifications to one or more package constituents.

3. Mechanical modeling will be highlighted as a tool to be used to develop a parametric understanding of stress impacts. For example, if an underfill modulus is changed, what happens to the stresses on the circuits under the bumps, on the die interface, in the underfill, etc.

4. Participants will know the types of stress analyses that should be performed for each package question, as well as the inputs and verification that is required to ensure the model is producing real answers, not just numbers.

5. Thermal and electrical modeling techniques needed to verify a package's performance well before tooling is committed will be described.

6. Participants will learn from real examples how best to utilize package design tools and will learn the software's strengths and weaknesses.

7. Participants will see examples of package design rules that, when incorporated in design manuals, enable robust reliable package design. Participants will also
l earn how to develop package design rules for their own products.

8. Knowledge gained from the class will improve time-to-market for participants by helping them avoid costly qualification failures.

COURSE OUTLINE

1. Assembly & Packaging Processes
    a. Material Selection
    b. Typical Assembly Process Flows
    c. Package Types & Evolution
    d. Simulation Tools & Applications
    e. Risk Evaluation & Risk Mitigation

2. Design for Manufacturability (DfM)
    a. Solid Mechanics
    b. Assembly-Induced Stress
    c. Package Warpage & Coplanarity
    d. Die Bonding, Wire Bonding, & Microbump Bonding
    e. Mold Flow Modeling and Correlations

3. Design for Reliability (DfR)
    a. Chip-to-Package Interaction (CPI)
    b. Interfacial Delamination & Adhesion
    c. Solder Joint Reliability (SJR)

4. Design for Performance
    a. Heat Transfer
    b. Package Thermal Resistance
    c. Steady State & Transient Thermal Behavior
    d. Power Distribution and Noise
    e. Compact Models
    f. Drop Testing & Simulation

5. Advanced Packaging Examples
    a. Multichip Packages
    b. Stacked Packages
    c. Wafer Level Packaging
    d. 3D Packaging
    e. Through Silicon Via (TSV) Interconnects

Upcoming Courses:

Public Course Schedule:

Product Qualification Overview - September 11, 2023 (Mon.) | Phoenix, Arizona - $695

Advanced CMOS/FinFET Fabrication - September 25-26, 2023 (Mon.-Tues.) | Phoenix, Arizona - $995

IC Packaging Technology - January 23-24, 2024 (Tues.-Wed.) | Phoenix, Arizona - $1,295

Advanced CMOS/FinFET Fabrication - January 29-30, 2024 (Mon.-Tues.) | Phoenix, Arizona - $995

Wafer Fab Processing - February 26-29, 2024 (Mon.-Thurs.) | Munich, Germany - $2,095

Failure and Yield Analysis - March 4-7, 2024 (Mon.-Thurs.) | Munich, Germany - $2,095

Semiconductor Reliability and Product Qualification - March 11-14, 2024 (Mon.-Thurs.) | Munich, Germany - $2,095

Defect-Based Testing - March 20-21, 2024 (Wed.-Thurs.) | Munich, Germany - $1,195

Webinar Schedule:

RF and Mixed-Signal Testing - August 28-31, 2023 (Mon.-Thurs.) | Online Webinar at 8:00 AM to 10:00 AM PDT - $995

IC Packaging Design and Modeling - September 18 - 21, 2023 (Mon. – Thurs.) | - $600

Have an idea for a course? If you have a suggestion or a comment regarding our courses, online training, discussion forums, or reference materials, or if you wish to suggest a new course or location, please email us at info@semitracks.com

To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered, please contact Jeremy Henderson at jeremy.henderson@semitracks.com

We are always looking for ways to enhance our courses and educational materials and look forward to hearing from you!