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Substrate Materials

By Christopher Henderson

In this section we will cover substrate materials. These are the materials used to create interposers and other substrates used in microelectronics packaging.

Lets begin with some terms and definitions. Engineers and scientists in the semiconductor industry use the term interposer to describe a substrate that goes in between the die and the printed circuit board. It is used to route and re-distribute signals to a different and/or larger footprint. We use the term BU or build-up to refer to the layers—both conducting and insulating—that create the interconnect between the die and the printed circuit board. These layers are typically built upon a core substrate material. We use the term thermoset to refer to an epoxy system that cures by the application of heat. Also importantly, once the thermoset is cured the process cannot be reversed; it is "set."

Many printed circuit boards and substrates in use today are composed of a material called FR4. The FR in FR4 stands for fire retardant. The 4 in FR4 is a particular composition that is a glass fiber epoxy laminate. 1.60mm FR4 uses 8 layers of (7628) glass fiber material. 7628 is a common glass fabric that has a particular weight, thickness, warp and weft. The red UL/manufacturers logo is in the middle (layer 4). FR3 is mainly a European product. It is

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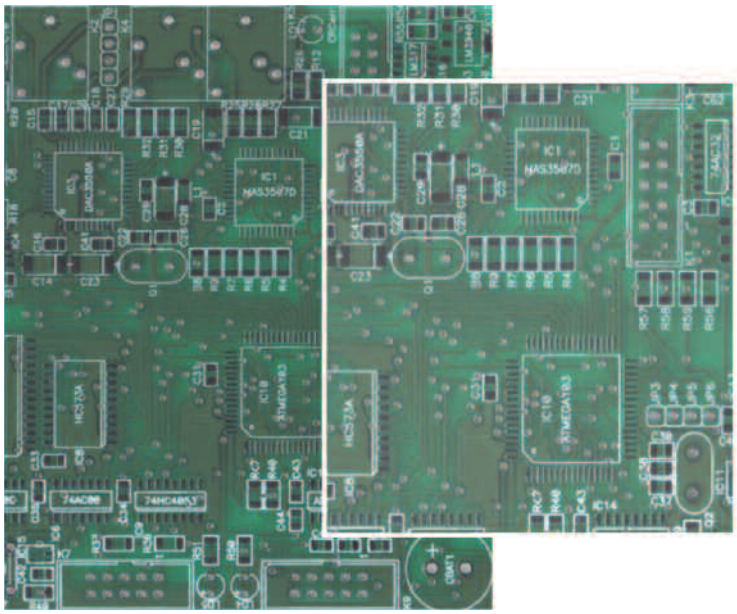
basically FR2, but instead of phenolic resin it uses an epoxy resin as binder. The basic layer is paper. FR2 is a paper material with phenolic binder. It is UL94-V0. FR1 is basically the same as FR2, but it has a higher glass transition temperature of 130ºC instead of 105ºC for FR2. Some laminate manufacturers that produce FR1 will not produce FR2, since the costs and usages are similar and there is no advantage to making both.

CEM stands for composite epoxy material. CEM-1 is a paper based laminate with one layer of (7628) woven glass fabric. It is not suitable for creating plated through holes. CEM-3 is very similar to FR4. Instead of woven glass fabric a "flies" type is used. CEM-3 has a milky white color and is very smooth. It is a complete replacement for FR4 and has a very large market share in Japan. A "prepreg" is an epoxy coated glass fabric. It has two usages: as a dielectric layer in multilayer PCBs, and as the raw material for FR4. 8 layers of "7628" prepregs are used in one sheet of 1.60mm FR4. The central layer (no. 4) usually carries the red company/UL logo. Plated through holes—or PTH—provide electrical connection from one side of the board to another, or from one layer within the board to another. Plated through holes can be made on FR4 and CEM-3 boards, but not on the other types. Finally, the term IPN —or Interpenetrating Polymer Network—is a term used for a polymer comprising of two or more networks, which are at least partially interlaced on a polymer scale.

Here are the physical properties of some of the more common printed circuit board materials. We compare dielectric constants, surface resistance, volume resistance, glass transition temperature arc resistance, flexural strength lengthwise, flexural strength crosswise, coefficients of thermal expansion and suitability for plated through holes. Notice that FR4 has a relatively high glass transition temperature, a superior arc resistance, and high flexural strength, both lengthwise and crosswise. Another advantage to FR4 is that it is a suitable material for plated through holes.

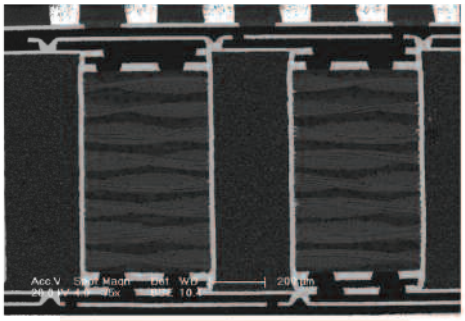
Feature	Unit	FR2	CEM1	CEM3	FR4	Teflon	Polyimide
Material Composition	-	Paper with Phenolic binder	Paper based with 1 Layer Glass	Glass fiber epoxy laminate (flies)	Glass fiber epoxy laminate (woven)	PTFE	Polyimide resin with aramide-reinforcing
Dielectric Constant @ 1 MHz	-	4.1	4.2	5.0	4.8	2.2-10.2	3.8
Surface Resistance	Ohm	10E11	10E11	10E11	10E11	10E11	10E11
Volume Resistance	Ohm cm	10E10	10E13	-	10E12	-	10E14
Glass Transition Temp (Tg)	°C	30	60/90	125	135	160-280	260
Arc Resistance	KV	15	40	-	40	-	90
Flexural strength, (X)	(N/mm)	160	400	480	600		
Flexural strength, (Y)	(N/mm)	140	220	330	450		
Thermal Stress	ppm/°K	270-330	300	190	170	100-200	-
For PTH	-	no	no	yes	yes		

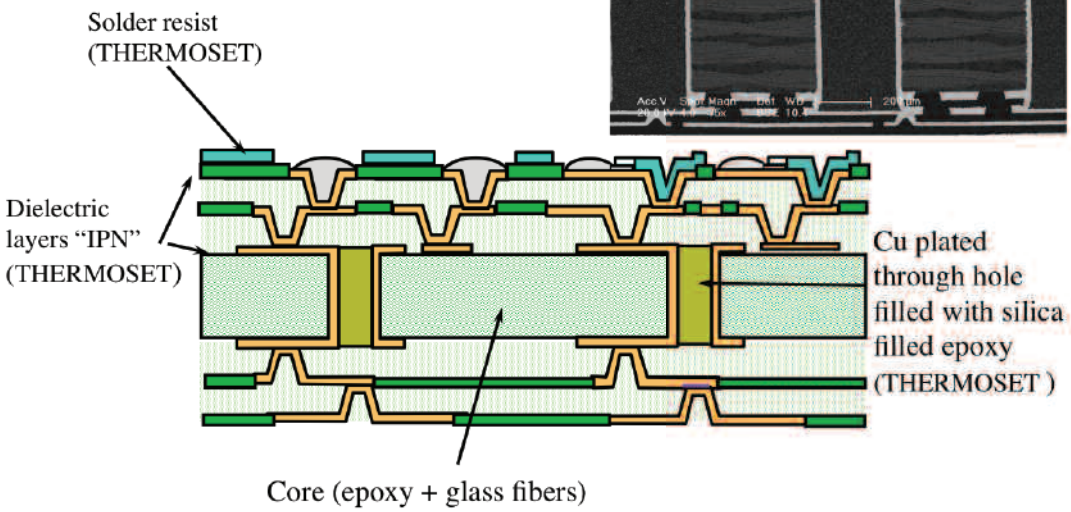
Here is an example of a board manufactured from FR4. Untreated FR4 is usually transparent. The green color comes from the solder mask in the PCB finished product. Here we have increased the magnification on a portion of the board. Notice that the solder traces are visible, along with the plated through holes. The white lettering and outlines are added to help with placement of components during the board assembly process.



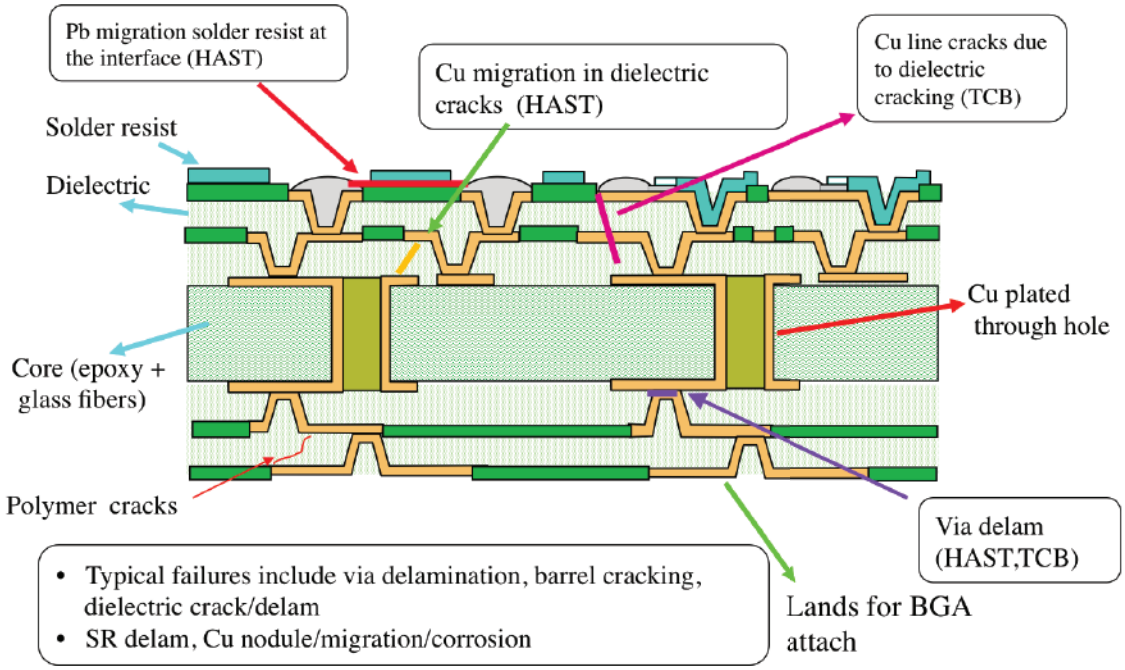
This is a cross section example of a multi-layer board with core resin and build up layers. The interconnection occurs through plated through holes and vias. The key defects due to processing and intrinsic CTE mismatches between various components or materials issues are: cracks through dielectric layers, cracks through plated through holes, delamination of vias, delamination at metal/dielectric interfaces, and defects in the dielectrics.

Schematic representation of an organic package cross-section highlighting the materials used in the multilayer package





This figure shows some of the typical substrate failures that can occur with a substrate that contains a core structure, plated-through-holes and build-up materials. These failures include mechanisms seen in highly accelerated stress testing (HAST) such as: lead migration over or under the solder resist at the interface, copper migration in cracks in the dielectric, and via delamination. Other types of failures seen in temperature cycling include: copper line cracks due to dielectric cracking, barrel cracking, via delamination, and polymer cracks.



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Technical Tidbit

Basic Steps for Characterizing a Decapsulation Process

There are several steps to creating a successful process for decapsulating an IC. Barry and Nancy Weavers of Left Coast Instruments put together a checklist of 8 steps to help you accomplish this task. We summarize the steps below.

First, determine the acid type:

90% Fuming Nitric Acid (HNO_3) is the least expensive, and is the lowest grade that will decapsulate plastic packages.

98% Fuming Nitric Acid (HNO_3) produces a faster etch rate, with much less metal damage. It can also be used over a wider temperature range.

Red Fuming Nitric Acid (HNO_3) can be used with some systems, like the Elite Etch.

96 to 98% Sulfuric Acid (H_2SO_4) is the least expensive, and is the lowest grade that will decapsulate high-temperature packages.

20% Fuming Sulfuric Acid (H_2SO_4) produces a faster etch rate, with much less metal damage.

Next, determine the etch temperature:

Failure analysts typically use HNO_3 in the 75 to 80°C range, mixed acids in the 80 to 90°C range, and H_2SO_4 in the 220 to 250°C range. In packages where unpassivated metals are used, a different technique is required. A mix of 3:1 is commonly used. The temperature range should be between 30 and 50°C in order to protect the metallization. The etch rate will be much slower, but the metal will be better preserved.

Next, determine the heat up time:

Programming the heat-up time depends on the mass of the device. Start with the maximum heat-up time. Drop the time in 5-second increments until the etched hole is reduced in size. Add 5 seconds to the reduced heat-up time for the correct heat-up time.

Next, determine the etch volume:

The etch volume is the amount of acid used (ml/min) that is programmed in the etch time. As a general rule, when using nitric acid one should start with a volume of 3 ml/min. The color of the waste material will determine the correct volume. If the waste acid is light brown to clear the volume is too high. If it is dark brown and not moving freely the volume is too low. If the waste acid is brown and moving freely the volume is correct.

Next, determine the correct fixturing:

Once the above have been determined, the correct fixturing can be chosen. The acid type used for decapsulation determines the definition gasket.

Next, determine the etch time:

The etch time is the amount of time (in seconds) that the device is actually being etched. The easiest way to determine the etch time is to run a sample of the package for a short period of time. For SO and TSOP packages start with 10 seconds; for all other packages 60 seconds works well as a starting time - these are your base etch times.

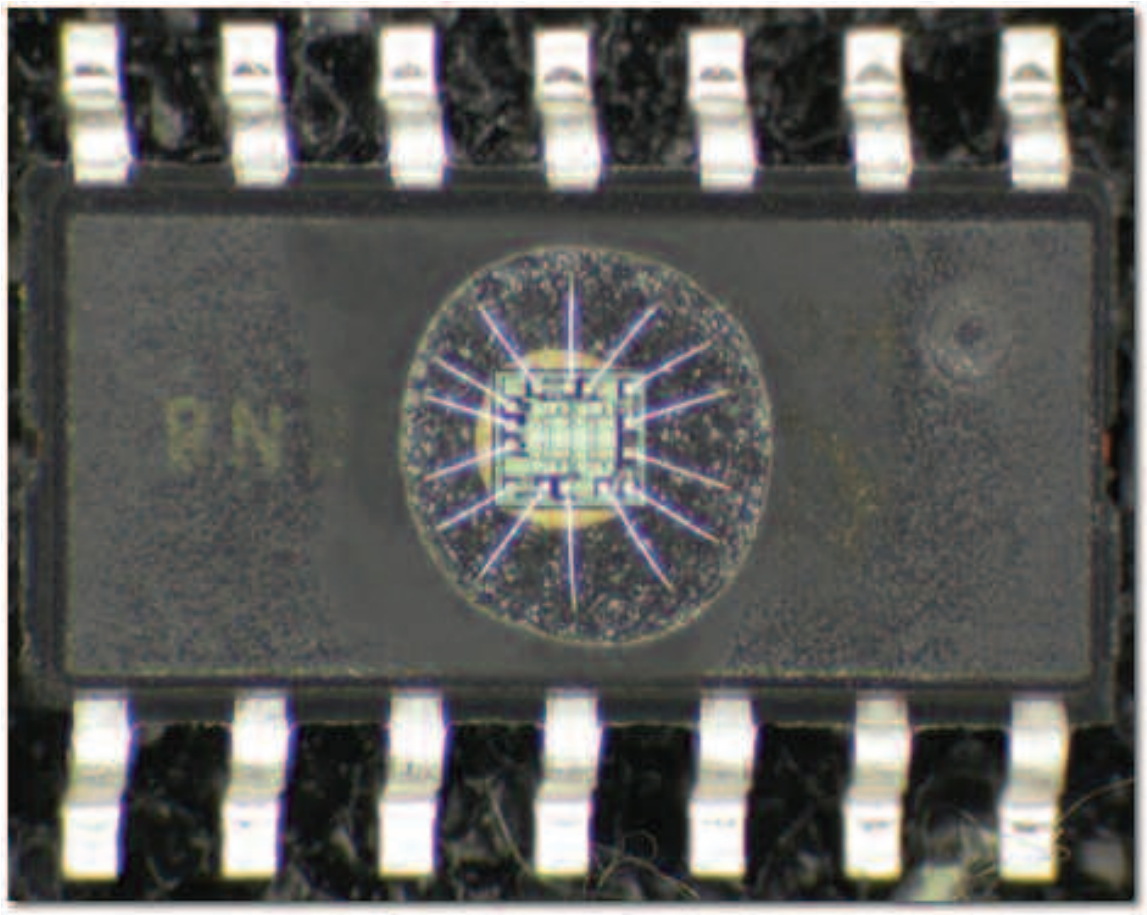
Next, choose Pulse or Reciprocal Etch mode:

The choice of pulse or reciprocal etch mode determines the relative angle of the sidewall. A reciprocating etch will produce a relatively straight sidewall, while pulse etch will produce a more rounded sidewall.

Finally, determine the rinse time:

The rinse time serves two functions. The first is to clean the part with cold acid and flush the part and waste line before nitrogen flush. The second, and very important function, is to make very small changes to the etch cavity. Start with “No Rinse” and then adjust as required.

If you follow these steps, you should be able to achieve good, repeatable results, like we show in the image below.



Ask the Experts

Q: I analyzed a customer return failure and the failure mechanism appears to be voiding due to intermetallic growth. What do you think happened to this part?

A: Based on the evidence, the part you're analyzing saw high temperatures for an extended period of time. We can't tell from the images when that might have happened though. It could have occurred during bonding (not likely, but possible), during some other portion of the assembly operation (also not likely, as you would have had many other failures), or during field use (more likely). You'll need to work with your customer to track down the root cause. Are other bond pads on this chip showing the same voiding?

You may want to stress some aspects more than others or conduct a simple one-day overview course. Many of our clients seek ongoing just-in-time training that builds in-depth, advanced levels of reliability expertise. We'll work with you to determine the best course of action and create a statement of work that emulates the very best practices of semiconductor reliability analysis.

Our instructors are active in the field and they practice the disciplines daily. Please give us a call (505) 858-0454 or drop us an e-mail (info@semitracks.com).

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Spotlight: Semiconductor Reliability

OVERVIEW

Semiconductor reliability is at a crossroads. In the past, reliability meant discovering, characterizing and modeling failure mechanisms and determining their impact on the reliability of the circuit. Today, reliability can involve tradeoffs between performance and reliability, assessing the impact of new materials, dealing with limited margins, etc. Analysis and experimentation is now performed at the wafer level instead of the packaging level. This requires knowledge of subjects like: design of experiments, testing, technology, processing, materials science, chemistry, and customer expectations. While reliability levels are at an all-time high level in the industry, rapid changes may quickly cause reliability to deteriorate. Your company needs competent engineers and scientists to help solve these problems. ***Semiconductor Reliability*** is a thtee- to five-day course that offers detailed instruction on a variety of subjects pertaining to semiconductor reliability. This course is designed for every manager, engineer, and technician concerned with reliability in the semiconductor field, using semiconductor components, or supplying tools to the industry.

Participants learn to develop the skills to determine what failure mechanisms might occur, and how to test for them, develop models for them, and eliminate them from the product.

1. **Overview of Reliability and Statistics.** Participants learn the fundamentals of statistics, sample sizes, distributions and their parameters.
2. **Failure Mechanisms.** Participants learn the nature and manifestation of a variety of failure mechanisms that can occur both at the die level and at the package level. These include: time-dependent dielectric breakdown, hot carrier degradation, electromigration, stress-induced voiding, moisture, corrosion, contamination, thermomechanical effects, etc.
3. **Qualification Principles.** Participants learn how test structures can be designed to help test for a particular failure mechanism.
4. **Test Strategies.** Participants learn the basics on how to test test structures, design screening tests, and how to perform burn-in testing effectively.

COURSE OBJECTIVES

1. The seminar will provide participants with an in-depth understanding of the failure mechanisms, test structures, equipment, and testing methods used to achieve today's high reliability components.
2. Participants will be able to gather data, determine how best to plot the data and make inferences from that data.
3. The seminar will identify the major failure mechanisms, explain how they are observed, how they are modeled, and how they are eliminated.
4. The seminar offers a variety of video demonstrations of analysis techniques, so the participants can get an understanding of the types of results they might expect to see with their equipment.
5. Participants will be able to identify basic test structures and how they are used to help quantify reliability on semiconductor devices.
6. Participants will be able to knowledgeably implement screens that are appropriate to assure the reliability of a component.
7. Participants will be able to identify appropriate tools to purchase when starting or expanding a laboratory

INSTRUCTIONAL STRATEGY

By using a combination of instruction by lecture, video, problem solving and question/answer sessions, participants will learn practical approaches to the failure analysis process. From the very first moments of the seminar until the last sentence of the training, the driving instructional factor is **application**. We use instructors who are internationally recognized experts in their fields that have years of experience (both current and relevant) in this field. The handbook offers hundreds of pages of additional reference material the participants can use back at their daily activities.

THE SEMITRACKS ANALYSIS INSTRUCTIONAL VIDEOS™

One unique feature of this workshop is the video segments used to help train the students. Reliability Analysis is a visual discipline. The ability to identify nuances and subtleties in graphical data is critical to locating and understanding the defect. Some tools output video images that must be interpreted by engineers and scientists. No other course of this type uses this medium to help train the participants. These videos allow the analysts to directly compare material they learn in this course with real analysis work they do in their daily activities.

COURSE OUTLINE

Day One (Lecture Time 8 Hours)

1. Introduction to Reliability
    a. Basic Concepts
    b. Definitions
    c. Historical Information
2. Statistics and Distributions
    a. Basic Statistics
    b. Normal Distribution
    c. Lognormal Distribution
    d. Weibull Distribution
    e. Exponential Distribution
    f. Which Distribution Should I Use?
    g. Data Handling

Day Two (Lecture Time 8 Hours)

3. Die-Level Failure Mechanisms
    a. Time Dependent Dielectric Breakdown
    b. Hot Carrier Damage
    c. Negative Bias Temperature Instability
    d. Electromigration
    e. Stress Induced Voiding

Day Three (Lecture Time 8 Hours)

4. Package Level Mechanisms
    a. Ionic Contamination
    b. Moisture/Corrosion
    c. Thermo-Mechanical Stress
    d. Thermal Stress/Cycling
5. Use Condition Mechanisms
    a. Electrical Overstress/ESD
    b. Radiation

Day Four (Lecture Time 8 Hours)

6. Test Structures and Test Equipment
    a. Test Structures
        i. Parametric Test Structures
        ii. Reliability Test Structures
        iii. Self-Stressing Test Structures
    b. Test Equipment
        i. Packaged Part Testing
        ii. Wafer Level Testing
7. Developing Screens, Stress Tests, and Life Tests
    a. Burn-In
    b. Life Testing
    c. HAST
8. Package Attach (Solder) Reliability
9. Board Level Reliability Mechanisms
10. Calculating Chip and System Level Reliability
11. Future Reliability Challenges

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http://www.asminternational.org/web/istfa-2015

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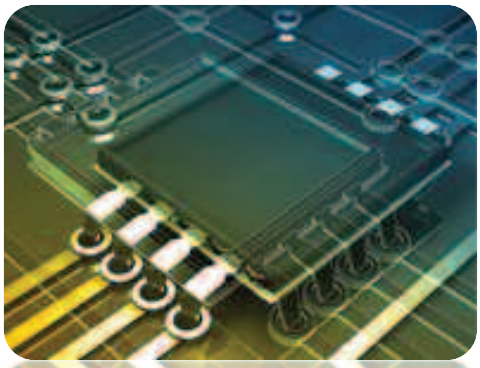
Semitracks will be attending and will be available for meetings. Please contact us at info@semitracks.com to schedule a meeting.



Upcoming Courses

(Click on each item for details)

Semiconductor Reliability
September 2 – 4, 2015 (Wed – Fri)
Munich, Germany

EOS, ESD and How to Differentiate
September 7 – 8, 2015 (Mon – Tue)
Munich, Germany

Product Qualification
September 9 – 10, 2015 (Wed – Thur)
Munich, Germany

MEMS Packaging and Reliability
September 14 – 15, 2015 (Mon – Tues)
Boston, Massachusetts

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To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered in the next newsletter, please contact Jeremy Henderson by Email (jeremy.henderson@semitracks.com).
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We look forward to hearing from you!