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Semitracks Monthly Newsletter

Analog Building Blocks

By Christopher Henderson

This month, we will begin a new series of Feature Articles that will cover some of the basic analog circuit building blocks used. Analog circuit design is in many respects quite a bit different than digital circuit design, as it requires a deep understanding of transistor behavior and innovative thinking as to how to use the transistor and other circuit elements to one's advantage. This month's Article will focus on current sources—a basic building block of amplifier circuits.

The bipolar transistor can be used in three different modes as an amplifier. They are: the common emitter, shown on the left in Figure 1; the common collector, shown in the center of Figure 1; and the common base, shown on the right of Figure 1. All three types are used for different applications in analog circuits.

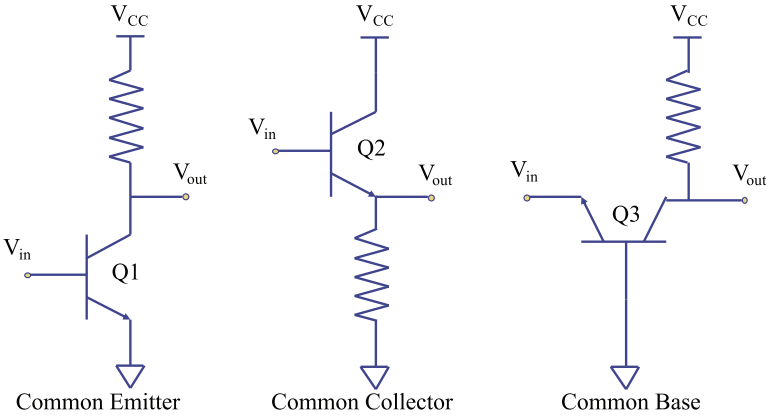

Figure 1. Diagram of different modes of bipolar transistor used as an amplifier.

In this Issue:

The common emitter has its emitter tied to ground. A small voltage in on the base of Q1 yields a larger voltage out because of the resistor between the supply voltage V_{CC} and the collector. The current into the collector of the npn transistor will change as the current into the base changes. This changing current through the resistor R1 will cause the output voltage—V_{OUT}—to change by an amount related to the gain of Q1.

In the common collector configuration, the collector is tied to the positive power supply. A voltage in on the base of Q2 produces a larger voltage out at the emitter due to R2.

In the common base configuration, the base is tied directly to ground. A voltage in on the emitter of Q3 will produce a voltage out that closely follows the input voltage. The common base configuration will always have a gain less than 1, so there are not many uses for this configuration. It is used in some high-frequency applications because there is good isolation between the input and the output, which leads to better stability in the amplifier circuit.

The diagram in Figure 2 shows a two-transistor current source. This type of current source is used widely because it is easy to construct and is quite flexible. It also produces a fairly stable current source. The reference current I_{REF} is established by placing a resistor, R1, between the collector of Q1 and the positive power supply voltage. This configuration will result in a voltage of approximately 0.7 volts on both the bases of Q1 and Q2. If the transistors are designed to be equal, the current into the collector of Q2, denoted as I_C, will be the same as I_{REF}.

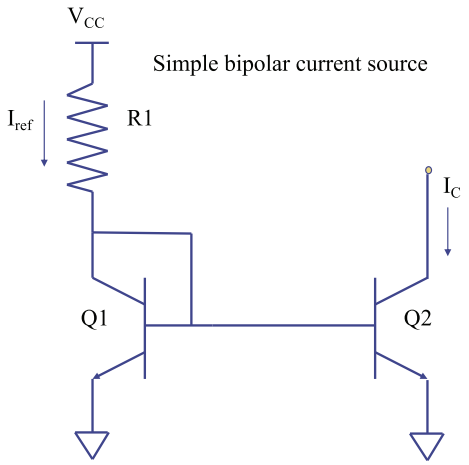

Figure 2. Diagram of two-transistor current source.

As we show in Figure 3, one can also create the same type of current source using MOS transistors (this type of circuit is known as a current mirror circuit). The circuit works in a similar manner to the bipolar current source. The resistor, R1, causes a particular voltage on the gate of both M1 and M2. This voltage in turn biases the two transistors such that they conduct a certain amount of current. This affects the current through the resistance and the voltage on M1 and M2. The circuit will quickly reach an equilibrium that is a function of the value of R1 and the transconductance of M1. This particular circuit can be more flexible than its bipolar equivalent because the two transistors can be sized to yield different

values of I_0. This current is determined by the width to length ratios of the two transistors. If we hold L constant with the two transistors, I_0 will be the ratio of the transistor widths, like we show in the equation here:

$$I_O = I_{D2} = \frac{W_2}{W_1} I_{D1}$$

Although this circuit is simple, it suffers from poor gain characteristics, so an alternative with better gain characteristics is the cascode connection.

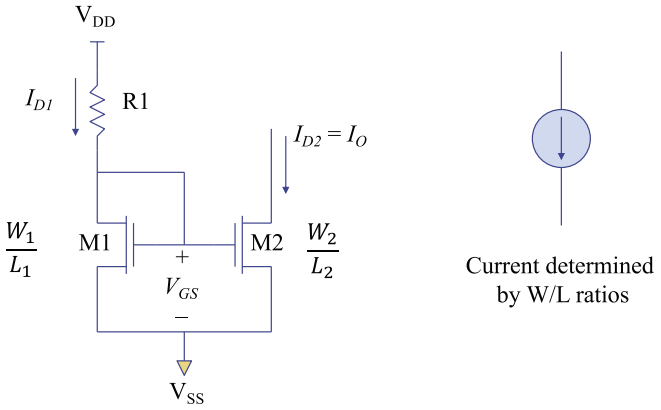

Figure 3. Diagram illustrating current mirror circuitry.

The cascode connection is essentially placing two transistors in the gain path instead of a single transistor. The term cascode is believed to be a contraction of the words “cascaded triode” used in vacuum tube technology. The cascode connection is used to increase the output resistance of an amplifier. The cascode connection can also be used to minimize the effects of power supply fluctuations on the output gain characteristics. In the MOS implementation (shown on the left of Figure 4), the cascode connection also increases the gain due to the larger output resistance and can reduce the input time constant since the gate-to-drain capacitance in M1 fluctuates less in a cascode configuration. In the bipolar implementation (shown on the right of Figure 4), the cascode connection is sometimes called the common emitter common base connection.

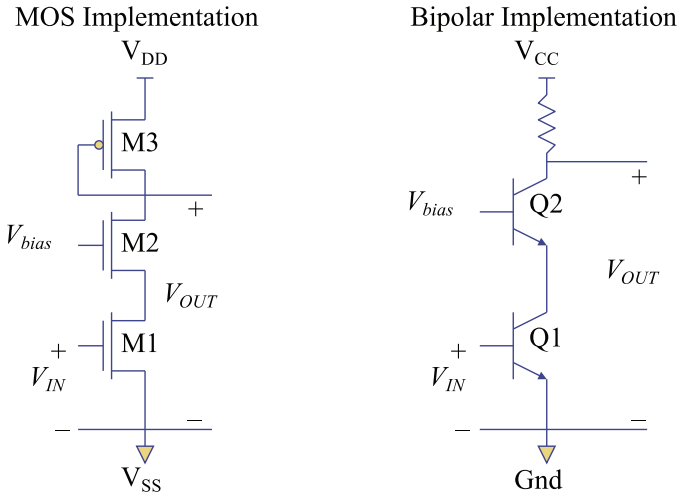

Figure 4. Cascode connection: diagram of MOS (left) and bipolar implementation (right).

Figure 5 helps illustrate the advantages of the cascode circuit. Transistors M3 and M4 are added to create the cascode mirror circuit, as shown on the left of Figure 5. The current-voltage graph (shown on the right of Figure 5) shows the differences between the standard current mirror circuit and the cascode mirror circuit. Notice how the cascode mirror current increases very little after V_0 reaches 2ΔV. This is indicative of a high output resistance. The main drawback to the cascode arrangement is that the output voltage must be above 2ΔV in order to achieve the high output resistance. A standard current mirror goes into its high output resistance mode at 1ΔV.

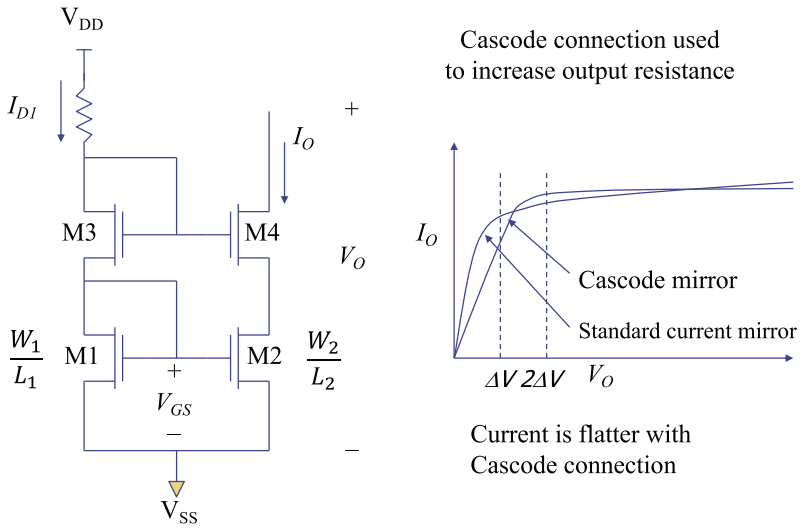

Figure 5. Diagram (left) and graph (right) illustrating cascode circuit advantages.

In next month's Feature Article, we will discuss reference circuits.

Technical Tidbit

Input/Output Cells

This month's Technical Tidbit covers input and output cells for integrated circuits.

For signals to come in and out of a silicon chip, designers use interface circuitry to ensure the signals come and go properly. This requires specialized circuitry and layouts for input connections, output connections, and connections that support both input and output connections, known as bi-directional connections. Figure 1 shows examples of the three types of circuitry found in cells. The red squares at the bottom of each cell in Figure 1 represent the bond pads, where the wires are bonded to the silicon die. So, for what use is the rest of the circuitry in the cell? We need to make sure that the circuitry on the silicon die can properly drive signals into the package and printed circuit board. In particular, the larger capacitance of the circuitry elsewhere on the printed circuit board creates difficulties. This means that there needs to be transistors that are larger to provide the current to switch the circuitry with this extra capacitance. However, large transistors take up a lot of room on the silicon. Therefore, designers use transistors that are closer to the minimum size for signals that route internal to the silicon die, and transistors that are larger to route to other chips and circuitry that are outside of the die. These larger transistors make up a portion of the output and bi-directional cells. Furthermore, the input, output, and bi-directional connections need to provide protection against voltage and current transients from outside of the chip. This means that these three cells will contain protection circuitry. This protection circuitry is typically input protection diodes to ground and the power supply; larger junctions on the output transistors to the ground and the power supply terminals; and resistors at the input of sensitive gates in an input cell. Often the three cells will contain a buffer circuit to condition the signal to go into the circuitry on the die, or to condition the internal signal to come out of the die. These designs can be rather complex, so there are design engineers who actually specialize in designing these types of cells. They are sometimes known as I/O designers, where I/O stands for Input Output.

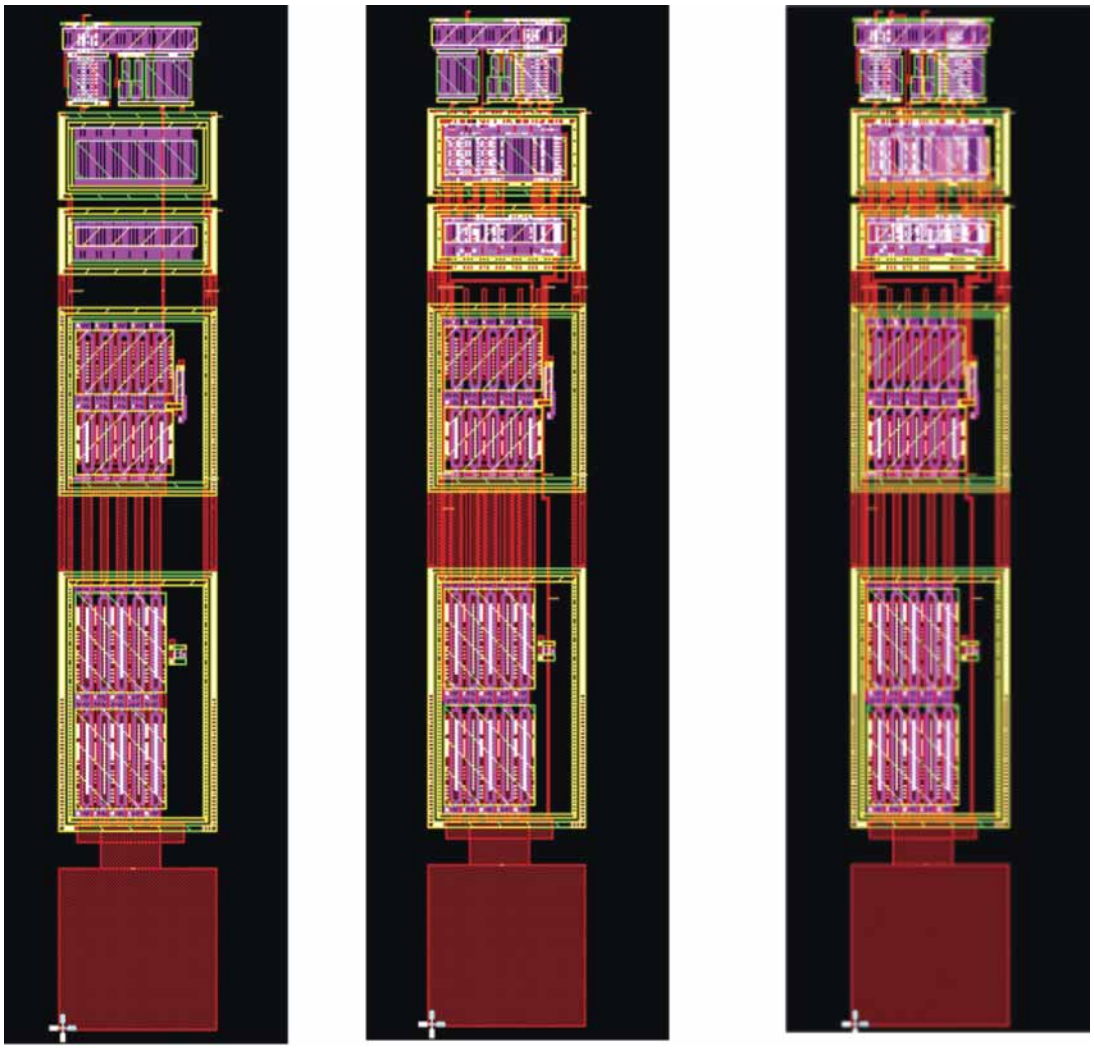

Figure 1. Input Cell (left); Output Cell (center); Bi-directional Cell (right).

Ask the Experts

Q: Has anyone published chemistries and times for decapsulation of different mold compounds?

A: While we are not aware of anyone who has publicly published a table with this information, companies such as Left Coast Instruments and Nisene Technology may have information on this topic. You need to be a customer to access their articles, but if you are, you can go to their website and look.

https://www.lcinst.com
https://www.nisene.com

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Spotlight: Wafer Fab Processing

OVERVIEW

Semiconductor and integrated circuit developments continue to proceed at an incredible pace. The industry as a whole has gotten to this point of incredible complexity through the process of countless breakthroughs and developments in wafer fab processing. Today's wafer fab contains some of the most complex and intricate procedures ever developed by mankind. ***Wafer Fab Processing*** is a 4-day course that offers an in-depth look into the semiconductor manufacturing process, and the individual processing technologies required to make them. We place special emphasis on the basics surrounding each technique, and we delve into the current issues related to manufacturing the next generation devices. This course is a must for every manager, engineer and technician working in the semiconductor industry, using semiconductor components or supplying tools to the industry.

By focusing on the basics of each processing step and the issues surrounding them, participants will learn why certain techniques are preferred over others. Our instructors work hard to explain how semiconductor processing works without delving heavily into the complex physics and mathematical expressions that normally accompany this discipline.

Participants learn basic but powerful aspects about the semiconductor industry. This skill-building series is divided into three segments:

1. **Basic Processing Steps.** Each processing step addresses a specific need in IC creation. Participants learn the fundamentals of each processing step and why they are used in the industry today.
2. **The Evolution of Each Processing Step.** It is important to understand how wafer fab processing came to the point where it is today. Participants learn how each technique has evolved for use in previous and current generation ICs.
3. **Current Issues in Wafer Fab Processing.** Participants learn how many processing steps are increasingly constrained by physics and materials science. They also learn about the impact of using new materials in the fabrication process and how those materials may create problems for the manufacturers in the future.

COURSE OBJECTIVES

1. The seminar will provide participants with an in-depth understanding of the semiconductor industry and its technical issues.
2. Participants will understand the basic concepts behind the fundamental wafer fab processing steps.
3. The seminar will identify the key issues related to each of the processing techniques and their impact on the continued scaling of the semiconductor industry.
4. The seminar offers a wide variety of sample problems that participants work to help them gain knowledge of the fundamentals of wafer fab processing.
5. Participants will be able to identify the basic features and principles associated with each major processing step. These include processes like chemical vapor deposition, ion implantation, lithography, and etching.

6. Participants will understand how processing, reliability, power consumption and device performance are interrelated.
7. Participants will be able to make decisions about how to construct and evaluate processing steps for CMOS, BiCMOS, and bipolar technologies.

INSTRUCTIONAL STRATEGY

By using a combination of instruction by lecture, classroom exercises, and question/answer sessions, participants will learn practical information on semiconductor processing and the operation of this industry. From the very first moments of the seminar until the last sentence of the training, the driving instructional factor is **application**. We use instructors who are internationally recognized experts in their fields that have years of experience (both current and relevant) in this field. The accompanying textbook offers hundreds of pages of additional reference material participants can use back at their daily activities.

COURSE OUTLINE

Day 1

1. Module 1: Basics & Fundamentals; Semiconductor Devices and ICs
    a. Acronyms
    b. Common Terminology
    c. Brief History
    d. Semiconductor Materials
    e. Electrical Conductivity
    f. Semiconductor Devices
    g. Classification of ICs & IC Processes
    h. Integrated Circuit Types
2. Module 2: Crystallinity, Crystal Defects, Crystal Growth
    a. Crystallinity
    b. Crystal Defects
    c. Crystal Growth
    d. Controlling Crystal Defects
3. Module 3: Basic CMOS Process Flow
    a. Transistors and Isolation
    b. Contacts/Vias Formation
    c. Interconnects
    d. Parametric Testing
4. Module 4: Ion Implantation 1 (The Science)
    a. Doping Basics
    b. Ion Implantation Basics
    c. Dopant Profiles
    d. Crystal Damage & Annealing

5. Module 5: Ion Implantation 2 (Equipment, Process Issues)
    a. Equipment
    b. Process Challenges
    c. Process Monitoring & Characterization
    d. New Techniques

Day 2

6. Module 6: Thermal Processing
    a. Overview of Thermal Processing
    b. Process Applications of SiO2
    c. Thermal Oxidation
    d. Thermal Oxidation Reaction Kinetics
    e. Oxide Quality
    f. Atomistic Models of Thermal Diffusion
    g. Thermal Diffusion Kinetics
    h. Thermal Annealing
    i. Thermal Processing Hardware
    j. Process Control
7. Module 7: Contamination Monitoring and Control
    a. Contamination Forms & Effects
    b. Contamination Sources & Control
    c. Contamination Characterization & Measurement
8. Module 8: Wafer Cleaning
    a. Wafer Cleaning Strategies
    b. Chemical Cleaning
    c. Mechanical Cleaning
9. Module 9: Vacuum, Thin Film, & Plasma Basics
    a. Vacuum Basics
    b. Thin Film Basics
    c. Plasma Basics
10. Module 10: CVD 1 (Basics, LPCVD, Epitaxy)
    a. CVD Basics
    b. LPCVD Films
    c. LPCVD Equipment
    d. Epi Basics
    e. Epi Process Applications
    f. Epi Deposition Process
    g. Epi Deposition Equipment

Day 3

11. Module 11: PVD
    a. PVD (Physical Vapor Deposition) Basics
    b. Sputter Deposition Process
    c. Sputter Deposition Equipment
    d. Al-Based Films
    e. Step Coverage and Contact/Via Hole Filling
    f. Metal Film Evaluation
12. Module 12: Lithography 1 (Photoresist Processing)
    a. Basic Lithography Process
    b. Photoresist Materials
    c. Photoresist Process Flow
    d. Photoresist Processing Systems
13. Module 13: Lithography 2 (Image Formation)
    a. Basic Optics
    b. Imaging
    c. Equipment Overview
    d. Actinic Illumination
    e. Exposure Tools
14. Module 14: Lithgroaphy 3 (Registration, Photomasks, RETs)
    a. Registration
    b. Photomasks
    c. Resolution Enhancement Techniques
    d. The Evolution of Optical Lithography
15. Module 15: Etch 1 (Basics, Wet Etch, Dry Etch)
    a. Etch Basics
    b. Etch Terminology
    c. Wet Etch Overview
    d. Wet Etch Chemistries
    e. Types of Dry Etch Processes
    f. Physics & Chemistry of Plasma Etching

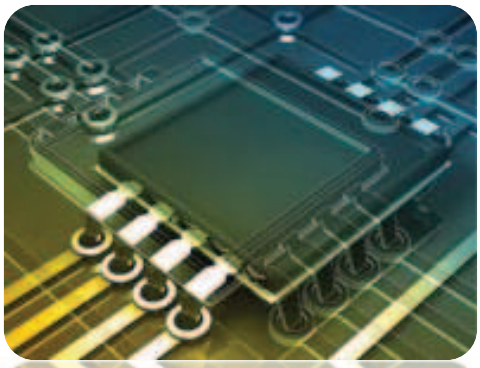
Day 4

16. Module 16: Etch 2 (Dry Etch Applications and Equipment)
    a. Dry Etch Applications
    b. SiO2
    c. Polysilicon
    d. Al & Al Alloys
    e. Photoresist Strip
    f. Silicon Nitride
    g. Dry Etch Equipment
    h. Batch Etchers
    i. Single Wafer Etchers
    j. Endpoint Detection
    k. Wafer Chucks
17. Module 17: CVD 2 (PECVD)
    a. CVD Basics
    b. PECVD Equipment
    c. CVD Films
    d. Step Coverage
18. Module 18: Chemical Mechanical Polishing
    a. Planarization Basics
    b. CMP Basics
    c. CMP Processes
    d. Process Challenges
    e. Equipment
    f. Process Control
19. Module 19: Copper Interconnect, Low-k Dielectrics
    a. Limitations of "Conventional" Interconnect
    b. Copper Interconnect
    c. Cu Electroplating
    d. Damascene Structures
    e. Low-k IMDs
    f. Cleaning Cu and low-k IMDs

20. Module 20: Leading Edge Technologies & Techniques
    a. Process Evolution
    b. Atomic Layer Deposition (ALD)
    c. High-k Gate and Capacitor Dielectrics
    d. Ni Silicide Contacts
    e. Metal Gates
    f. Silicon on Insulator (SOI) Technology
    g. Strained Silicon
    h. Hard Mask Trim Etch
    i. New Doping Techniques
    j. New Annealing Techniques
    k. Other New Techniques
    l. Summary of Industry Trends

References:

Wolf, Microchip Manufacturing,
Doering & Nishi, Semiconductor Manufacturing Technology, 2nd ed.
Wolf, Silicon Processing, Vol. 4
Wolf, Silicon Processing, Vol. 1, 2nd ed.



Upcoming Webinars

(Click on each item for details)

Design for Reliability WEBINAR

2 sessions of 4 hours each
Europe: June 13 – 14, 2022 (Mon – Tue), 1:00 P.M. – 5:00 P.M. CET

Semiconductor Reliability / Product Qualification WEBINAR

4 sessions of 4 hours each
US: August 15 – 18, 2022 (Mon – Thur), 8:00 A.M. – 12:00 NOON PDT

Wafer Fab Processing WEBINAR

4 sessions of 4 hours each
US: October 3 – 6, 2022 (Mon – Thur), 8:00 A.M. – 12:00 NOON PDT

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To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered in the next newsletter, please contact Jeremy Henderson by Email (jeremy.henderson@semitracks.com).
We are always looking for ways to enhance our courses and educational materials.

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We look forward to hearing from you!