Issue 142 April 2021

InfoTracks

Semitracks Monthly Newsletter

Resistors

By Christopher Henderson

This month, we will conclude our series of Feature Articles by discussing several case histories.

The first case history involves the failure of a thin-film resistor network. The thin-film resistor network uses nichrome as the resistor material, and in Figure 1 (a), we show an image of the resistor network chip. The resistor network was used inside of a hybrid microcircuit. One resistor in the network had a high resistance value, which caused the hybrid to malfunction. A detailed examination of the anomalous resistor revealed an area of missing nichrome thin film. The missing nichrome was located near the interface to the metal connect, as shown in Figure 1 (b). The appearance of the missing nichrome is typical of a reaction with water while in a biased condition. The water entered through a cracked glass seal on the hybrid lead.

In this Issue:

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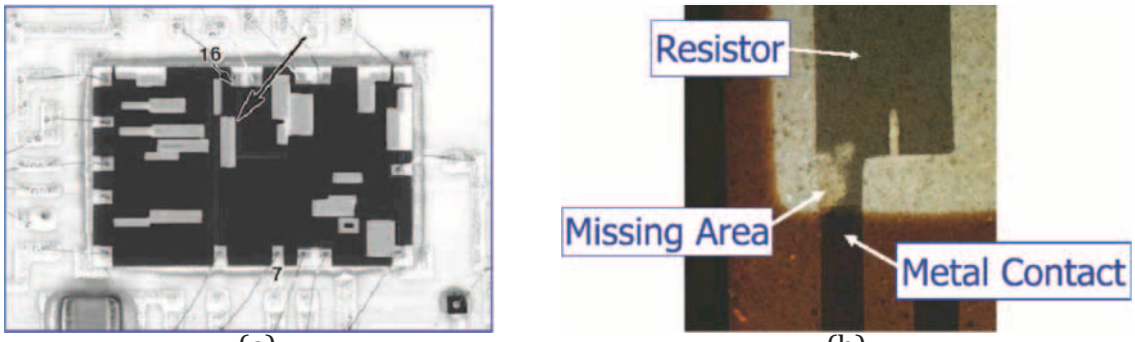


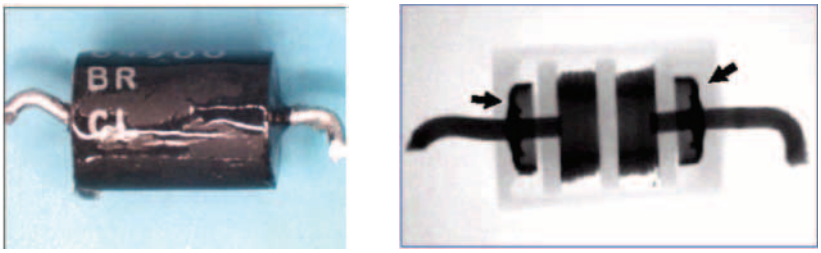
(a) (b)

Figure 1. (a) Resistor network chip used inside a hybrid microcircuit, and (b) Portion of a nichrome thin film showing a missing area of the element.

Next, let's discuss a case history involving several carbon composition resistors. The nominal values of these carbon composition resistors should be 10 kΩ +/- 5%. An example of a 10 kΩ carbon composition resistor is shown in Figure 2. Several of the carbon composition resistors submitted for analysis exhibited out-of-tolerance values, ranging from 10.8 to 11.5 kΩ. Nominally, they should be 10.0 +/- 5% or 9.5 to 10.5 kΩ. There was no external evidence of damage. The failure analysts baked the devices at 100°C for 24 hours, and measured the electrical characteristics afterwards. They noted that all of the devices were within nominal values after the bake. Carbon composition resistors are known to increase in resistance if exposed to atmospheric moisture for long periods, so it is likely that these devices failed due to moisture exposure.

Figure 2. 10 kΩ carbon composition resistor.

The third case history involves a wire-wound resistor. In this case study, the customer found a wire-wound resistor to be electrically open. We show the resistor in Figure 3 (a). An x-ray examination determined that the resistor wire was open at the interface to the end cap. Figure 3 (b) shows an x-ray image of the wire elements and the end caps.



(a) (b)

Figure 3. (a) Overall exterior view of a wire-wound resistor, and (b) X-ray image of the wire elements and the end caps (indicated by the arrows).

The enlarged x-ray image in Figure 4 shows that the wire is sandwiched between the weld tab and end cap. This type of wire is too fine to be welded directly to the end cap. The failure analyst then decapsulated the wire-wound resistor to perform an internal examination. The internal examination showed that the wire was excessively deformed by pressure and/or the weld.

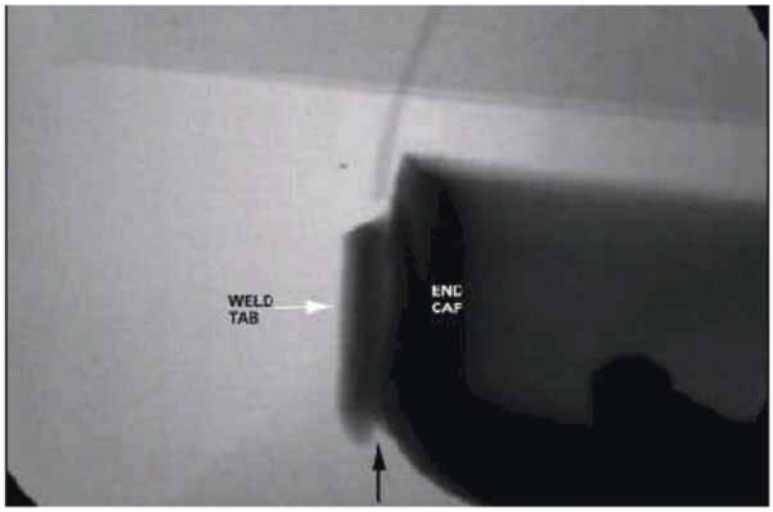


Figure 4. Enlarged x-ray view showing the open between the resistor wire and the end cap.

Figure 5 shows the internal view of the wire-to-end cap interface; however, the open is not obvious since the wire is held in place by a coating. Thermal cycling in the application then broke the wire at the thinned down area resulting in the open.

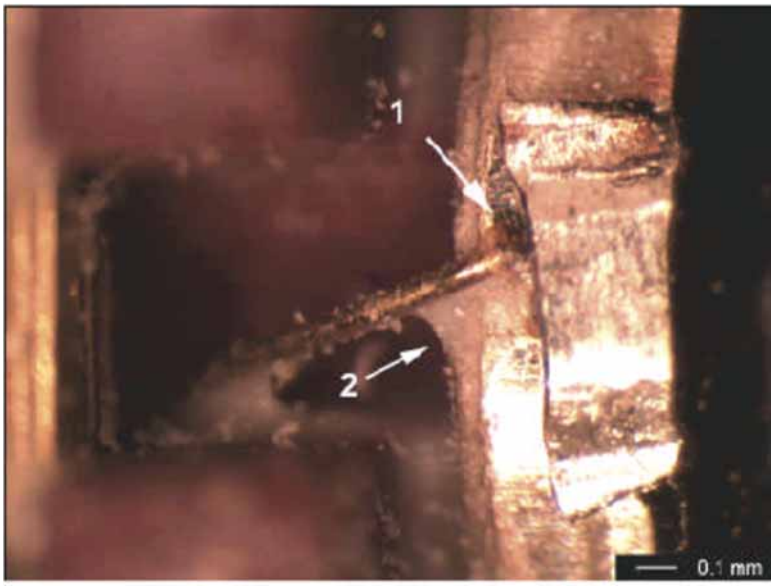
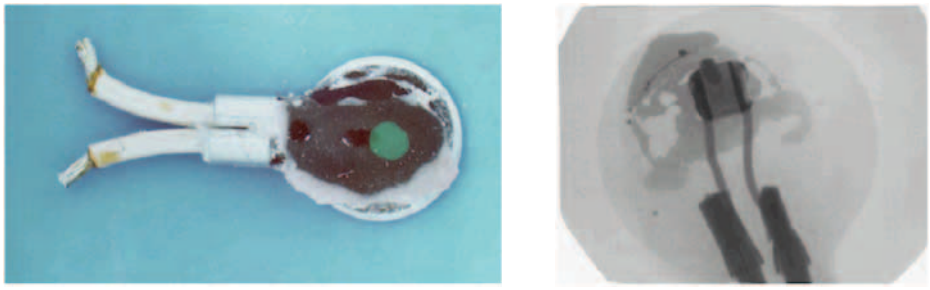


Figure 5. Internal view showing the wire-to-end cap interface.

The fourth case history involves a film resistor. In this case history, the film resistor was leaded and encapsulated, and was a precision resistor (as shown in Figure 6), nominally 1 kΩ ± 1%. Characterization indicated the device was under value at low currents and over value at higher currents. Furthermore, the curve tracer characterization showed non-linearity of the device I-V characteristic, indicating it was stable, and not self-heating induced. The failure analyst traced the non-linearity, using a microprobe station, to the metal system at the connection to the external leads. The external leads were welded to bond pads, and the bond pads had an under-plate to contact the resistor element. In this instance, incorrect processing caused the non-linearity.

Figure 6. Example of a precision film resistor.

The final case study involves a thermistor. In this case study, several shorted thermistors were received for analysis. Figure 7 (a) shows an overall view of the thermistor after it was removed from the circuit. An initial x-ray analysis revealed that the internal solder had bridged across the thermistor element, as shown in Figure 7 (b). Further analysis determined that the internal solder had a low melting point. Subsequent tests revealed that normal soldering installation procedures would not reflow the internal solder. Additional investigation determined that the thermistors were being mounted using an uncontrolled heat gun to quick cure the mounting material, causing uneven results.



(a) (b)

Figure 7. (a) Overall view of the thermistor after it was removed from the circuit, and (b) X-ray view of thermistor showing reflowed solder.

We can conclude from these case histories that resistor failures cannot be ignored, and are every bit as important as semiconductor and integrated circuit failures. In fact, resistor failures tend to occur more often due to their less-automated manufacturing techniques. We described general resistor construction. We provided an overview of the failure analysis approach, and described a number resistor failure analysis techniques, and the application of techniques to actual failures through the use of several case histories.

Technical Tidbit

Stress Control in Dielectric Layers

This month's Technical Tidbit covers stress control during deposition of dielectric layers. Stress is an important property to control, since high levels of stress can result in changes in transistor properties, stress induced voiding in metal lines adjacent to the dielectrics, and even wafer warpage.

We can adjust the stress in a dielectric layer through three major techniques: adjustment of stoichiometry (or the ratio of the elements in the layer), the addition of low frequency power, and through the adjustment of the carrier gas chemistry.

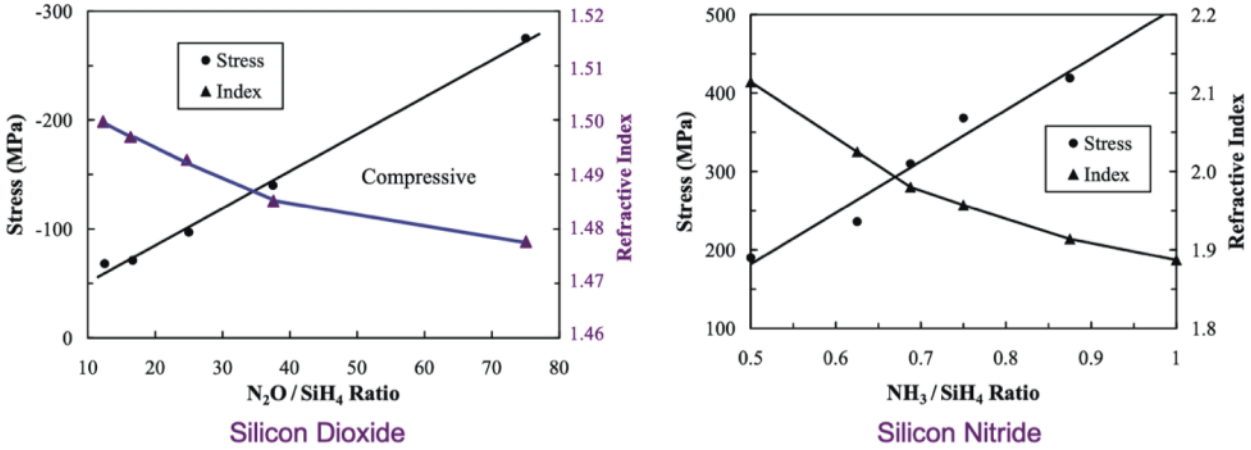


Figure 1. Stress and Refractive Index as a Function of the Ratio of the Input Gases.

The composition of PECVD SiO_2 and Si_3N_4 depends fundamentally on the respective N_2O/SiH_4 and NH_3/SiH_4 gas flow ratios. The two graphs shown in Figure 1 demonstrate, that by lowering the gas flow ratio to create a slightly Si-rich film, the stress decreases for both types of film. In the case of SiO_2 (the graph on the left of Figure 1), the film stress, which is compressive, decreases monotonically from about -300 MPa to a low value of -50 MPa as the N_2O/SiH_4 ratio decreases from 80 to approximately 10. This corresponds to a change in refractive index from 1.47 to approximately 1.50. For Si_3N_4 (the graph on the right of Figure 1), the film stress, which is tensile, can be adjusted from approximately 400 MPa to approximately 200 MPa as the NH_3/SiH_4 ratio decreases from approximately 0.9 to 0.5. This corresponds to a change in refractive index from about 1.9 to 2.1.

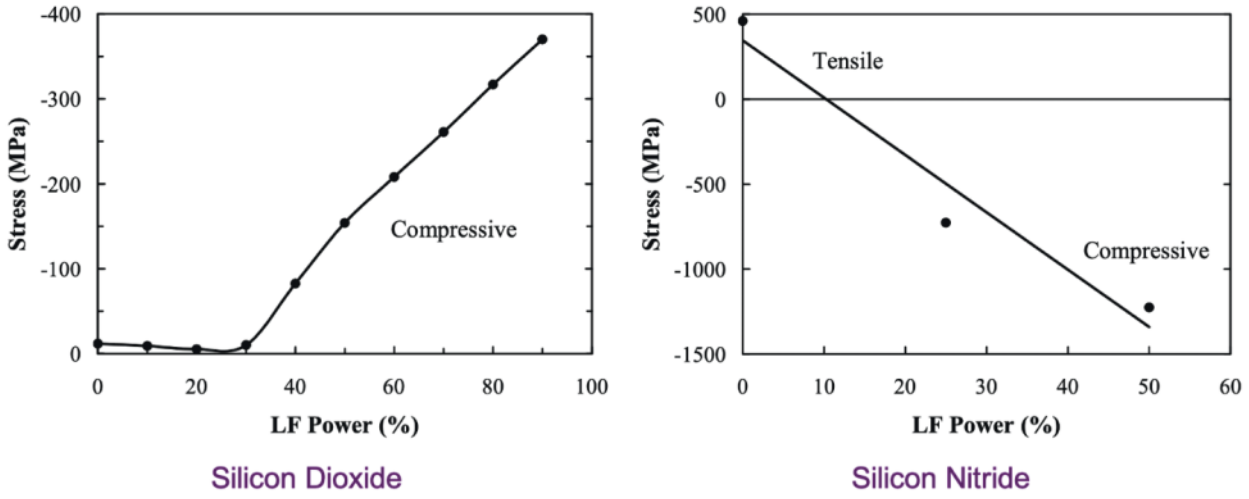


Figure 2. Stress as a Function of Low Frequency Power.

Another common technique to control the film stress of PECVD Si-based dielectrics in a conventional parallel plate reactor operating at 13.56 MHz is through the addition of low frequency power. The graph on the left of Figure 2 shows the stress in PECVD SiO_2 films as a function of added low-frequency power. In this example, the deposition rates were approximately 3000Å per minute. Also, in the graph on the left of Figure 2, the addition of low frequency power places SiO_2 in a compressive state. The graph on the right of Figure 2 shows the stress in PECVD Si_3N_4 films as a function of added low-frequency power. The deposition rates were between 500 and 1000Å per minute. Also, in the graph on the right of Figure 2, the addition of low frequency (380 kHz) power caused a controlled change in the stress state from tensile to compressive for Si_3N_4 films. The high-energy ion bombardment that occurs through the addition of low frequency (<1 MHz) is responsible for the compressive stress of the deposited films. The densification of the film caused by the ion bombardment causes the film to expand against its volume and therefore results in a compressive stress.

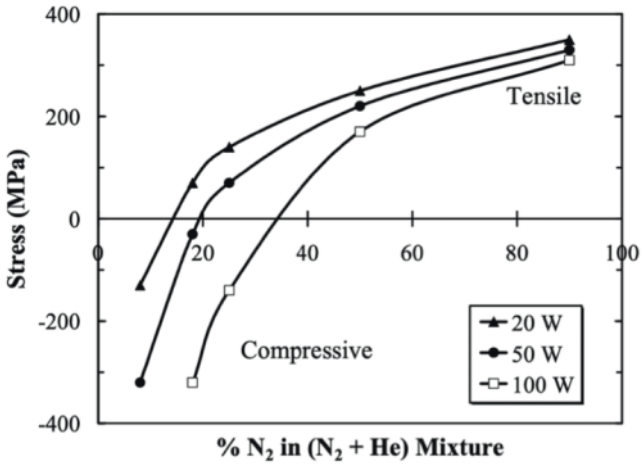


Figure 3. Stress as a Function of Added N_2 Gas.

A third technique for controlling stress is through the carrier gas chemistry. As we show here in Figure 3, it is possible, through the addition of He carrier gas to the standard mixture of SiH_4, NH_3 and N_2, to control the stress of Si_3N_4 from about 300 MPa tensile through zero to about

-300 MPa, compressive. Without the requirement of a low frequency source, the possibility of plasma-induced damage is reduced with this He dilution method, which operates at a low rf power density of less than 50 mW/cm^2.

Ask the Experts

Q: What is a Design Construction Certificate?

A: AA Design Construction Certificate is used in various qualification methods. It may also go by the name Certification of Design, Construction and Qualification. It serves as a document to let the customer know that the supplier's circuit has been designed and manufactured to the customer's specifications. It also provides the customer with information as to basic characteristics of the device, like wafer fab location, packaging location, die technology, wire bond materials, and a number of other parameters. There is a template available from the Automotive Electronics Council called AEC_Q100_CDC_Rev_H that can be used for this activity, and it is free to download from the Automotive Electronics Council website, www.aecouncil.com

Spotlight: IC Packaging Technology

OVERVIEW

Overview: Integrated Circuit packaging has always been integral to IC performance and functionality. An IC package serves many purposes: (1) pitch conversion between the fine features of the IC die and the system level interconnection, (2) chemical, environmental and mechanical protection, (3) heat transfer, (4) power, ground and signal distribution between the die and system, (5) handling robustness, and (6) die identification among many others. Numerous critical technologies have been developed to serve these functions, technologies that continue to advance with each new requirement for cost reduction, space savings, higher speed electrical performance, finer pitch, die surface fragility, new reliability requirements, and new applications. Packaging engineers must fully understand these technologies to design and fabricate future high-performance packages with high yields at exceptional low-costs to give their company a critical competitive advantage.

This two-day class will detail the vital technologies required to construct IC packages in a reliable, cost effective, and quick time to market fashion. When completed, the participant will understand the wide array of technologies available, how technologies interact, what choices must be made for a high-performance product vs. a consumer device, and how such choices impact the manufacturability, functionality, and reliability of the finished product. An emphasis will be given to manufacturing, processes and materials selection tailoring and development. Each fundamental package family will be discussed, including flip chip area array technologies, Wafer Level Packaging (WLP), Fan-Out Wafer Level Packaging (FO-WLP), and the latest Through Silicon Via (TSV) developments. Additionally, future directions for each package technology will be highlighted, along with challenges that must be surmounted to succeed.

WHAT WILL I LEARN BY TAKING THIS CLASS?

1. **Molded Package Technologies.** Participants learn the fundamentals of molding critical to leaded, leadless, and area array packaging, enabling them to eliminate problems such as flash, incomplete fill, and wire sweep.
2. **Flip Chip Technologies.** Participants learn the fundamentals of plating, bumping, reflow, underfill, and substrate technologies that are required for both high performance and portable products.
3. **Wafer Level Packages.** Participants learn the newest technologies that enable the increasingly popular Wafer Chip Scale Level Packages (WCSPs) and Fan-Out Wafer Level Packages (FO-WLPs).
4. **Through Silicon Via Packages and Future Directions.** Participants will know the latest advances in the recently productized TSV technology, as well as future directions that will lead to the products of tomorrow.

COURSE OBJECTIVES

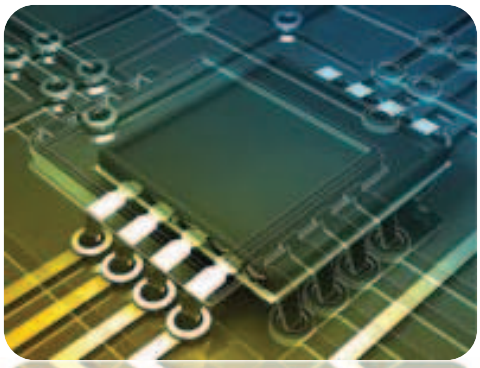
1. The course will supply participants with an in-depth understanding of package technologies current and future.
2. Potential defects associated with each package technology will be highlighted to enable the student to identify and eliminate such issues in product from both internal assembly and OSAT houses.

3. Cu and solder plating technologies will be described with special emphasis on package applications in TSVs and Cu pillars for FO-WLPs. Emphasis will be placed on eliminating issues such as reliability, non-uniformity, void free thermal aging performance, and contamination free interfaces.
4. New package processes employed in Through Silicon Via production will be described, along with current cost reduction thrusts, to enable the student to understand the advantages and limits of the technologies.
5. Temporary bonding and wafer thinning processes will be highlighted, as well as the cost reduction approaches currently being pursued to enable wider adoption of TSV packages.
6. The trade-offs between silicon, glass, and organic interposers will be highlighted, along with the processes used for each.
7. Participants will gain an understanding of the surface mount technologies that enable today's fine pitch products.
8. The class will provide detailed references for participants to study and further deepen their understanding.

COURSE OUTLINE

1. The Package Development Process as a Package Technology:
   a. Materials and Process Co-Design
2. Molded Package Technologies:
   a. Die Attach
      i. Plasma Cleans
   b. Wire Bonding
      i. Au vs. Cu vs. Ag
      ii. Die Design for Wire Bonding
   c. Lead Frames
   d. Transfer and Liquid Molding
      i. Flash
      ii. Incomplete Fill
      iii. Wire Sweep
      iv. Green Materials
   e. Pre- vs. Post-Mold Plating
   f. Trim Form
   g. Saw Singulation
   h. High Temperature and High Voltage Materials
3. Flip Chip and Ball Grid Array Technologies:
   a. Wafer Bumping Processing
      i. Cu and Solder Plating
      ii. Cu Pillar Processing
   b. Die Design for Wafer Bumping
   c. Flip Chip Joining
   d. Underfills

   e. Substrate Technologies
      i. Surface Finish Trade-Offs
      ii. Core, Build-up, and Coreless
   f. Thermal Interface Materials (TIMs) and Lids
   g. Fine Pitch Warpage Reduction
   h. Stacked Die and Stacked Packages
   i. Material Selection for Board Level Temperature Cycling and Drop Reliability
4. Wafer Chip Scale Packages:
   a. Redistribution Layer Processing
   b. Packing and Handling
   c. Underfill vs. No-Underfill
5. Fan-Out Wafer Level Packages:
   a. Chip First vs. Chip Last Technologies
   b. Redistribution Layer Processing
   c. Through Mold Vias
6. Through Silicon Via Technologies:
   a. Current Examples
   b. Fundamental TSV Process Steps
      i. TSV Etching
      ii. Cu Deep Via Plating
      iii. Temporary Carrier Attach
      iv. Wafer Thinning
   c. Die Stacking and Reflow
   d. Underfills
   e. Interposer Technologies: Silicon, Glass, Organic
7. Surface Mount Technologies:
   a. PCB Types
   b. Solder Pastes
   c. Solder Stencils
   d. Solder Reflow



Upcoming Webinars

(Click on each item for details)

Advanced CMOS/FinFET Fabrication

4 sessions of 2 hours each
US: May 25 – 28, 2021 (Tue – Fri),
8:00 A.M. – 10:00 A.M. PDT

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We are always looking for ways to enhance our courses and educational materials.

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We look forward to hearing from you!