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Reliability Test Equipment: Packaged Parts

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This document covers reliability test equipment for packaged parts.

Figure 1. Examples of temperature and temperature/humidity chambers.

In addition to the equipment needed to hold the wafers and provide electrical contact, reliability test requires equipment to create the ambient environment for accelerated testing. This includes temperature and temperature/humidity chambers. Several companies make systems that directly address semiconductor reliability. FormFactor, Micro Instrument Company, and Qualitau manufacture systems specifically for reliability testing. Companies like Thermotron and ESPEC manufacture multi-purpose chambers that are used for reliability testing. Also, there are hundreds of

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temperature chamber manufacturers that make basic oven systems. Some of the more well-known companies in this area are Aehr, Blue-M and Delta Designs. Temperature/humidity chambers, also called Highly Accelerated Stress Test or HAST chambers, are used when performing reliability testing involving moisture. Companies that manufacture these types of chambers include ESPEC, Hirayama, and Thermotron.

Figure 2. llustration of packaged part test system from Qualitau.

Qualitau is the largest supplier that deals exclusively with the semiconductor reliability market. It is one of the most popular packaged part test systems on the market. It can hold up to 1024 parts when fully populated with 16 64-socket cards. It can test parts at temperatures as high as 350°C. The Multiple Interface Reliability Analyzer, or MIRA system, can be used to perform TDDB, hot carrier, and electromigration testing. It can do this on packaged devices and also at the wafer level. Qualitau also sells systems that are dedicated to specific mechanisms. For instance, the Infinity tester handles TDDB testing, while the ACE tester performs electromigration testing. They also manufacture a multiprobe system for multiple sites in parallel.

Figure 3. Illustration of packaged part test system from FormFactor.

The FormFactor system is very similar to the Qualitau system. It has multiple temperature chambers on individual controls, giving it some additional flexibility. The FormFactor systems can also perform electromigration, hot carrier, and TDDB tests.

Figure 4. Illustration of packaged part test system from Micro Control Company.

The Micro Control Company system is somewhat similar to the Qualitau system. It has individual device temperature controls, giving it some additional flexibility. The Micro Control Company systems can also perform electromigration, hot carrier, and TDDB tests.

Highly Accelerated Stress Testing or HAST requires specialized ovens. They must be able to withstand high temperatures, high humidity levels, and pressure. In order to achieve high temperature and high humidity at the same time, the vapor pressure of H2O in the chamber must exceed one atmosphere, making pressure containment necessary. There are numerous vendors for this equipment. Three well-known manufacturers are Micro Instrument Company, ESPEC, and Hirayama. These chambers can be quite expensive. In order to test a sufficient number of devices, one might have to purchase a number of chambers. Since these studies are done somewhat infrequently, it may make sense to contract this test out to a test laboratory. Tandex Labs and Environmental Associates are two companies that provide this service.

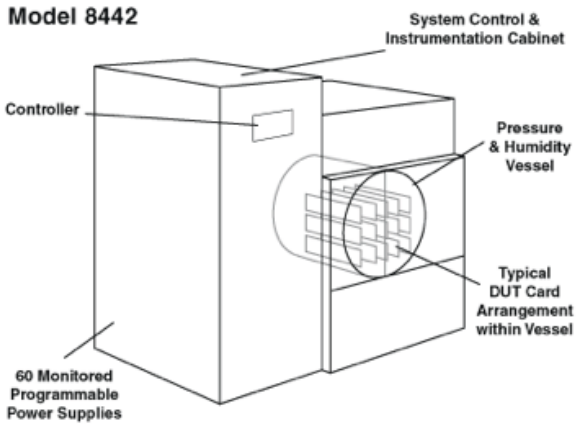


Figure 5. Diagram of specialized oven for HAST testing from Micro Instrument.

This instrument from the Micro Instrument Company can operate at temperatures up to 166°C, 100% relative humidity and 90 psi. In order for the chambers to withstand this combination of heat and humidity, special care must be taken to ensure there are no exposed parts that can rust.

- Non-condensing atmosphere, no rain
- Fully self contained – No special facilities or plumbing required
- Without FANS – A uniform non-condensing atmosphere
- Self-cleaning features
- Does NOT produce any waste by-products
- Self-locking door with built in safety features
- Drain could be a simple bucket
- Electronic system totally isolated from the main chamber and plumbing
- Stainless steel plumbing circulates all incoming water
- Non corrosive atmosphere

Figure 6. Illustration of specialized oven for HAST testing from Hirayama.

Hirayama is another manufacturer. This system is fully self-contained and operates without fans. The electronics are isolated from the main chamber and plumbing to ensure they do not degrade. It is self-cleaning and does not generate a corrosive atmosphere.

- Automatic humidity filling
- Automatic door lock
- Square workspace allows more product to be loaded
- Hermetic power-pin system for bias testing
- Hermetic port connection allows special signal lines like coax or fiber optics to be run into the chamber; can use hermetic port plugs like those from Buffalo Conax with the port system

Figure 7. Illustration of specialized oven for HAST testing from ESPEC.

The system shown here in Figure 7 by ESPEC has automatic humidity filling and an automatic door lock. The space in the chamber has been optimized to hold the most possible devices for test. The system also contains hermetic ports to allow cabling to be run through the chamber walls for electrical monitoring during testing.

In conclusion, there is a wide variety of test equipment, probe cards, and probes available on the market. Since many systems and components are designed for certain applications, one needs to understand the test scenario and issues before purchasing a system or setting up for a test. Some of the more important issues include the sensitivity of the voltage and current measurements, the test frequency, the duration of the test, and thermal expansion. These all help determine whether tri-axial shielding is necessary, the type of probe cards and probes, the type of wafer chuck, the necessary overdrive, the type of HAST system, etc.

Technical Tidbit

Retrograde Implants

This month's technical tidbit covers retrograde implants.

One type of implant that might be necessary is the retrograde implant. A retrograde implant produces higher doping below the surface than at the surface, which is opposite to a standard diffusion profile. A retrograde implant is typically performed before the polysilicon deposition, so that it affects the entire well region, not just the source and drain regions. The extra dopant atoms deeper beneath the surface can help to prevent punchthrough under the halo implants. They can help prevent parasitic channel formation on the active sidewall beneath the source-drain regions. Faster diffusing ions like boron, phosphorus, or arsenic are okay for this type of implant.

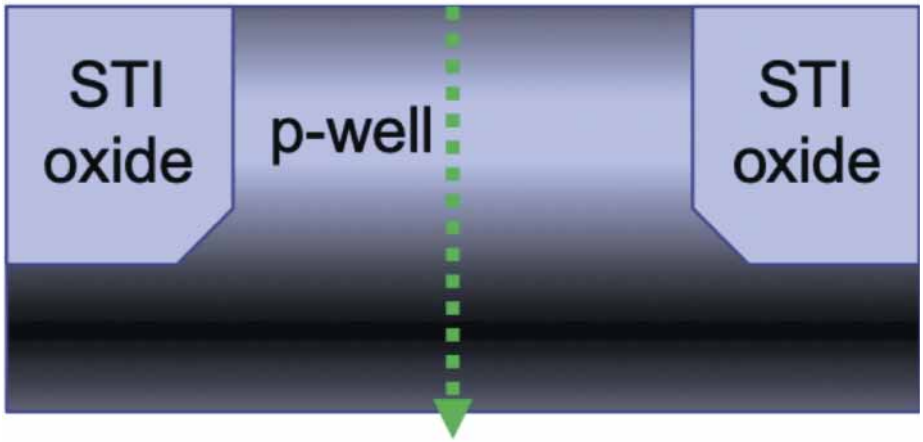


Figure 1. Example application of retrograde implant: transistor well.

Another type of retrograde implant is a shallow or steep surface channel implant. These might be done to control the threshold voltage, or to reduce noise in a transistor. Because the placement of these ions is critical, engineers typically use bigger ions like gallium or antimony, since they are slower diffusers. Yet another type of retrograde implant is the very high dose deep implant. These might be used for latch-up prevention, or for noise immunity. These ions can be smaller, because accurate placement is not as critical, so boron, phosphorus and arsenic are okay. Finally, the implant order matters to prevent ion channeling, especially for the shallow implant.

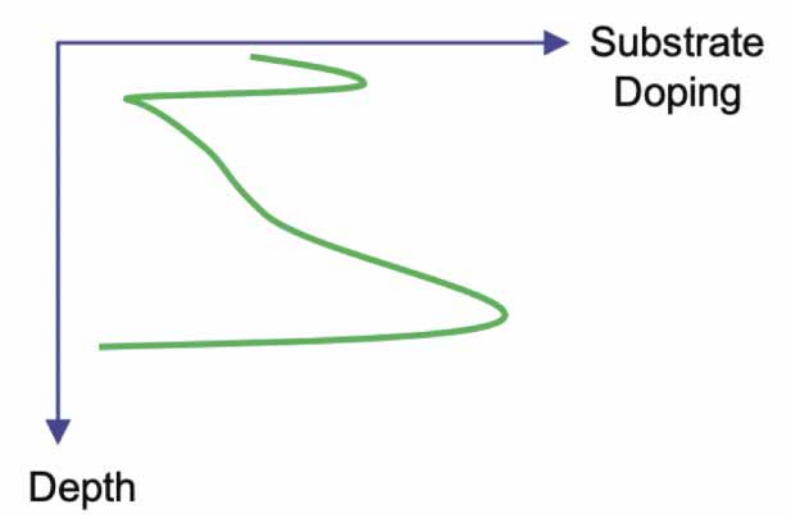


Figure 2. Example retrograde well doping concentration profile as a function of depth.

Ask the Experts

Q: Are there chemicals or treatments on the leadframe to prevent epoxy bleed-out?

A: Resin bleed-out tends to occur on high energy surfaces such as metal leadframes without any organic coating. In particular, if plasma cleaning is utilized to remove the contaminants prior to assembly, the bleeding issue may become more pronounced due to the increase in surface energy. There are several approaches to control or eliminate resin bleed-out. These approaches include modifying formulation by selecting appropriate anti-EBO, using die attach film (DAF)/B-stage epoxy, controlling surface roughness, creating mechanical barrier, and lowering the surface energy of lead frames by surface coating.

Spotlight: Semiconductor Reliability and Product Qualification

OVERVIEW

Package reliability and product qualification continues to evolve with the electronics industry. New electronics applications require new approaches to reliability and qualification. In the past, reliability meant discovering, characterizing and modeling failure mechanisms and determining their impact on the reliability of the circuit. Today, reliability can involve tradeoffs between performance and reliability, assessing the impact of new materials, dealing with limited margins, etc. in particular, the proliferation of new package types. This requires information on subjects like: statistics, testing, technology, processing, materials science, chemistry, and customer expectations. While customers expect high reliability levels, incorrect testing, calculations, and qualification procedures can severely impact reliability. Your company needs competent engineers and scientists to help solve these problems. ***Semiconductor Reliability and Qualification*** is a four-day course that offers detailed instruction on a variety of subjects pertaining to semiconductor reliability and qualification. This course is designed for every manager, engineer, and technician concerned with reliability in the semiconductor field, qualifying semiconductor components, or supplying tools to the industry.

What Will I Learn By Taking This Class?

Participants learn to develop the skills to determine what failure mechanisms might occur, and how to test for them, develop models for them, and eliminate them from the product.

1. **Overview of Reliability and Statistics.** Participants learn the fundamentals of statistics, sample sizes, distributions and their parameters.
2. **Failure Mechanisms.** Participants learn the nature and manifestation of a variety of failure mechanisms that can occur both at the die and at the package level. These include: time-dependent dielectric breakdown, hot carrier degradation, electromigration, stress-induced voiding, moisture, corrosion, contamination, thermomechanical effects, interfacial fatigue, etc.
3. **Qualification Principles.** Participants learn how test structures can be designed to help test for a particular failure mechanism.
4. **Test Strategies.** Participants learn about the JEDEC test standards, how to design screening tests, and how to perform burn-in testing effectively.

COURSE OBJECTIVES

1. The seminar will provide participants with an in-depth understanding of the failure mechanisms, test structures, equipment, and testing methods used to achieve today's high reliability components.
2. Participants will be able to gather data, determine how best to plot the data and make inferences from that data.
3. The seminar will identify the major failure mechanisms, explain how they are observed, how they are modeled, and how they are eliminated.
4. The seminar offers a variety of video demonstrations of analysis techniques, so the participants can get an understanding of the types of results they might expect to see with their equipment.
5. Participants will be able to identify the steps and create a basic qualification process for semiconductor devices.

6. Participants will be able to knowledgeably implement screens that are appropriate to assure the reliability of a component.
7. Participants will be able to identify appropriate tools to purchase when starting or expanding a laboratory.

COURSE OUTLINE

Day 1 (Lecture Time 8 Hours)

1. Introduction to Reliability
    1. Basic Concepts
    2. Definitions
    3. Historical Information
2. Statistics and Distributions
    1. Basic Statistics
    2. Distributions (Normal, Lognormal, Exponent, Weibull)
    3. Which Distribution Should I Use?
    4. Acceleration
    5. Number of Failures

Day 2 (Lecture Time 8 Hours)

1. Overview of Die-Level Failure Mechanisms
    1. Time Dependent Dielectric Breakdown
    2. Hot Carrier Damage
    3. Negative Bias Temperature Instability
    4. Electromigration
    5. Stress Induced Voiding
2. Package Level Mechanisms
    1. Ionic Contamination
    2. Moisture/Corrosion
        1. Failure Mechanisms
        2. Models for Humidity
        3. Tja Considerations
        4. Static and Periodic stresses
        5. Exercises
    3. Thermo-Mechanical Stress
        1. Models
        2. Failure Mechanisms
    4. Interfacial Fatigue
        1. Low-K fracture
    5. Thermal Degradation/Oxidation

Day 3 (Lecture Time 8 Hours)

1. Package Attach (Solder) Reliability
    1. Creep/Sheer/Strain
    2. Lead-Free Issues
    3. Electromigration/Thermomigration
    4. MSL Testing
    5. Exercises
2. TSV Reliability Overview
3. Board Level Reliability Mechanisms
    1. Interposer
    2. Substrate
4. Electrical Overstress/ESD
5. Test Structures and Test Equipment
6. Developing Screens, Stress Tests, and Life Tests
    1. Burn-In
    2. Life Testing
    3. HAST
    4. JEDEC-based Tests
    5. Exercises

Day 4 (Lecture Time 8 Hours)

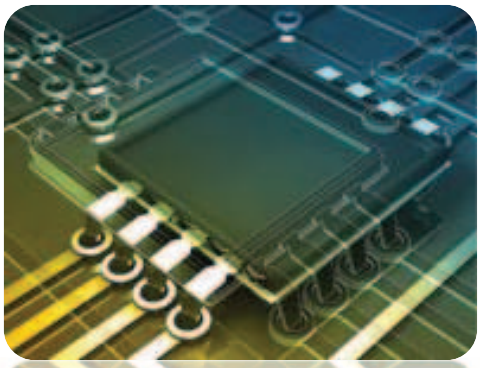
1. Calculating Chip and System Level Reliability
2. Developing a Qualification Program
    1. Process
    2. Standards-Based Qualification
    3. Knowledge-Based Qualification
    4. MIL-STD Qualification
    5. JEDEC Documents (JESD47H, JESD94, JEP148)
    6. AEC-Q100 Qualification
    7. When do I deviate? How do I handle additional requirements?
    8. Exercises and Discussion

INSTRUCTIONAL STRATEGY

By using a combination of instruction by lecture, video, problem solving and question/answer sessions, participants will learn practical approaches to the failure analysis process. From the very first moments of the seminar until the last sentence of the training, the driving instructional factor is **application**. We use instructors who are internationally recognized experts in their fields that have years of experience (both current and relevant) in this field. The handbook offers hundreds of pages of additional reference material the participants can use back at their daily activities.

The Semitracks Analysis Instructional Videos™

One unique feature of this workshop is the video segments used to help train the students. Reliability Analysis is a visual discipline. The ability to identify nuances and subtleties in graphical data is critical to locating and understanding the defect. Some tools output video images that must be interpreted by engineers and scientists. No other course of this type uses this medium to help train the participants. These videos allow the analysts to directly compare material they learn in this course with real analysis work they do in their daily activities.



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(Click on each item for details)

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Date To Be Determined
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Semiconductor Reliability / Product Qualification
Date To Be Determined
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Failure and Yield Analysis
Date To Be Determined
Munich, Germany

IC Packaging Technology
Date To Be Determined
Munich, Germany

Advanced CMOS/FinFET Fabrication
Date To Be Determined
Munich, Germany