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InfoTracks

Semitracks Monthly Newsletter

Bump Processes—Part II

By Christopher Henderson

This month, we continue our look into bump processes. Let's look at fine or tight pitch issues a little further. Notice that if we have an 80µm pitch pad structure and use an 85µm height solder bump we can have problems with shorting between bumps. We can eliminate this problem by going to a 40µm solder bump, but this introduces other problems. For example, a small bump will be more susceptible to electromigration. The shorter height may also introduce manufacturing problems, like flowing underfill around the solder bumps efficiently. This is where the copper pillar can be advantageous. We can easily achieve an 80µm pitch and an 85µm height because of the pillar shape and eliminate wetting to the sidewalls, which might increase the pillar width.

For copper pillar bumping, we can use the same two approaches: solder masked defined and pad defined. In the solder mask defined approach, we deposit solder in the openings in the solder mask, bring the chip with its copper pillars in contact to the solder, and then reflow the solder to make the connection. In the pad-defined process, we deposit solder on the copper pillar, bring the chip in contact to the bare copper pad, and then reflow the solder. This creates the connection between the chip and the substrate.

In this Issue:

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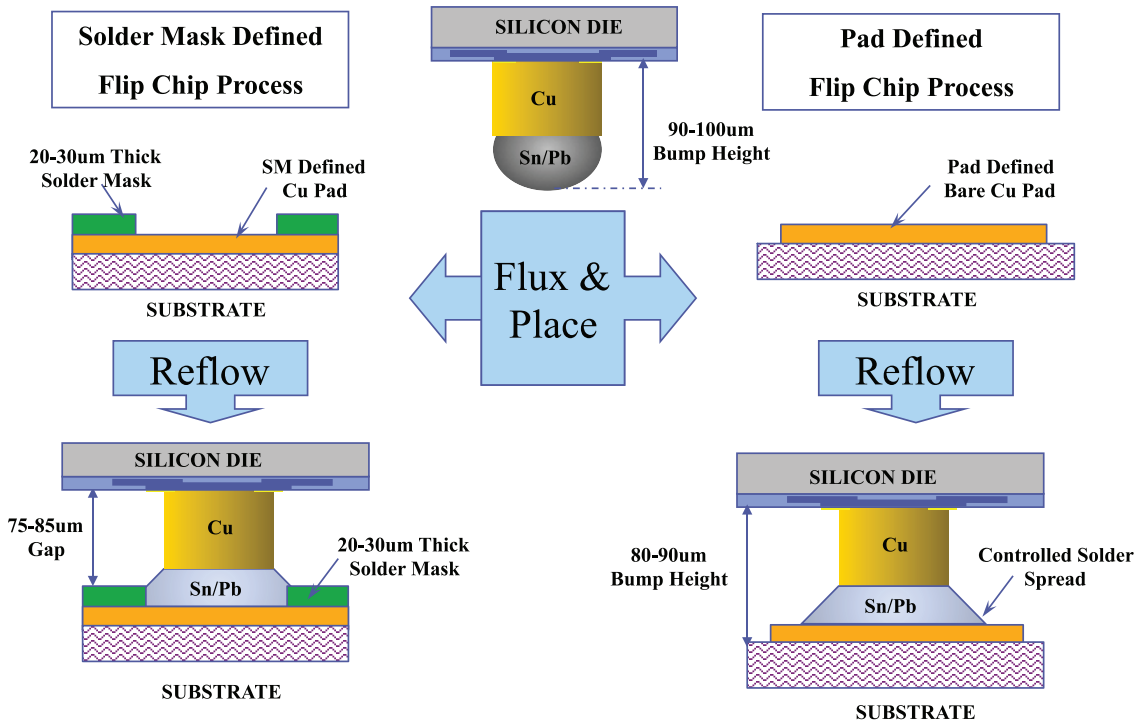


Figure 1. Solder Mask Defined and Pad Defined Solder Bump Processes.

This series of diagrams in Figure 2 help to describe the copper pillar bump process flow. After wafer cleaning, one sputters titanium and then copper on top of the chip and patterns these materials such that they only remain on the pads. After etching the Under Bump Metallization (UBM) metals and removing the resist, one can then expose and develop an area above the bond pads and then electro-deposit a copper layer that forms the pillar, followed by solder. Once the solder is deposited, one can remove the resist and reflow the solder to create the solder bump on top of the pillar.

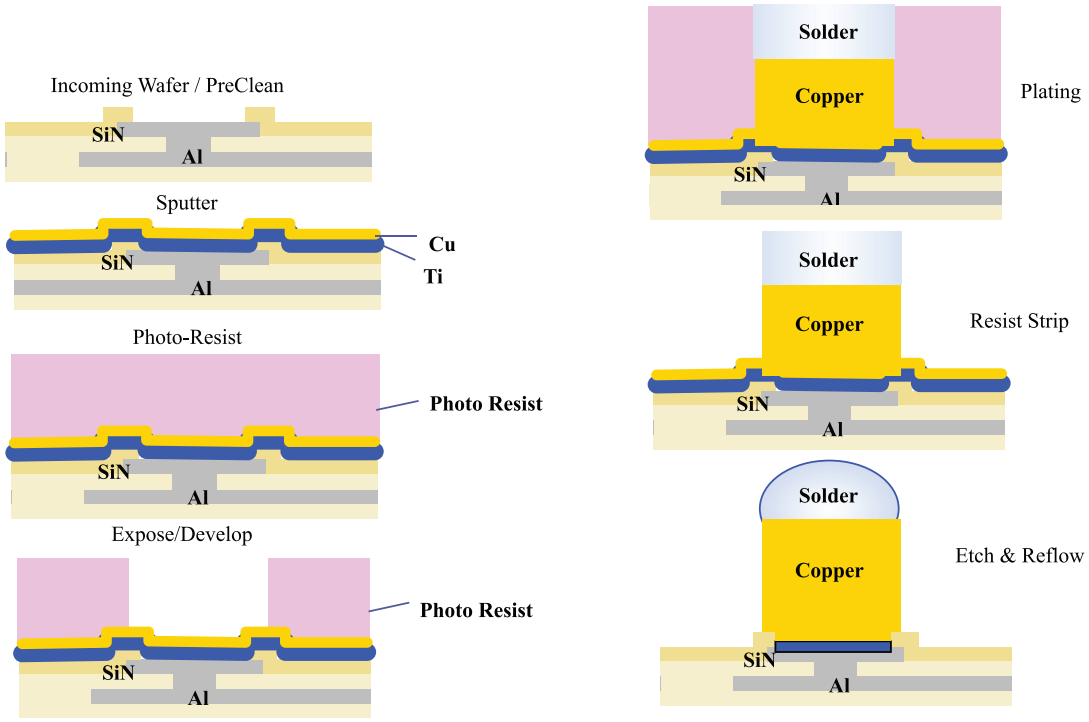


Figure 2. Common Copper Pillar Bump Process Flow.

Figure 3 shows the equipment used for ball attach reflow and wash. This is a typical in-line process for Ball Grid Array packages.

Figure 3. Ball attach reflow and wash equipment.

One method for creating solder balls is to use a screen print process. The engineers use a stencil and substrate to create the solder balls and simultaneously align them to the package and board. The

Flux/Paste is for the balls; the flux dissolves the native oxides on the balls, permitting wetting. The stencil can then be used with the ball mounter head. It is attached to the ball mounter head. The ball mounter head is a vacuum chuck that picks up the balls from the ball reservoir, aligning them to the stencil. At attachment one releases the vacuum to let the balls stick in the flux.

To improve bonding, it can be helpful to use a noble metal bond pad cap. This helps prevent oxidation and diffusion of other materials. BOAC is one such technology; it uses a copper nickel palladium gold structure that resists intermetallics. It works well for high temperatures. Some companies use deposited copper or thick metal copper layer with a nickel-palladium capping layer.

Next month in Part III we will discuss redistribution layers and the methods for creating these layers.

Technical Tidbit

Packing and Shipping Labels

*After initial packing, the reels, tubes, and trays are usually then packed into boxes for shipping. *Most large semiconductor manufacturers use distribution centers located in or *near major worldwide shipping hubs. Most components are also small enough that they can be shipped by air via UPS, FedEx, DHL, or other couriers. One concern with shipping components is that components are generally static sensitive, and the shipping process does not allow for static control. In order to protect the components, engineers will use static protective bags, tubes and reels. Furthermore, they use labels to indicate that the components being transported are static sensitive. The semiconductor industry uses labels like the ones we show on the right to indicate static sensitivity. The military
requires labels, and JEDEC-compliancy requires the labels as well. One must put labels on the unit pack and the intermediate and exterior containers.

Figure 1. ESD Shipping Labels.

Components also need to be labeled as to their moisture sensitivity. The moisture that is being absorbed by the device is inherent during the assembly and molding process and this moisture trapped within the device may cause the unit to crack, known as the popcorn effect, during IR reflow, vapor phase reflow, or similar processes at board mounting operation due to the high amount of heat that is being applied. The bake step we mentioned removes this trapped moisture inside the package at a slower pace without causing any package cracking or solderability concerns. The units can then be dry packed afterwards to ensure no moisture absorption will take place until the devices are ready to be mounted to the boards by our customers. Operators then list the MSL sensitivity on the labels on the exterior of the box and dry-ship bags.

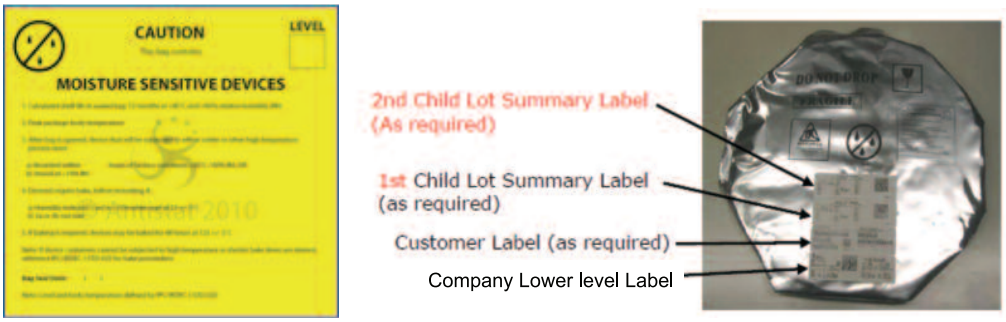


Figure 2. Moisture sensitive devices label (left) and dry pack shipping bag (right).

Spotlight: Product Qualification

OVERVIEW

Package reliability and qualification continues to evolve with the electronics industry. New electronics applications require new approaches to reliability and qualification. In the past, reliability meant discovering, characterizing and modeling failure mechanisms and determining their impact on the reliability of the circuit. Today, reliability can also involve tradeoffs between performance and reliability, assessing the impact of new materials, dealing with limited margins, etc. In particular, the proliferation of new package types can create difficulties. This requires information on subjects like: statistics, testing, technology, processing, materials science, chemistry, and customer expectations. Customers expect fast, smooth qualification, but incorrect assumptions, use conditions, testing, calculations, and qualification procedures can severely impact this process. Your company needs competent engineers and scientists to help solve these problems. ***Product Qualification*** is a two-day course that offers detailed instruction on a variety of subjects pertaining to semiconductor technology and product qualification. This course is designed for every manager, engineer, and technician concerned with qualification in the semiconductor field, qualifying semiconductor components, or supplying tools to the industry.

Participants learn to develop the skills to determine the best process for qualification, how to identify issues and how to resolve them.

1. **Overview of Reliability and Statistics.** Participants learn the fundamentals of statistics, sample sizes, distributions and relationship to qualification.
2. **Failure Mechanisms.** Participants learn how product qualification and failure mechanisms relate to one another. We provide an overview of these mechanisms. These include: time-dependent dielectric breakdown, hot carrier degradation, electromigration, stress-induced voiding, moisture, corrosion, contamination, thermomechanical effects, interfacial fatigue, EOS, ESD, latchup, drop tests, etc.
3. **Qualification Principles.** Participants learn how test structures can be designed to help test for a particular failure mechanism.
4. **Test Strategies.** Participants learn about the JEDEC test standards, how to design screening tests, and how to perform burn-in testing effectively.

COURSE OBJECTIVES

1. The seminar will provide participants with an in-depth understanding of the failure mechanisms, test structures, equipment, and testing methods used to qualify today's components.
2. Participants will be able to gather data, determine how best to plot the data and make inferences from that data.
3. The seminar will identify major failure mechanisms; explain how they are observed, how they are modeled, and how they are handled in qualification.
4. The seminar will discuss the major qualification processes, including JEDEC JESD47, AEC Q-100, MIL-STD, and other related documents.

5. Participants will be able to identify the steps and create a basic qualification process for semiconductor devices.
6. Participants will be able to knowledgeably implement additional tests that are appropriate to assure the reliability of a component.
7. Participants will be able to identify appropriate tools to purchase when starting or expanding a laboratory.

INSTRUCTIONAL STRATEGY

By using a combination of instruction by lecture, classroom exercises, and question/answer sessions, participants will learn practical information on semiconductor processing and the operation of this industry. From the very first moments of the seminar until the last sentence of the training, the driving instructional factor is **application**. We use instructors who are internationally recognized experts in their fields that have years of experience (both current and relevant) in this field. The accompanying textbook offers hundreds of pages of additional reference material participants can use back at their daily activities.

COURSE OUTLINE

1. Introduction to Reliability
   a. Basic Concepts
   b. Definitions
   c. Historical Information
2. Statistics and Distributions
   a. Basic Statistics
   b. Distributions (Normal, Lognormal, Exponent, Weibull)
   c. Which Distribution Should I Use?
   d. Acceleration
   e. Number of Failures
3. Overview of Die-Level Failure Mechanisms
   a. Time Dependent Dielectric Breakdown
   b. Hot Carrier Damage
   c. Negative Bias Temperature Instability
   d. Electromigration
   e. Stress Induced Voiding
4. Overview of Package Level Mechanisms
   a. Ionic Contamination
   b. Moisture/Corrosion
   c. Thermo-Mechanical Stress
   d. Interfacial Fatigue
   e. Thermal Degradation/Oxidation
   f. Solder Joint Reliability

5. Overview of Board Level Reliability
   a. Solder Joint Reliability
   b. EOS/ESD/LatchUp
   c. Single Event Effects

Day Two (Lecture Time 8 Hours)

6. Test Structures and Test Equipment
7. Developing Screens, Stress Tests, and Life Tests
   a. Burn-In
   b. Life Testing
   c. HAST
   d. JEDEC-based Tests
   e. Exercises
8. Developing a Qualification Program
   a. Process
   b. Standards-Based Qualification
   c. Knowledge-Based Qualification
   d. MIL-STD Qualification
   e. JEDEC Documents (JESD47H, JESD94, JEP148)
   f. AEC-Q100 Qualification
   g. When do I deviate? How do I handle additional requirements?
   h. Exercises

Semitracks will be present at the

2014 International Reliability Physics Symposium (IRPS)

June 1 – 5

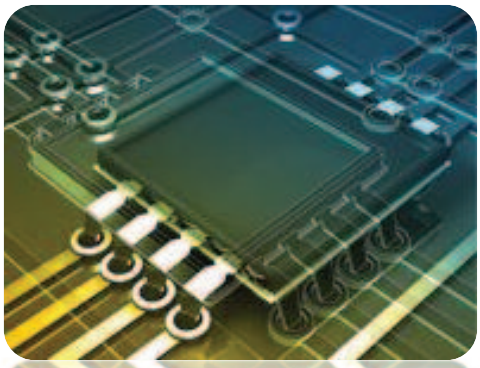
Hilton Waikoloa Village • Hawaii

Stop by and see us!

For more information on IRPS, please go to www.irps.org.

Please feel free to contact us to set up an appointment while you are there!

http://www.irps.org



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To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered in the next newsletter, please contact Jeremy Henderson by Email (jeremy.henderson@semitracks.com).
We are always looking for ways to enhance our courses and educational materials.

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http://www.semitracks.com

To post, read, or answer a question, visit our forums.
We look forward to hearing from you!

Upcoming Courses

(Click on each item for details)

Failure and Yield Analysis
May 5 – 8, 2014 (Mon – Thur)
Munich, Germany

MEMS Technology
May 12 – 13, 2014 (Mon – Tues)
Munich, Germany

Semiconductor Reliability
May 12 – 14, 2014 (Mon – Wed)
Munich, Germany

Product Qualification
May 15 – 16, 2014 (Thur – Fri)
Munich, Germany